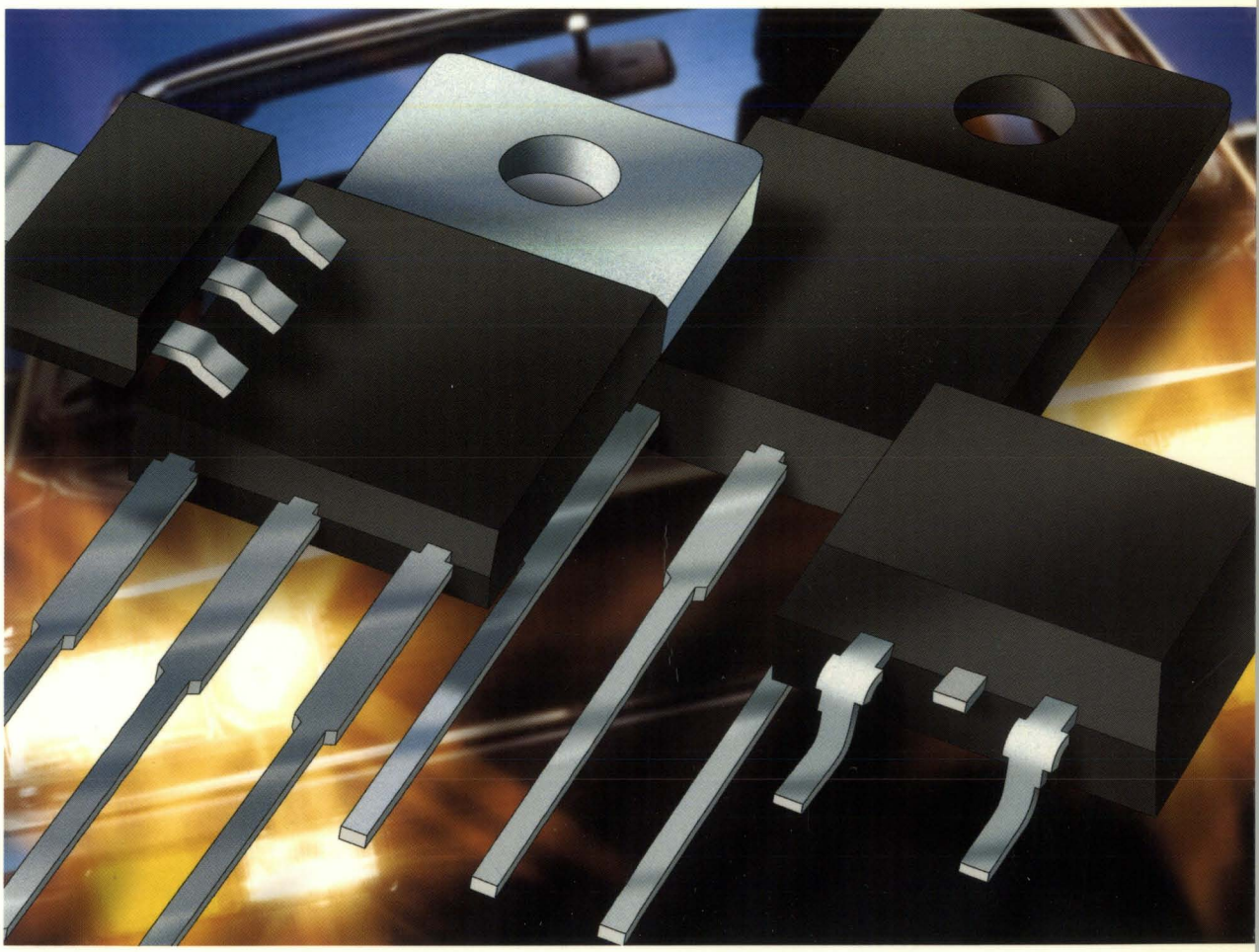
DISCRETE SEMICONDUCTORS

PowerMOS Transistors incl. TOPFETs and IGBTs



1997

Data Handbook SC13a

Let's make things better.

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

PowerMOS Transistors incl. TOPFETs and IGBTs

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Dear Customer,

We are pleased to introduce this new update of Philips Semiconductors' PowerMOS Transistors data handbook, SC13a. In this book you will find a number of exciting new products, such as TrenchMOS, Surface Mount MOSFETs and a new range of Commodity PowerMOS products. More details are available in the section called "New Products".

We are planning to publish a new data handbook, SC13b, by mid 1997, which will be called "Small-signal and Medium-power MOS Transistors". Together with this new SC13a you will have a complete overview of Philips Semiconductors' product offering in small-signal, medium and high-power MOS transistors.

Thank you very much for using Philips Semiconductors' devices.

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PowerMOS Transistors including TOPFETs and IGBTs

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Types added to the range since the last issue of data handbook SC13 (1995) are shown in bold print.

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SELECTION GUIDE

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
50	0.028	25	50	125	BUK106-50L	TOPFET	SOT263
50	0.028	25	50	125	BUK106-50LP	TOPFET	SOT263-01
50	0.028	25	50	125	BUK116-50L	TOPFET	SOT426
50	0.028	25	50	125	BUK106-50S	TOPFET	SOT263
50	0.028	25	50	125	BUK106-50SP	TOPFET	SOT263-01
50	0.028	25	50	125	BUK116-50S	TOPFET	SOT426
50	0.028	25	50	125	BUK102-50GS	TOPFET	TO220AB
50	0.028	25	50	125	BUK110-50GS	TOPFET	SOT404
50	0.035	25	45	125	BUK102-50DL	TOPFET	TO220AB
50	0.035	25	45	125	BUK110-50DL	TOPFET	SOT404
50	0.035	25	45	125	BUK102-50GL	TOPFET	TO220AB
50	0.035	25	45	125	BUK110-50GL	TOPFET	SOT404
50	0.05	13	29	75	BUK101-50GS	TOPFET	TO220AB
50	0.05	13	29	75	BUK109-50GS	TOPFET	SOT404
50	0.06	13	26	75	BUK101-50DL	TOPFET	TO220AB
50	0.06	13	26	75	BUK109-50DL	TOPFET	SOT404
50	0.06	13	26	75	BUK101-50GL	TOPFET	TO220AB
50	0.06	13	26	75	BUK109-50GL	TOPFET	SOT404
50	0.093	6	12	52	BUK111-50GL	TOPFET	SOT426
50	0.093	6	12	52	BUK112-50GL	TOPFET	SOT263-01
50	0.1	7.5	15	40	BUK104-50L	TOPFET	SOT263
50	0.1	7.5	15	40	BUK104-50LP	TOPFET	SOT263-01
50	0.1	7.5	15	40	BUK114-50L	TOPFET	SOT426
50	0.1	7.5	15	40	BUK104-50S	TOPFET	SOT263
50	0.1	7.5	15	40	BUK104-50SP	TOPFET	SOT263-01
50	0.1	7.5	15	40	BUK114-50S	TOPFET	SOT426
50	0.1	7.5	15	40	BUK100-50GS	TOPFET	TO220AB
50	0.1	7.5	15	40	BUK108-50GS	TOPFET	SOT404
50	0.125	7.5	13.5	40	BUK100-50DL	TOPFET	TO220AB
50	0.125	7.5	13.5	40	BUK108-50DL	TOPFET	SOT404
50	0.125	7.5	13.5	40	BUK100-50GL	TOPFET	TO220AB
50	0.125	7.5	13.5	40	BUK108-50GL	TOPFET	SOT404
50	0.175	0.1	0.7	1.8	BUK107-50DS	TOPFET	SOT223
50	0.2	0.1	0.7	1.8	BUK107-50DL	TOPFET	SOT223
50	0.2	0.1	0.7	1.8	BUK107-50GL	TOPFET	SOT223

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
50	0.2	1	4	4	BUK113-50DL[1]	TOPFET	SOT223
50	0.038	10	20	125	BUK202-50X	TOPFET High side switch	SOT263-01
50	0.038	10	20	125	BUK202-50Y	TOPFET High side switch	SOT263-01
50	0.038	10	20	125	BUK206-50X	TOPFET High side switch	SOT426
50	0.038	10	20	125	BUK206-50Y	TOPFET High side switch	SOT426
50	0.06	7.5	15	83.3	BUK201-50X	TOPFET High side switch	SOT263-01
50	0.06	7.5	15	83.3	BUK201-50Y	TOPFET High side switch	SOT263-01
50	0.06	7.5	15	83.3	BUK205-50X	TOPFET High side switch	SOT426
50	0.06	7.5	15	83.3	BUK205-50Y	TOPFET High side switch	SOT426
50	0.1	5	10	62.5	BUK200-50X	TOPFET High side switch	SOT263-01
50	0.1	5	10	62.5	BUK200-50Y	TOPFET High side switch	SOT263-01
50	0.1	5	10	62.5	BUK204-50X	TOPFET High side switch	SOT426
50	0.1	5	10	62.5	BUK204-50Y	TOPFET High side switch	SOT426
50	0.22	2	4	50	BUK203-50X	TOPFET High side switch	SOT263-01
50	0.22	2	4	50	BUK203-50Y	TOPFET High side switch	SOT263-01
50	0.22	2	4	50	BUK207-50X	TOPFET High side switch	SOT426
50	0.22	2	4	50	BUK207-50Y	TOPFET High side switch	SOT426

1 In development at date of handbook publication.

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
48	0.085	10	21	75	BUK553-48C	Protected L^2FET N	TO220AB
48	0.085	10	21	75	BUK563-48C	Protected L^2FET N	SOT404
48	0.085	10	13	50	BUK573-48C	Protected L^2FET N	SOT186A

* indicates new types which will be available Q1/Q2 1997

55	0.008	25	75	187	BUK7508-55	TrenchMOS N	TO220AB
55	0.008	25	75	187	BUK7608-55 *	TrenchMOS N	SOT404
55	0.008	25	75	187	BUK9508-55	L^2TrenchMOS N	TO220AB
55	0.008	25	75	187	BUK9608-55 *	L^2TrenchMOS N	SOT404
55	0.014	25	68	142	BUK7514-55	TrenchMOS N	TO220AB
55	0.014	25	68	142	BUK7614-55 *	TrenchMOS N	SOT404
55	0.014	25	68	142	BUK9514-55	L^2TrenchMOS N	TO220AB
55	0.014	25	68	142	BUK9614-55 *	L^2TrenchMOS N	SOT404
55	0.018	25	57	125	BUK7518-55	TrenchMOS N	TO220AB
55	0.018	25	57	125	BUK7618-55 *	TrenchMOS N	SOT404
55	0.018	25	57	125	BUK9518-55	L^2TrenchMOS N	TO220AB
55	0.018	25	57	125	BUK9618-55 *	L^2TrenchMOS N	SOT404
55	0.020	25	52	115	BUK7520-55 *	TrenchMOS N	TO220AB
55	0.020	25	52	115	BUK7620-55 *	TrenchMOS N	SOT404
55	0.020	25	52	115	BUK9520-55 *	L^2TrenchMOS N	TO220AB
55	0.020	25	52	115	BUK9620-55 *	L^2TrenchMOS N	SOT404
55	0.024	25	45	103	BUK7524-55	TrenchMOS N	TO220AB
55	0.024	25	45	103	BUK7624-55 *	TrenchMOS N	SOT404
55	0.024	25	45	103	BUK9524-55	L^2TrenchMOS N	TO220AB
55	0.024	25	45	103	BUK9624-55 *	L^2TrenchMOS N	SOT404
55	0.030	15	30	75	BUK7530-55 *	TrenchMOS N	TO220AB
55	0.030	15	30	75	BUK7630-55 *	TrenchMOS N	SOT404
55	0.030	15	30	75	BUK9530-55 *	L^2TrenchMOS N	TO220AB
55	0.030	15	30	75	BUK9630-55 *	L^2TrenchMOS N	SOT404
55	0.040	5	10.7	8.3	BUK7840-55 *	TrenchMOS N	SOT223
55	0.040	5	10.7	8.3	BUK9840-55 *	L^2TrenchMOS N	SOT223
55	0.070	10	19	60	BUK7570-55 *	TrenchMOS N	TO220AB
55	0.070	10	19	60	BUK7670-55 *	TrenchMOS N	SOT404
55	0.070	10	19	60	BUK9570-55 *	L^2TrenchMOS N	TO220AB
55	0.070	10	19	60	BUK9670-55 *	L^2TrenchMOS N	SOT404

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
55	0.080	5	7.5	8.3	BUK7880-55 *	TrenchMOS N	SOT223
55	0.080	5	7.5	8.3	BUK9880-55 *	L²TrenchMOS N	SOT223
55	0.150	5	5.5	8.3	BUK78150-55 *	TrenchMOS N	SOT223
55	0.150	5	5.5	8.3	BUK98150-55 *	L²TrenchMOS N	SOT223
60	0.020	25	60	150	BUK466-60H	MOSFET N	SOT404
60	0.020	25	60	150	BUK456-60H	MOSFET N	TO220AB
60	0.022	25	60	150	BUK556-60H	L²FET N	TO220AB
60	0.022	25	60	150	BUK566-60H	L²FET N	SOT404
60	0.026	25	50	150	BUK556-60A	L²FET N	TO220AB
60	0.026	25	50	150	BUK566-60A	L²FET N	SOT404
60	0.028	29	52	150	BUK456-60A	MOSFET N	TO220AB
60	0.028	29	52	150	BUK466-60A	MOSFET N	SOT404
60	0.028	29	52	150	PHP50N06	MOSFET N	TO220AB
60	0.03	29	51	150	BUK456-60B	MOSFET N	TO220AB
60	0.03	20	43	125	BUK465-60H	MOSFET N	SOT404
60	0.03	20	43	125	BUK455-60H	MOSFET N	TO220AB
60	0.03	20	22.5	30	BUK475-60H	MOSFET N	SOT186A
60	0.038	20	41	125	BUK455-60A	MOSFET N	TO220AB
60	0.038	20	41	125	BUK555-60H	L²FET N	TO220AB
60	0.038	20	41	125	BUK454-60H	MOSFET N	TO220AB
60	0.038	20	21	30	BUK474-60H	MOSFET N	SOT186
60	0.038	20	41	125	BUK464-60H	MOSFET N	SOT404
60	0.038	20	21	30	BUK545-60H	L²FET N	SOT186
60	0.038	20	41	125	BUK565-60H	L²FET N	SOT404
60	0.038	20	41	125	BUK465-60A	MOSFET N	SOT404
60	0.038	20	21	30	BUK475-60A	MOSFET N	SOT186A
60	0.038	20	41	125	PHP36N06E	MOSFET N	TO220AB
60	0.038	20	41	125	PHB36N06E	MOSFET N	SOT404
60	0.042	20	39	125	BUK555-60A	L²FET N	TO220AB
60	0.042	20	20	30	BUK545-60A	L²FET N	SOT186
60	0.042	20	39	125	BUK554-60H	L²FET N	TO220AB
60	0.042	20	20	30	BUK574-60H	L²FET N	SOT186A
60	0.042	20	39	125	BUK564-60H	L²FET N	SOT404
60	0.042	20	39	125	BUK565-60A	L²FET N	SOT404

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
60	0.045	20	38	125	BUK455-60B	MOSFET N	TO220AB
60	0.045	220	20	30	BUK475-60B	MOSFET N	SOT186A
60	0.055	20	35	125	BUK555-60B	L²FET N	TO220AB
60	0.055	20	18	30	BUK545-60B	L²FET N	SOT186
60	0.08	10	22	75	BUK453-60A	MOSFET N	TO220AB
60	0.08	10	22	75	BUK463-60A	MOSFET N	SOT404
60	0.08	9	13	25	BUK473-60A	MOSFET N	SOT186A
60	0.08	10	22	75	PHP20N06E	MOSFET N	TO220AB
60	0.08	9	13	25	PHX15N06E	MOSFET N	SOT186A
60	0.085	10	21	75	BUK553-60A	L²FET N	TO220AB
60	0.085	10	21	75	BUK563-60A	L²FET N	SOT404
60	0.085	10	13	25	BUK543-60A	L²FET N	SOT186
60	0.1	10	20	75	BUK553-60B	L²FET N	TO220AB
60	0.1	10	20	75	BUK453-60B	MOSFET N	TO220AB
60	0.1	10	12	25	BUK543-60B	L²FET N	SOT186
60	0.1	3.2	3.2	1.8	BUK483-60A	MOSFET N	SOT223
60	0.1	3.2	3.2	1.8	BUK583-60A	L²FET N	SOT223
60	0.1	9	12	25	BUK473-60B	MOSFET N	SOT186A
60	0.13	8.5	15	60	BUK452-60A	MOSFET N	TO220AB
60	0.13	2.5	2.5	1.7	BUK482-60A	MOSFET N	SOT223
60	0.13	8.5	15	60	BUK462-60A	MOSFET N	SOT404
60	0.13	8.5	10	22	BUK472-60A	MOSFET N	SOT186A
60	0.13	8.5	15	60	PHP15N06E	MOSFET N	TO220AB
60	0.15	8.5	14	60	BUK552-60A	L²FET N	TO220AB
60	0.15	8.5	9.2	22	BUK542-60A	L²FET N	SOT186
60	0.15	8.5	14	60	BUK452-60B	MOSFET N	TO220AB
60	0.15	2.7	2.7	1.7	BUK582-60A	L²FET N	SOT223
60	0.15	8.5	14	60	BUK562-60A	L²FET N	SOT404
60	0.15	8.5	9.2	22	BUK472-60B	MOSFET N	SOT186A
60	0.15	6	12	40	PHP3055E	MOSFET N	TO220AB
60	0.18	8.5	13	60	BUK552-60B	L²FET N	TO220AB
60	0.18	6	12	40	PHP3055L	L²FET N	TO220AB
60	0.18	8.5	8.4	22	BUK542-60B	L²FET N	SOT186
60	0.35	1.6	1.6	1.5	BUK481-60A	MOSFET N	SOT223
60	0.40	1.5	1.5	1.5	BUK581-60A	L²FET N	SOT223

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
100	0.038	20	41	125	PHP10N10E	MOSFET N	TO220AB
100	0.057	15	34	150	BUK456-100A	MOSFET N	TO220AB
100	0.057	15	34	150	PHP33N10	MOSFET N	TO220AB
100	0.065	15	32	150	BUK456-100B	MOSFET N	TO220AB
100	0.08	13	26	125	BUK455-100A	MOSFET N	TO220AB
100	0.08	13	14	30	BUK475-100A	MOSFET N	SOT186A
100	0.08	13	26	125	PHP26N10E	MOSFET N	TO220AB
100	0.085	13	25	125	BUK555-100A	L^2FET N	TO220AB
100	0.085	13	13	30	BUK545-100A	L^2FET N	SOT186
100	0.1	13	23	125	BUK455-100B	MOSFET N	TO220AB
100	0.1	13	12	30	BUK475-100B	MOSFET N	SOT186A
100	0.11	13	22	125	BUK555-100B	L^2FET N	TO220AB
100	0.11	13	12	30	BUK545-100B	L^2FET N	SOT186
100	0.16	5	14	75	BUK453-100A	MOSFET N	TO220AB
100	0.16	5	9	25	BUK473-100A	MOSFET N	SOT186A
100	0.16	5	14	75	PHP12N10E	MOSFET N	TO220AB
100	0.18	5	8.3	25	BUK543-100A	L^2FET N	SOT186
100	0.18	6.5	13	75	BUK553-100A	L^2FET N	TO220AB
100	0.2	5	13	75	BUK453-100B	MOSFET N	TO220AB
100	0.2	5	8	25	BUK473-100B	MOSFET N	SOT186A
100	0.22	5	7.5	25	BUK543-100B	L^2FET N	SOT186
100	0.22	6.5	12	75	BUK553-100B	L^2FET N	TO220AB
100	0.25	5.5	11	60	BUK452-100A	MOSFET N	TO220AB
100	0.25	5.5	6.6	22	BUK472-100A	MOSFET N	SOT186A
100	0.28	5.5	6.3	22	BUK542-100A	L^2FET N	SOT186
100	0.28	5.5	10	60	BUK552-100A	L^2FET N	TO220AB
100	0.28	1.8	1.8	1.8	BUK482-100A	MOSFET N	SOT223
100	0.3	5.5	10	60	BUK452-100B	MOSFET N	TO220AB
100	0.3	5.5	6.1	22	BUK472-100B	MOSFET N	SOT186A
100	0.31	1.7	1.7	1.8	BUK582-100A	L^2FET N	SOT223
100	0.35	5.5	8.5	60	BUK552-100B	L^2FET N	TO220AB
100	0.35	5.5	5.6	22	BUK542-100B	L^2FET N	SOT186
100	0.8	1	1	1.5	BUK481-100A	MOSFET N	SOT223
100	0.9	0.9	.9	1.5	BUK581-100A	L^2FET N	SOT223
100	0.25	5.5	11	60	BUK462-100A	MOSFET N	SOT404

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
100	0.28	5.5	10	60	BUK562-100A	L^2FET N	SOT404
100	0.16	5	14	75	BUK463-100A	MOSFET N	SOT404
100	0.18	6.5	13	75	BUK563-100A	L^2FET N	SOT404
100	0.08	13	26	125	BUK465-100A	MOSFET N	SOT404
100	0.085	13	14	30	BUK565-100A	L^2FET N	SOT404
100	0.057	15	34	150	BUK466-100A	MOSFET N	SOT404
200	0.16	10	19	150	BUK456-200A	MOSFET N	TO220AB
200	0.18	11	18	136	PHP18N20E	MOSFET N	TO220AB
200	0.2	10	17	150	BUK456-200B	MOSFET N	TO220AB
200	0.23	7	7.6	30	BUK545-200A	L^2FET N	SOT186
200	0.23	7	7.6	30	BUK445-200A	MOSFET N	SOT186
200	0.23	7	14	125	BUK555-200A	L^2FET N	TO220AB
200	0.23	7	14	125	BUK455-200A	MOSFET N	TO220AB
200	0.23	7	7.6	30	BUK475-200A	MOSFET N	SOT186A
200	0.28	7	7	30	BUK545-200B	L^2FET N	SOT186
200	0.28	7	7	30	BUK445-200B	MOSFET N	SOT186
200	0.28	7	13	125	BUK555-200B	L^2FET N	TO220AB
200	0.28	7	13	125	BUK455-200B	MOSFET N	TO220AB
200	0.28	7	7	30	BUK475-200B	MOSFET N	SOT186A
200	0.4	3.5	9.2	90	BUK454-200A	MOSFET N	TO220AB
200	0.4	3.5	9.2	90	BUK554-200A	L^2FET N	TO220AB
200	0.4	3.5	5.3	25	BUK444-200A	MOSFET N	SOT186
200	0.4	3.5	5.3	25	BUK474-200A	MOSFET N	SOT186A
200	0.4	3.5	9.2	90	PHP8N20E	MOSFET N	TO220AB
200	0.5	3.5	8.2	90	BUK454-200B	MOSFET N	TO220AB
200	0.5	3.5	8.2	90	BUK554-200B	L^2FET N	TO220AB
200	0.5	3.5	4.7	25	BUK444-200B	MOSFET N	SOT186
200	0.23	7	14	125	BUK565-200A	L^2FET N	SOT404
200	0.23	7	14	125	BUK465-200A	MOSFET N	SOT404
200	0.4	3.5	9.2	90	BUK564-200A	L^2FET N	SOT404
200	0.4	3.5	9.2	90	BUK464-200A	MOSFET N	SOT404
200	0.16	10	19	150	BUK466-200A	MOSFET N	SOT404
200	0.5	3.5	4.7	25	BUK474-200B	MOSFET N	SOT186A
200	0.8	2.5	5	40	PHP5N20E	MOSFET N	TO220AB

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
200	0.9	2	2	8.3	BUK482-200A	MOSFET N	SOT223
200	1.5	1.7	3.5	20	PHP3N20E	MOSFET N	TO220AB
400	0.55	5	10	125	PHP10N40E	MOSFET N	TO220AB
400	0.55	5	4.9	30	PHX5N40E	MOSFET N	SOT186A
400	1	3.25	6.5	100	PHP5N40E	MOSFET N	TO220AB
400	1	3.25	3.6	30	PHX4N40E	MOSFET N	SOT186A
400	1.8	2.1	4.2	75	PHP4N40E	MOSFET N	TO220AB
400	1.8	2.1	2.4	25	PHX2N40E	MOSFET N	SOT186A
400	3.5	1.25	2.5	50	PHP2N40E	MOSFET N	TO220AB
400	3.5	1.25	1.75	25	PHX1N40E	MOSFET N	SOT186A
500	0.8	4	8	125	PHP8N50E	MOSFET N	TO220AB
500	0.8	4	4	30	PHX5N50E	MOSFET N	SOT186A
500	1.5	2.65	5.3	100	PHP4N50E	MOSFET N	TO220AB
500	1.5	2.65	2.9	30	PHX4N50E	MOSFET N	SOT186A
500	3	1.6	3.2	75	PHP3N50E	MOSFET N	TO220AB
500	3	1.6	1.9	25	PHX2N50E	MOSFET N	SOT186A
500	5	1	2	50	PHP1N50E	MOSFET N	TO220AB
500	5	1	1.4	25	PHX1N50E	MOSFET N	SOT186A
600	1.2	3.25	6.5	125	PHP6N60E	MOSFET N	TO220AB
600	1.2	3.25	3.2	30	PHX4N60E	MOSFET N	SOT186A
600	2.2	2.15	4.3	100	PHP3N60E	MOSFET N	TO220AB
600	2.2	2.15	2.4	30	PHX2N60E	MOSFET N	SOT186A
600	4.4	1.3	2.6	75	PHP2N60E	MOSFET N	TO220AB
600	6	0.9	1.9	50	PHP1N60E	MOSFET N	TO220AB
600	6	0.9	1.3	25	PHX1N60E	MOSFET N	SOT186A

V_{DS} (V)	$R_{DS(ON)}$ (Ω)	@I_D (A)	I_D (A)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
800	3	1.5	4	125	BUK456-800A	MOSFET N	TO220AB
800	3	1.5	2	30	BUK446-800A	MOSFET N	SOT186
800	4	1.5	3.5	125	BUK456-800B	MOSFET N	TO220AB
800	4	1.5	1.7	30	BUK446-800B	MOSFET N	SOT186
800	6	1	2.4	100	BUK454-800A	MOSFET N	TO220AB
800	6	1.0	1.4	30	BUK444-800A	MOSFET N	SOT186
800	8	1	2.0	100	BUK454-800B	MOSFET N	TO220AB
800	8	1	1.2	30	BUK444-800B	MOSFET N	SOT186
1000	5	1.5	3.1	125	BUK456-1000B	MOSFET N	TO220AB
1000	5	1.5	1.5	30	BUK446-1000B	MOSFET N	SOT186

Insulated Gate Bipolar Transistors (IGBTs)

V_{CE} (V)	$V_{CE(SAT)}$ (V)	I_C (A)	t_f (μs)	P_D (W)	TYPE NUMBER	TECHNOLOGY	ENVELOPE
400	2.2	15	10	125	BUK856-400IZ	Protected L^2IGBT	TO220AB
400	2.2	15	10	125	BUK866-400IZ	Protected L^2IGBT	SOT404
800	3.5	12	0.4	85	BUK854-800A	Fast IGBT	TO220AB
800	3.5	24	0.4	125	BUK856-800A	Fast IGBT	TO220AB

REPLACED / WITHDRAWN TYPES

The following type numbers were in the previous issue of this handbook, but are not in the current version:

TYPE NUMBER	REPLACED BY	REASON FOR DELETION
BUK105-50L	see BUK104/106-50L	
BUK105-50LP	see BUK104/106-50LP	
BUK105-50S	see BUK104/106-50S	
BUK105-50SP	see BUK104/106-50SP	
BUK444-400B	PHX4N40E	
BUK444-500B	PHX3N50E	
BUK444-600B	PHX2N60E	
BUK445-400B	PHX5N40E	
BUK445-500B	PHX4N50E	
BUK445-600B	PHX3N60E	
BUK454-400B	PHP4N40E	
BUK454-500B	PHP3N50E	
BUK454-600B	PHP2N60E	
BUK455-400B	PHP5N40E	
BUK455-500B	PHP4N50E	
BUK455-600B	PHP3N60E	
BUK457-400B	PHP10N40E	
BUK457-500B	PHP8N50E	
BUK457-600B	PHP6N60E	
BUK655-500B		non preferred
BUK657-400B		non preferred
BUK657-500B		non preferred
BUK854-500IS	see BUK856-400IZ	
BUK856-450IX	see BUK856-400IZ	
BUK445-60A	BUK475-60A	
BUK445-60B	BUK475-60B	
BUK445-60H	BUK475-60H	
BUK443-60A	BUK473-60A	
BUK443-60B	BUK473-60B	
BUK445-100A	BUK475-100A	
BUK445-100B	BUK475-100B	
BUK443-100A	BUK473-100A	
BUK443-100B	BUK473-100B	
BUK442-100A	BUK472-100A	
BUK442-100B	BUK472-100B	

INTRODUCTION

QUALITY

Total Quality Management

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

QUALITY ASSURANCE

Based on ISO9000 standards, customer standards such as Ford TQE, CDF-AEC-Q100 & -Q101 and IBM MDQ and the CECC system of conformity. Our factories are certified to ISO 9000, QS9000 and CECC by external inspectorates and to Philips' own PQA90 award.

PARTNERSHIPS WITH CUSTOMERS

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

PARTNERSHIPS WITH SUPPLIERS

Ship-to-stock, statistical process control and ISO 9000 audits.

QUALITY IMPROVEMENT PROGRAMME

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

Recognition

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

TYPE NUMBERS

Philips Power MOSFETs and related products can be grouped into three distinct type number schemes. The Type numbers are made up as follows:

a) Standard DMOS - 'BUKxxx' type numbers

The format is BUK prefix then a 3-digit 'type code' and a hyphen followed by a voltage and a single or two letter suffix.

The 3-digit 'type code' conform to the scheme shown in the table below. The first digit defines the technology, the second outline and the third indicates the approximate chip size. TOPFET's use a modified scheme where the second and third digits are chosen sequentially as each new type is released.

Example: BUK563-60A is a logic level FET in SOT404 outline~ with a size 3 chip, 60V rated maximum V_{DS} and top grade: R_{DS}(on).

b) TrenchMOS™ Type Numbers

The TrenchMOS™ type numbering scheme system follows a similar scheme the standard DMOS range. Again the first digit after BUK refers to the technology: '7' for a standard level device and '9' for a logic level device. The second digit is again the package designation and follows the same relationship as the DMOS range. These are also shown in the table below. The major difference with the TrenchMOS™ numbering scheme is the use of the subsequent two digits to express the R_{DS}(on) maximum rating of the device in mΩ. TrenchMOS™ devices can therefore be identified easily as they have a 4 digit 'type code' after the BUK prefix.

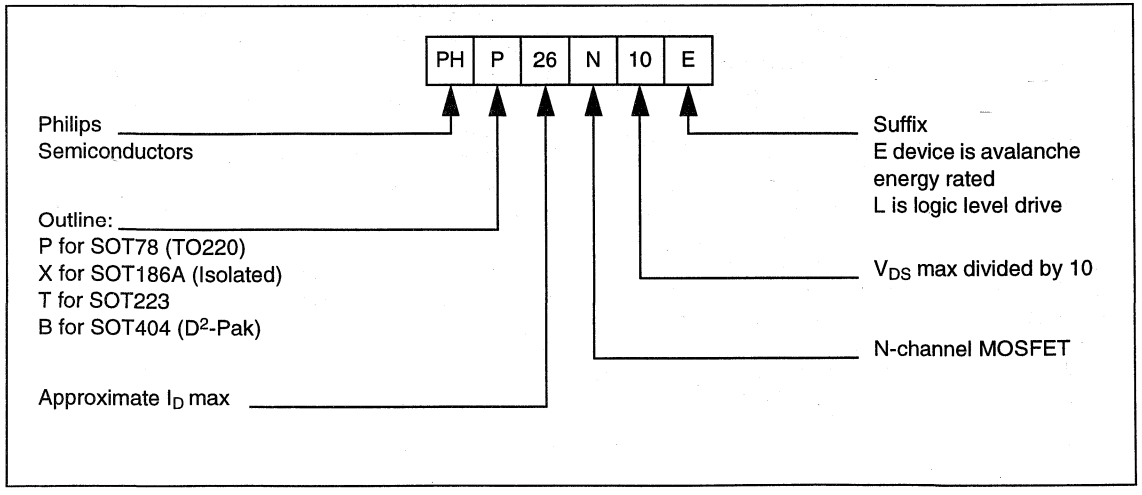
Example: BUK7508-55 is a standard level TrenchMOS™ device in a SOT78 with an R_{DS}(on) maximum rating of 8mOhms and a 55V maximum drain-source rating.

DIGIT	1st	2nd	3rd
CODE	TECHNOLOGY	OUTLINE	CHIP SIZE (mm^2)
0	(-)	(-)	(-)
1	L.S. TOPFET	(-)	2
2	H.S. TOPFET	SOT428	4
3	(-)	(-)	6
4	NMOSFET	SOT186	8
5	L^2FET	TO220AB	14
6	(-)	SOT404	20
7	STD TRENCH	SOT186A	25
8	IGBT	SOT223	36
9	L^2TRENCH	SOT262	42

c) PHP style type numbers

A new range of products has recently been released under this scheme which is designed for easy cross reference to industry standard type numbers.

There Is one notable exception to this scheme - the PHP3055E family. For historical reasons this industry standard device does not conform



FEATURES

Higher maximum junction temperature

All of the low voltage types (up to 200 V) in TO220AB outlines are now published with T_j(max) of 175 °C.

Logic level gate

This range of products has logic level gate drive. These can be fully switched on with a VGS of only 5 V and is therefore compatible with standard digital integrated circuits.

Ruggedness

The majority of the products in this book are 100% tested to guarantee the published avalanche energy rating.

Application information

Application information for power MOS devices and other Philips Semiconductors power products is published in the power Semiconductors Applications Handbook. The order code for this publication is; 9398 652 85011

The Applications Handbook contains information on the theory of power transistors and diodes in typical applications such as SMPS and TV deflection circuits. Examples are included to support the theory.

A number of other useful technical publications and cross reference guides are available through our fact sheet system.

NEW PRODUCTS

Philips Semiconductors are working intensively on bringing new products to the market in PowerMOS and related technologies. These are the new products and technologies that appear for the first time in this data handbook.

TrenchMOS™

TrenchMOS™ is Philips Semiconductors' revolutionary new MOSFET design which delivers extremely low R_{DS}(On) performance. Compared with the standard DMOS process, TrenchMOS™ achieves reductions of up to 55% in R_{DS}(on) performance. This translates into significant benefits such as improved current handling, die size reductions and lower power dissipation. TrenchMOS™ allows the same current handling capability to be achieved with a die size two thirds the traditional DMOS size.

This is possible since the lower R_{DS}(on) value offsets the increased thermal resistance of a smaller die area. The process also offers rugged avalanche capability and excellent reliability. All Philips TrenchMOS™ devices have built in ESD protection.

Surface Mount Power- SOT404/S0T426 outlines

SOT404 is the Philips surface mount equivalent to the very popular SOT78 (TO220) package. The introduction of SOT404 again underlines Philips commitment to surface mount technologies. SOT404 is a purpose designed surface mount package with many design differences over the SOT78 (T0220) through hole package. SOT404 has selective plating on a specifically designed leadframe, revised die attach methods, and a new plastic compound ideally suited to the demanding environment of surface mount.

SOT404 is a three pin package and is complemented by the SOT426, a five pin version which is particularly relevant for the TOPFET range of devices.

Commodity PowerMOS range

An extended range of PowerMOS devices under the new PHP style type numbering scheme described in the last section. The new types are designed as close equivalents to types widely accepted as industry standard. The choice of part numbering strongly underlines this strategy.

Medium Voltage PowerMOS

In recent years Philips Semiconductors has not been focused on the medium and high voltage MOSFET market. We define this area as those MOSFETs with a V_{DS}(max) of 400 V and up. As a direct result of increased capacity and market focus we have redesigned our medium voltage range to re-address this market. Objective specifications for the first range of devices are included for the first time in this edition of SC13, comprising devices in TO220, SOT186A and SOT223 outlines. A number of range extensions are planned for 1997. The new range all carry a 'ruggedness' rating which is specified in the data sheets as a maximum unclamped inductive load turn-off energy.

These new releases demonstrate our commitment to enhancing our position as a broad range Power Semiconductor supplier.

All manufacturers of power MOSFETs provide a data sheet for every type produced. The purpose of the data sheet is primarily to give an indication as to the capabilities of a particular product. It is also useful for the purpose of selecting device equivalents between different manufacturers. In some cases however data on a number of parameters may be quoted under subtly different conditions by different manufacturers, particularly on second order parameters such as switching times. In addition the information contained within the data sheet does not always appear relevant for the application. Using data sheets and selecting device equivalents therefore requires caution and an understanding of exactly what the data means and how it can be interpreted. Throughout this chapter the BUK553-100A is used as an example, this device is a 100 V logic level MOSFET.

Information contained in the Philips data sheet

The data sheet is divided into 8 sections as follows:

* Quick reference data
* Limiting values
* Thermal resistances
* Static characteristics
* Dynamic characteristics
* Reverse diode limiting values and characteristics
* Avalanche limiting value
* Graphical data

The information contained within each of these sections is now described.

Quick reference data

This data is presented for the purpose of quick selection. It lists what is considered to be the key parameters of the device such that a designer can decide at a glance whether the device is likely to be the correct one for the application or not. Five parameters are listed, the two most important are the drain-source voltage V_{DS} and drain-source on-state resistance, $R_{DS(ON)}$. V_{DS} is the maximum voltage the device will support between drain and source terminals in the off-state. $R_{DS(ON)}$ is the maximum on-state resistance at the quoted gate voltage, V_{GS}, and a junction temperature of 25 °C. (NB $R_{DS(ON)}$ is temperature dependent, see static characteristics). It is these two parameters which provide a first order indication of the devices capability.

A drain current value (I_D) and a figure for total power dissipation are also given in this section. These figures should be treated with caution since they are quoted for conditions that are rarely attainable in real applications. (See limiting values.) For most applications the usable dc current will be less than the quoted figure in the quick reference data. Typical power dissipations that can be tolerated by the majority of designers are less than 20 W (for discrete devices), depending on the heatsinking arrangement used. The junction temperature (T_J) is usually given as either 150 °C or 175 °C. It is not recommended that the internal device temperature be allowed to exceed this figure.

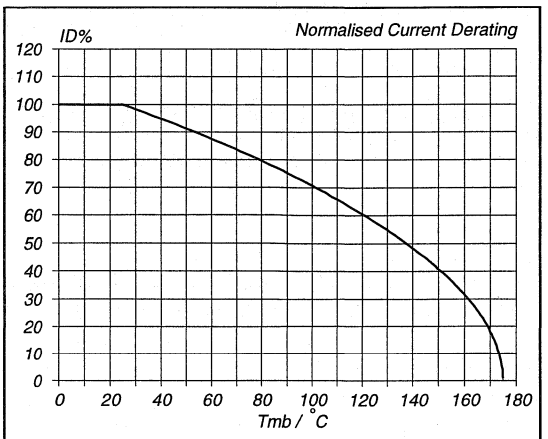


Fig.1 Normalised continuous drain current.
ID% = 100 . $I_D/I_{D25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

Limiting values

This table lists the absolute maximum values of six parameters. The device may be operated right up to these maximum levels however they must not be exceeded, to do so may incur damage to the device.

Drain-source voltage and drain-gate voltage have the same value. The figure given is the maximum voltage that may be applied between the respective terminals. Gate-source voltage, $\pm V_{GS}$, gives the maximum value that may be allowed between the gate and source terminals. To exceed this voltage, even for the shortest period can cause permanent damage to the gate oxide. Two values for the dc drain current, I_D, are quoted, one at a mounting base temperature of 25 °C and one at a mounting base temperature of 100 °C. Again these currents do not represent attainable operating levels. These currents are the values that will cause the junction temperature to reach its maximum value when the mounting base is held at the quoted value. The maximum current rating is therefore a function of the mounting base temperature and the quoted figures are just two points on the derating curve ,see Fig.1.

The third current level quoted is the pulse peak value, I_{DM}. PowerMOS devices generally speaking have a very high peak current handling capability. It is the internal bond wires which connect to the chip that provide the final limitation. The pulse width for which I_{DM} can be applied depends upon the thermal considerations (see section on calculating currents.) The total power dissipation, P_{tot}, and maximum junction temperature are also stated as for the quick reference data. The P_{tot} figure is calculated from the simple quotient given in equation 1 (see section on safe

operating area). It is quoted for the condition where the mounting base temperature is maintained at 25 °C. As an example, for the BUK553-100A the P_{tot} figure is 75 W, dissipating this amount of power while maintaining the mounting base at 25 °C would be a challenge! For higher mounting base temperatures the total power that can be dissipated is less. Obviously if the mounting base temperature was made equal to the max permitted junction temperature, then no power could be dissipated internally. A derating curve is given as part of the graphical data, an example is shown in Fig.2 for a device with a limiting T_j of 175 °C.

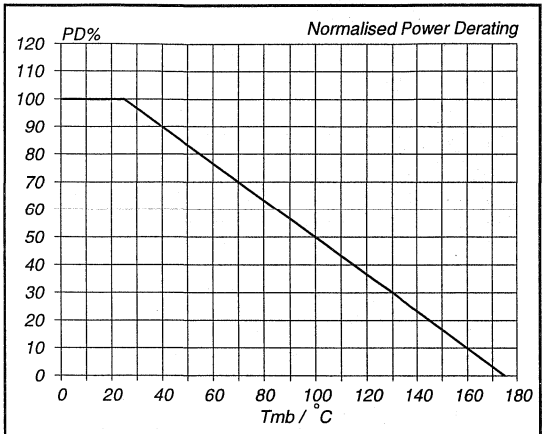


Fig.2 Normalised power dissipation.
PD% = 100 $P_D/P_{D\ 25\ °C}$ = f(T_{mb})

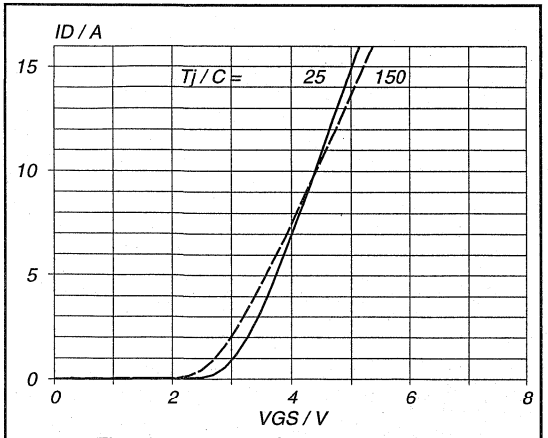


Fig.3 Typical transfer characteristics.
I_D = f(V_{GS}); conditions: V_{DS} = 25 V; parameter T_j

Storage temperature limits are also quoted, usually between -40 /-55 °C and +150 /+175 °C. Both the storage temperature limits and the junction temperature limit are figures at which extensive reliability work is performed by our Quality department. To exceed these figures will cause a reduction in long-term reliability.

Thermal resistance.

For non-isolated packages two thermal resistance values are given. The value from junction to mounting base (R_{thj-mb}) indicates how much the junction temperature will be raised above the temperature of the mounting base when dissipating a given power. Eg a BUK553-100A has a R_{thj-mb} of 2 K/W, dissipating 10 W, the junction temperature will be 20 °C above the temperature of its mounting base. The other figure quoted is from junction to ambient. This is a much larger figure and indicates how the junction temperature will rise if the device is NOT mounted on a heatsink but operated in free air. Eg for a BUK553-100A, R_{thj-a} = 60 K/W, dissipating 1 W while mounted in free air will produce a junction temperature 60 °C above the ambient air temperature.

For isolated packages, (F-packs) the mounting base (the metal plate upon which the silicon chip is mounted) is fully encapsulated in plastic. Therefore it is not possible to give a thermal resistance figure junction to mounting base. Instead a figure is quoted from junction to heatsink, R_{thj-hs}, which assumes the use of heatsink compound. Care should be taken when comparing thermal resistances of isolated and non-isolated types. Consider the following example:

The non-isolated BUK553-100A has a R_{thj-mb} of 2 K/W. The isolated BUK543-100A has a R_{thj-hs} of 5 K/W. These devices have identical crystals but mounted in different packages. At first glance the non-isolated type might be expected to offer much higher power (and hence current) handling capability. However for the BUK553-100A the thermal resistance junction to heatsink has to be calculated, this involves adding the extra thermal resistance between mounting base and heatsink. For most applications some isolation is used, such as a mica washer. The thermal resistance mounting base to heatsink is then of the order 2 K/W. The total thermal resistance junction to heatsink is therefore

R_{thj-hs} (non isolated type) = R_{thj-mb} + $R_{thmb-hs}$ = 4 K/W

It can be seen that the real performance difference between the isolated and non isolated types will not be significant.

Static Characteristics

The parameters in this section characterise breakdown voltage, threshold voltage, leakage currents and on-resistance.

A drain-source breakdown voltage is specified as greater than the limiting value of drain-source voltage. It can be measured on a curve tracer, with gate terminal shorted to the source terminal, it is the voltage at which a drain current of 250 µA is observed. Gate threshold voltage, $V_{GS(TO)}$, indicates the voltage required on the gate (with

respect to the source) to bring the device into its conducting state. For logic level devices this is usually between 1.0 and 2.0 V and for standard devices between 2.1 and 4 V.

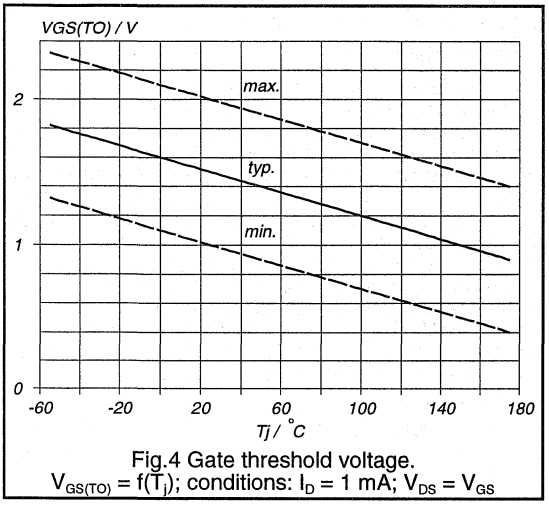


Fig.4 Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

Useful plots in the graphical data are the typical transfer characteristics (Fig.3) showing drain current as a function of V_{GS} and the gate threshold voltage variation with junction temperature (Fig.4). An additional plot also provided is the sub-threshold conduction, showing how the drain current varies with gate-source voltage below the threshold level (Fig.5).

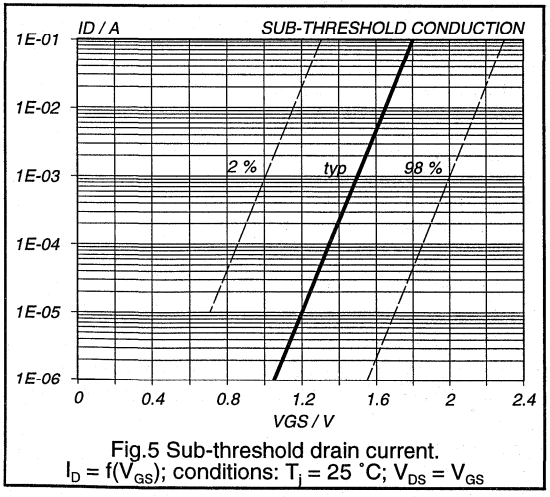


Fig.5 Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

Off-state leakage currents are specified for both the drain-source and gate-source under their respective maximum voltage conditions. Note, although gate-source leakage current is specified in nano-amps, values are typically of the order of a few pico-amps.

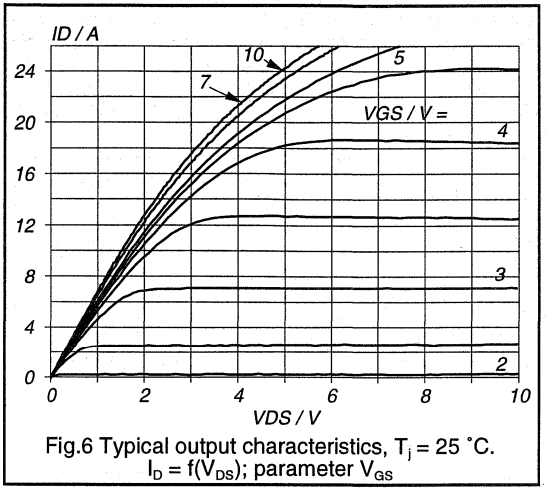


Fig.6 Typical output characteristics, T_j = 25 °C.
$I_D = f(V_{DS})$; parameter V_{GS}

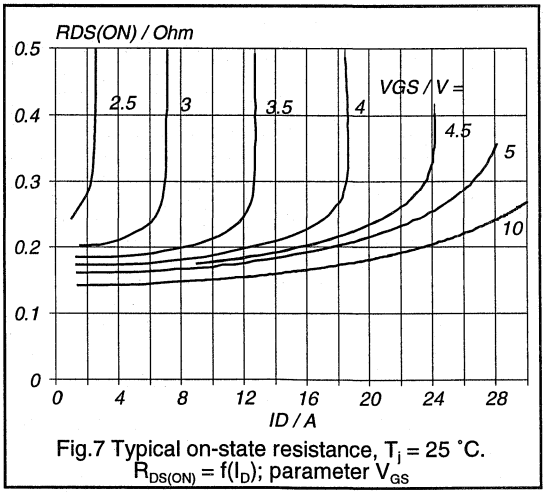


Fig.7 Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

The drain-source on-resistance is very important. It is specified at a gate-source voltage of 5 V for logic level FETs and 10 V for a standard device. The on-resistance for a standard MOSFET cannot be reduced significantly by increasing the gate source voltage above 10 V. Reducing the gate voltage will however increase the on-resistance. For the logic level FET, the on-resistance is given for a gate voltage of 5 V, a further reduction is

possible however at gate voltages up to 10 V, this is demonstrated by the output characteristics, Fig.6 and on-resistance characteristics, Fig.7 for a BUK553-100A.

The on-resistance is a temperature sensitive parameter, between 25 °C and 150 °C it approximately doubles in value. A plot of normalised $R_{DS(ON)}$ versus temperature (Fig.8) is included in each data sheet. Since the MOSFET will normally operate at a T_j higher than 25 °C, when making estimates of power dissipation in the MOSFET, it is important to take into account the higher $R_{DS(ON)}$.

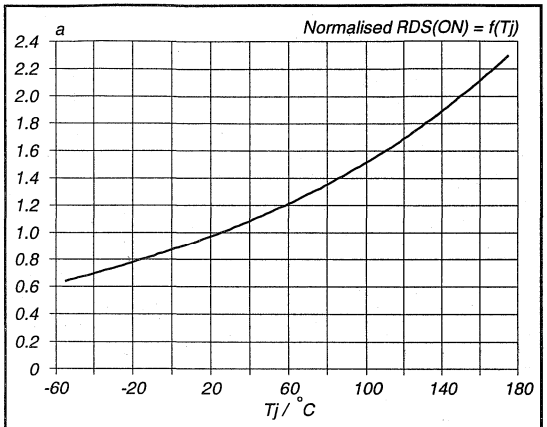


Fig.8 Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 6.5 A; V_{GS} = 5 V

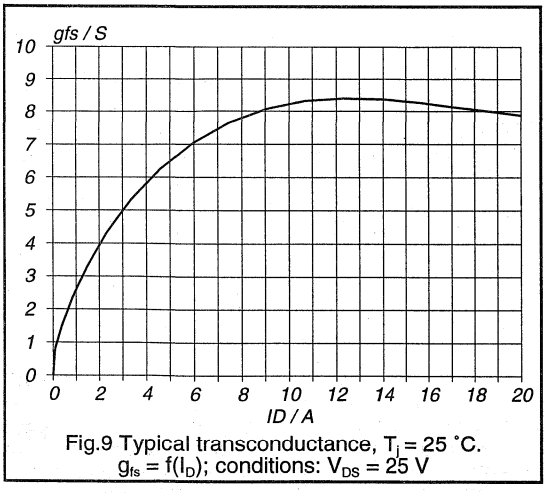


Fig.9 Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

Dynamic Characteristics

These include transconductance, capacitance and switching times. Forward transconductance, g_{fs}, is essentially the gain parameter which indicates the change in drain current that will result from a fluctuation in gate voltage when the device is saturated. (NB saturation of a MOSFET refers to the flat portion of the output characteristics.) Fig.9 shows how g_{fs} varies as a function of the drain current for a BUK553-100A.

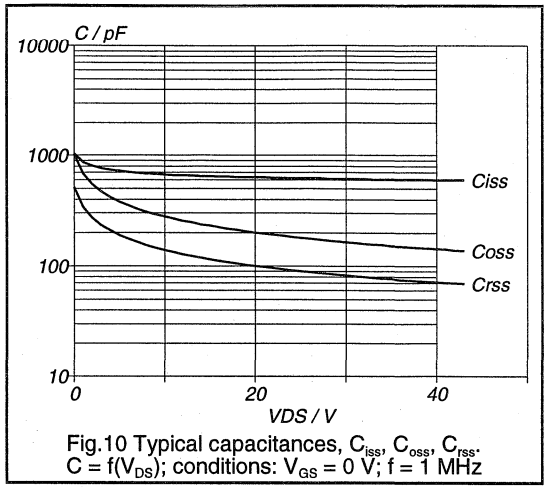


Fig.10 Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

Capacitances are specified by most manufacturers, usually in terms of input, output and feedback capacitance. The values quoted are for a drain-source voltage of 25 V. However this is only part of the story as the MOSFET capacitances are strongly voltage dependent, increasing as drain-source voltage is reduced. Fig.10 shows how these capacitances vary with voltage. The usefulness of the capacitance figures is limited. The input capacitance value gives only a rough indication of the charging required by the drive circuit. Perhaps more useful is the gate charge information an example of which is shown in Fig.11. This plot shows how much charge has to be input to the gate to reach a particular gate-source voltage. Eg. to charge a BUK553-100A to V_{GS} = 5 V, starting from a drain-source voltage of 80 V, requires 12.4 nc. The speed at which this charge is to be applied will give the gate circuit current requirements. More information on MOSFET capacitance is given in chapter 1.2.2.

Resistive load switching times are also quoted by most manufacturers, however extreme care should be taken when making comparisons between different manufacturers data. The speed at which a power MOSFET can be switched is essentially limited only by circuit and package inductances. The actual speed in a circuit is determined by how fast the internal capacitances of the MOSFET are charged and discharged by the drive circuit. The switching times are therefore extremely dependent on the circuit conditions employed; a low gate drive resistance will provide for faster switching and vice-versa. The Philips data sheet presents the switching times for all PowerMOS with a resistor between gate and source of 50 Ω. The device is switched from a pulse

generator with a source impedance also of 50 Ω. The overall impedance of the gate drive circuit is therefore 25 Ω.

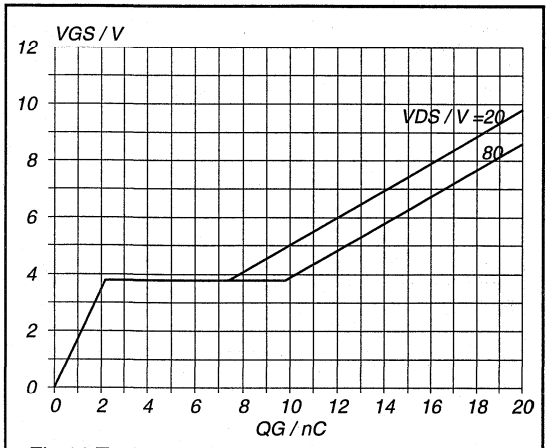


Fig.11 Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 13 A; parameter V_{DS}

Also presented under dynamic characteristics are the typical inductances of the package. These inductances become important when very high switching speeds are employed such that large dI/dt values exist in the circuit. Eg. turning-on 30 A within 60 ns gives a dI/dt of 0.5 A/ns. The typical inductance of the source lead is 7.5 nH, from V = -L*dI/dt the potential drop from the source bond pad (point where the source bond wire connects to the chip internally) to the bottom of the source lead would be 3.75 V. Normally a standard device will be driven with a gate-source voltage of 10 V applied across the gate and source terminals, the actual voltage gate to source on the semiconductor however would only be 6.25 V during the turn-on period! The switching speed is therefore ultimately limited by package inductance.

Reverse diode limiting values and characteristics

The reverse diode is inherent in the vertical structure of the power MOSFET. In some circuits this diode is required to perform a useful function. For this reason the characteristics of the diode are specified. The forward currents permissible in the diode are specified as 'continuous reverse drain current' and 'pulsed reverse drain current'. The forward voltage drop of the diode is also provided together with a plot of the diode characteristic, Fig.12. The switching capability of the diode is given in terms of the reverse recovery parameters, t_{rr} and Q_{rr}.

Because the diode operates as a bipolar device it is subject to charge storage effects. This charge must be removed for the diode to turn-off. The amount of charge stored is given by Q_{rr}, the reverse recovery charge, the

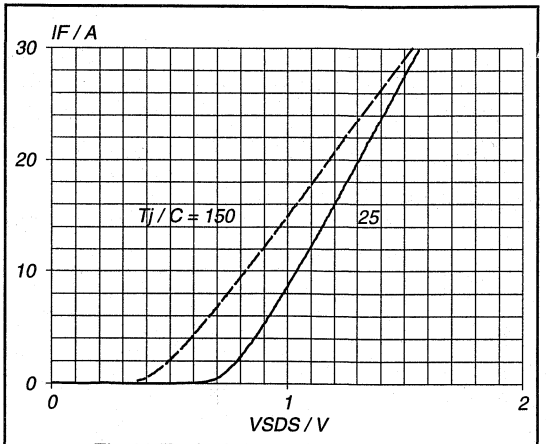


Fig.12 Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} =) V; parameter T_j

time taken to extract the charge is given by t_{rr}, the reverse recovery time. NB. trr depends very much on the $-dI_f/dt$ in the circuit, t_{rr} is specified in data at 100 A/µs.

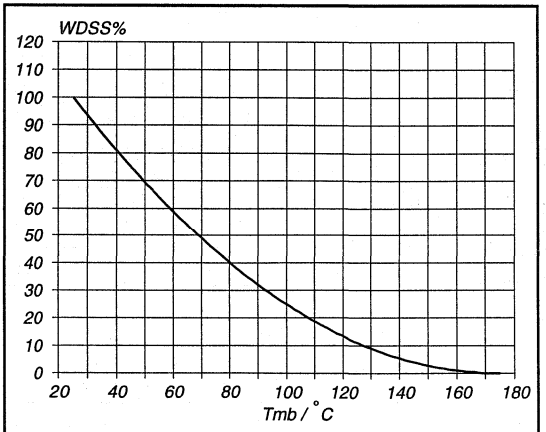


Fig.13. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 13 A

Avalanche limiting value

This parameter is an indication as to the ruggedness of the product in terms of its ability to handle a transient overvoltage, ie the voltage exceeds the drain-source voltage limiting value and causes the device to operate in an avalanche condition. The ruggedness is specified in terms of a drain-source non-repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 °C. This energy level must be derated at higher mounting base temperatures as shown in Fig.13. NB. this rating is non-repetitive which means the circuit should not be designed to force the PowerMOS repeatedly into

avalanche. This rating is only to permit the device to survive if exceptional circuit conditions arise such that a transient overvoltage occurs.

The new generation of Philips Medium Voltage MOSFETs also feature a repetitive ruggedness rating. This rating is specified in terms of a drain-source repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 °C, and indicates that the devices are able to withstand repeated momentary excursions into avalanche breakdown provided the maximum junction temperature is not exceeded.

Safe Operating Area

A plot of the safe operating area is presented for every PowerMOS type. Unlike bipolar transistors a PowerMOS exhibits no second breakdown mechanism. The safe operating area is therefore simply defined from the power dissipation that will cause the junction temperature to reach the maximum permitted value.

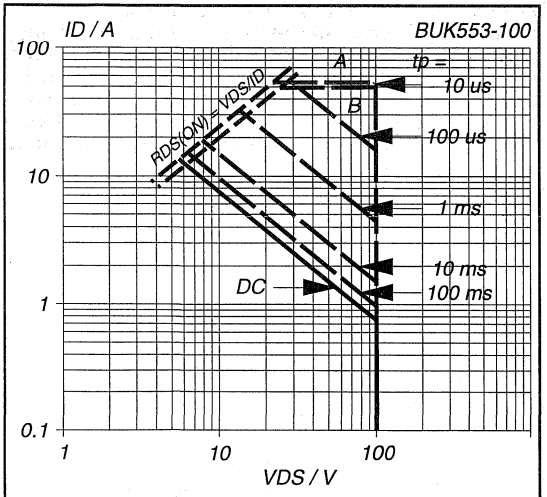


Fig.14 Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

Fig.14 shows the SOA for a BUK553-100. The area is bounded by the limiting drain source voltage, limiting current values and a set of constant power curves for various pulse durations. The plots in data are all for a mounting base temperature of 25 °C. The constant power curves therefore represent the power that raises the junction temperature by an amount T_{jmax} - T_{mb}, ie. 150 °C for a device with a limiting T_j of 175 °C and 125 °C for a device with a limiting T_j of 150 °C. . Clearly in most applications the mounting base temperature will be higher than 25 °C, the SOA would therefore need to be reduced. The maximum power curves are calculated very simply. The dc curve is based upon the thermal resistance junction to mounting base (junction to heatsink in the case of isolated packages), which is substituted into equation 1. The curves for pulsed operation assume a single shot pulse and instead of thermal resistance, a value for transient thermal impedance is used. Transient thermal impedance is supplied as graphical data for each type, an example is shown in Fig.15. For calculation of the single shot power dissipation capability, a value at the required pulse width is read from the D = 0 curve and substituted in to equation 2. (A more detailed explanation of transient thermal impedance and how to use the curves can be found in chapter 7.)

$$P_{tot(dc)} = \frac{T_{jmax} - T_{mb}}{R_{thj-mb}} \quad 1$$

$$P_{tot(pulse)} = \frac{T_{jmax} - T_{mb}}{Z_{thj-mb}} \quad 2$$

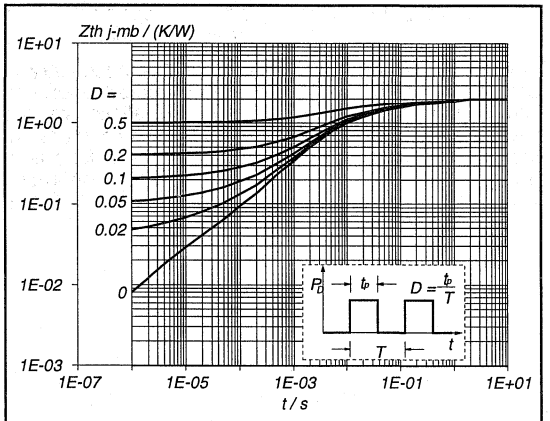


Fig.15 Transient thermal impedance.
Z_{thj-mb} = f(t); parameter D = t_p/T

Examples of how to calculate the maximum power dissipation for a 1 ms pulse are shown below. Example 1 calculates the maximum power assuming a T_j of 175 °C and T_{mb} of 25 °C. This power equates to the 1 ms curve on the SOA plot of Fig.14. Example 2 illustrates how the power capability is reduced if T_{mb} is greater than 25 °C.

Example 1: 1 ms pulse at 25 °C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 °C, T_{mb} = 25 °C

$$P_{max(1\,ms\,pulse)} = \frac{175 - 25}{0.32} = 469\,W$$

The 469 W line is observed on Fig.13, (4.69 A @ 100 V and 15.6 A @ 30 V etc)

Example 2: 1 ms pulse at 75 °C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 °C, T_{mb} = 75 °C

$$P_{max(1\,ms\,pulse)} = \frac{175 - 75}{0.32} = 312\,W$$

Therefore with a mounting base temperature of 75 °C the maximum permissible power dissipation is reduced by one third compared with the 25 °C value on the SOA plot.

Calculating Currents

The current ratings quoted in the data sheet are derived directly from the maximum power dissipation.

$$I_D(@T_{mb})^2 \cdot R_{DS(ON)}(@T_{jmax}) = P_{tot} \qquad 3$$

substituting for P_{tot} from equation 1

$$I_D(@T_{mb}) = \left\{ \frac{T_{jmax} - T_{mb}}{R_{thj-mb} \cdot R_{DS(ON)}(@T_{jmax})} \right\}^{\frac{1}{2}} \qquad 4$$

To calculate a more realistic current it is necessary to replace T_{jmax} in equation 4 with the desired operating junction temperature and T_{mb} with a realistic working value. It is generally recommended that devices are not operated continuously at T_{jmax}. For reasons of long term reliability, 125 °C is a more suitable junction operating temperature. A value of T_{mb} between 75 °C and 110 °C is also a more typical figure.

As an example a BUK553-100A is quoted as having a dc current rating of 13 A. Assuming a T_{mb} of 100 °C and operating T_j of 125 °C the device current is calculated as follows:

From Fig.8

$$R_{DS(ON)}(@\,125^oC) = 1.75 \cdot R_{DS(ON)}(@\,25^oC) = 1.75 \cdot 0.18 = 0.315\Omega$$

$R_{thj\text{-}mb}$ = 2 K/W, using equation 4

$$I_D = \left\{ \frac{25}{2 \cdot 0.315} \right\}^{\frac{1}{2}} = 6.3A$$

The device could therefore conduct 6.3 A under these conditions which equates to a 12.5 W power dissipation.

Conclusions

The most important information presented in the data sheet is the on-resistance and the maximum voltage drain-source. Current values and maximum power dissipation values should be viewed carefully since they are only achievable if the mounting base temperature is held to 25 °C. Switching times are applicable only for the specific conditions described in the data sheet, when making comparisons between devices from different manufacturers, particular attention should be paid to these conditions.

DEVICE DATA

in alphanumeric sequence

PowerMOS transistor Logic level TOPFET

BUK100-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		13.5	A
P_D	Total power dissipation		40	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		125	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

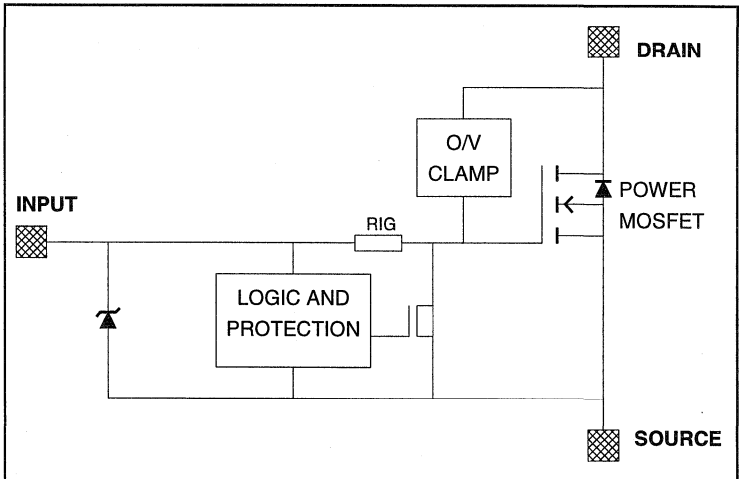
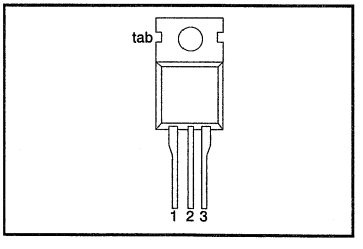


Fig.1. Elements of the TOPFET.

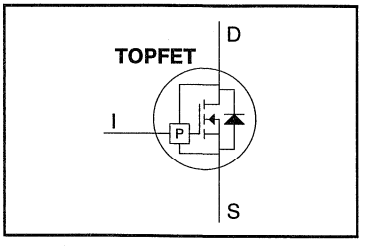
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	24	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 15$ A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	25	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	60	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	8	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	40	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	40	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	35	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	15	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

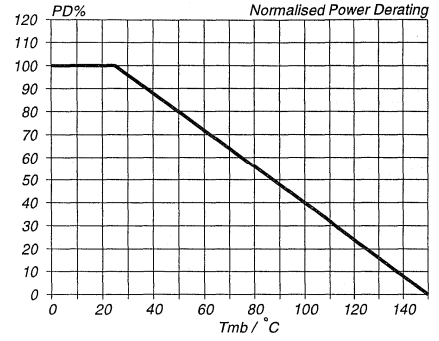


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

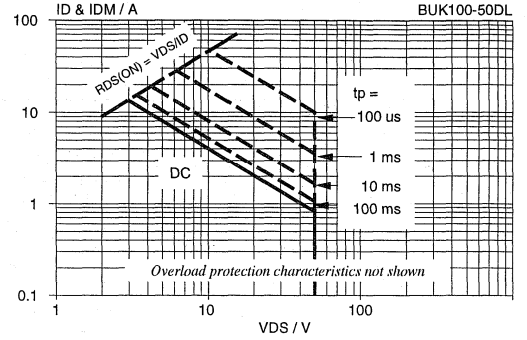


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

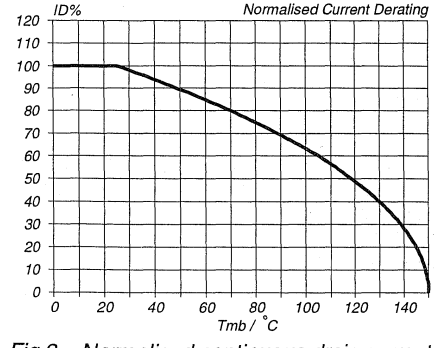


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: V_{IS} = 5 V

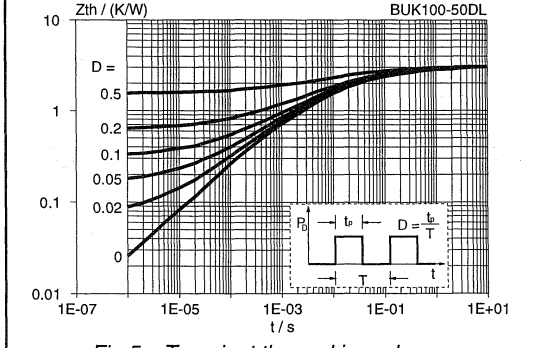


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

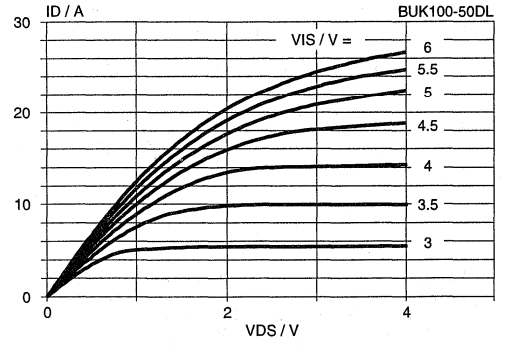


Fig.6. Typical on-state characteristics, T_j = 25 ˚C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

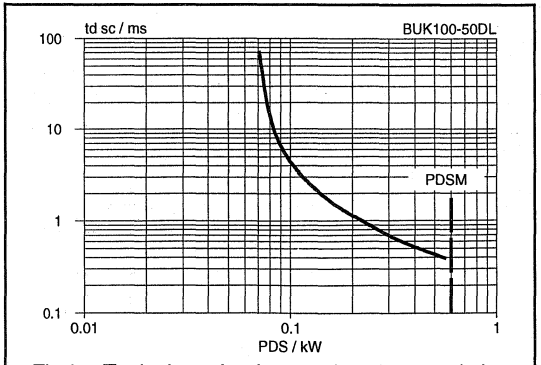


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq$ 4 V; T_j = 25 ˚C.

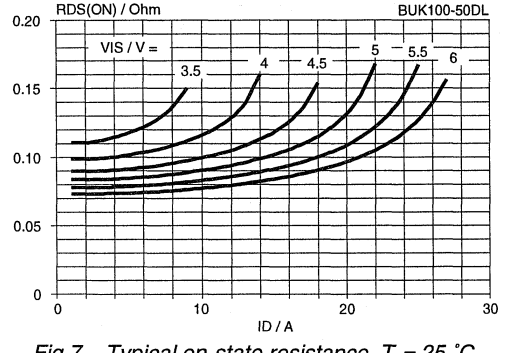


Fig.7. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

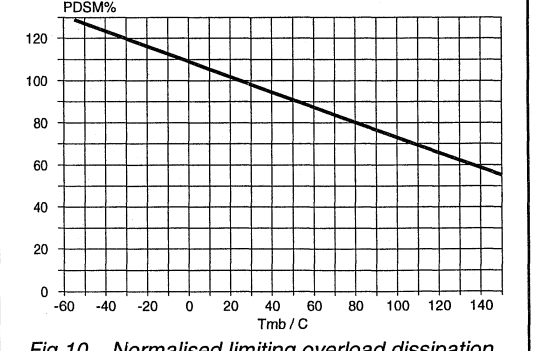


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 ˚C) = f(T_{mb})

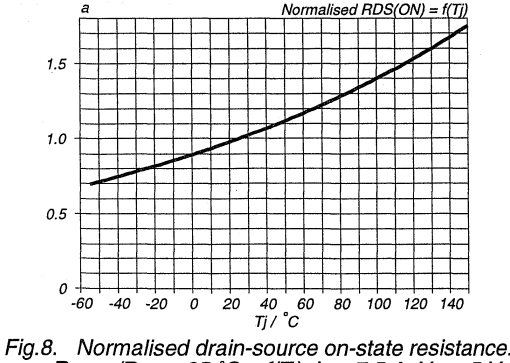


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 ˚C = f(T_j); I_D = 7.5 A; V_{IS} = 5 V

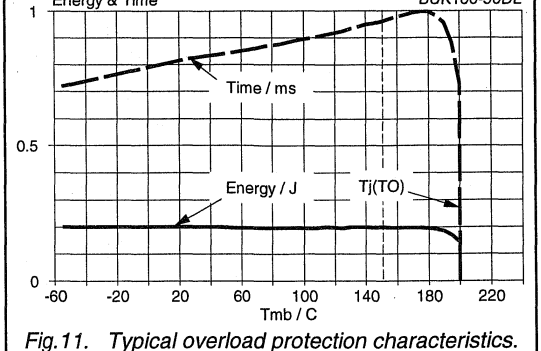


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

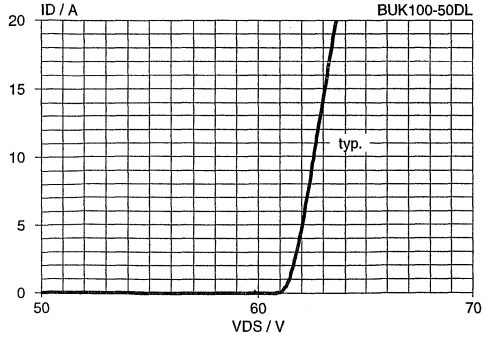


Fig.12. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

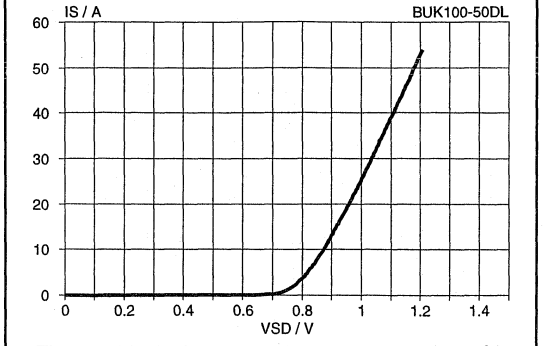


Fig.15. Typical reverse diode current, $T_j = 25$ ˚C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V; $t_p = 250$ µs

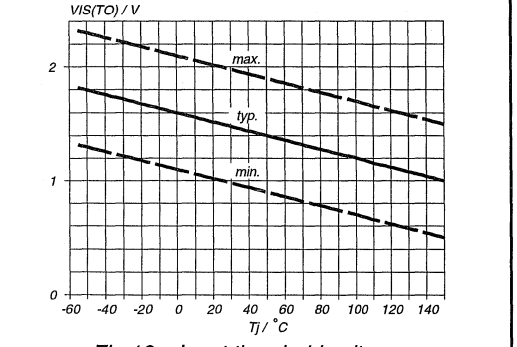


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

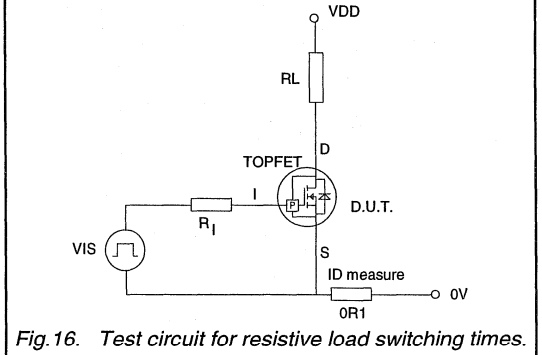


Fig.16. Test circuit for resistive load switching times.

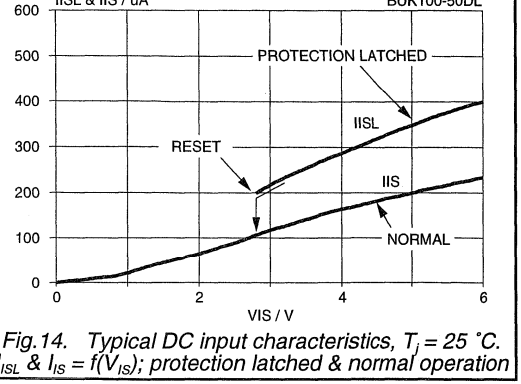


Fig.14. Typical DC input characteristics, $T_j = 25$ ˚C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

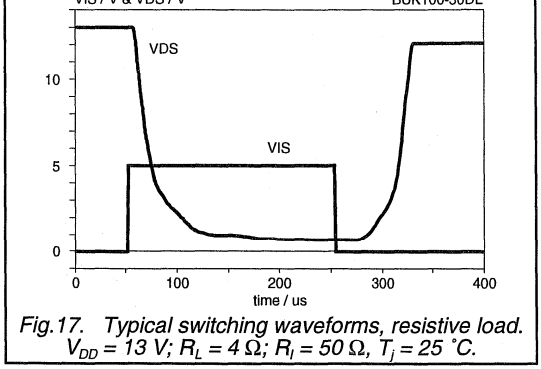


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 4\ \Omega$; $R_I = 50\ \Omega$, $T_j = 25$ ˚C.

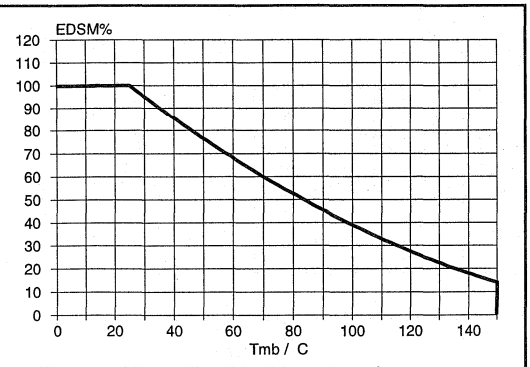


Fig.18. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

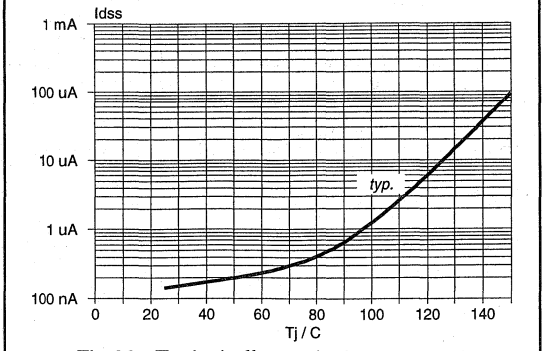


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

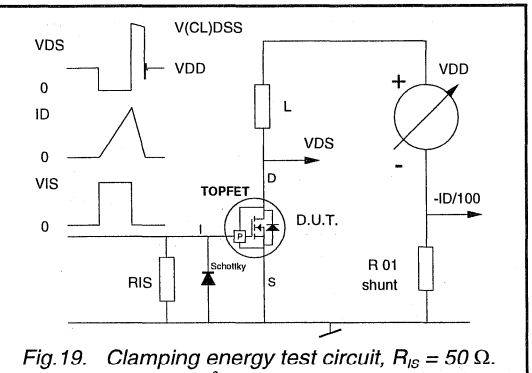


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

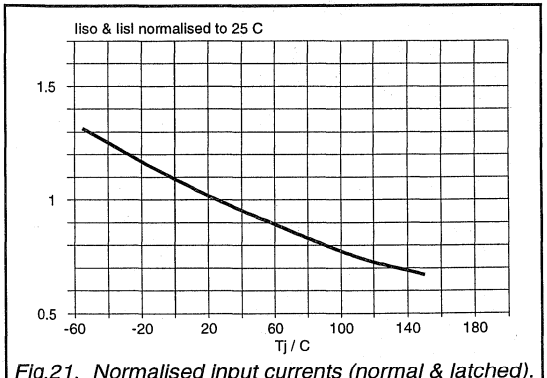


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25°C$ & $I_{ISL}/I_{ISL}25°C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK100-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	13.5	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	125	mΩ

FUNCTIONAL BLOCK DIAGRAM

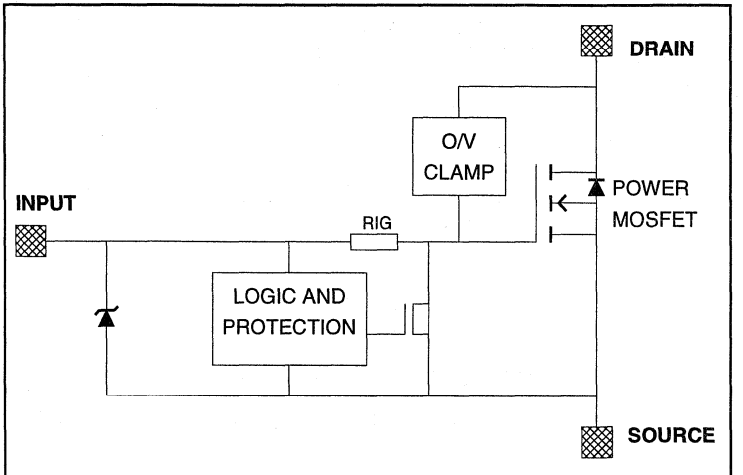
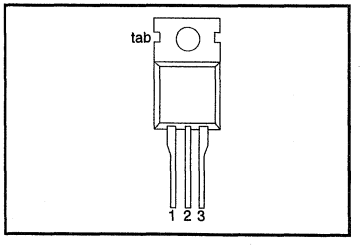


Fig.1. Elements of the TOPFET.

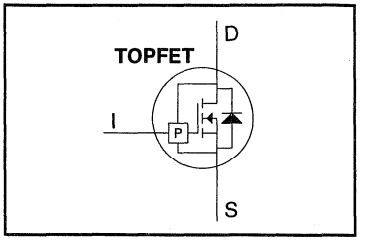
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \le 300$ µs; $\delta \le 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \le 300$ µs; $\delta \le 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \ge 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq$ 300 µs; $\delta \leq$ 0.01	5	9	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	25	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	6	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	4.5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	13.5	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

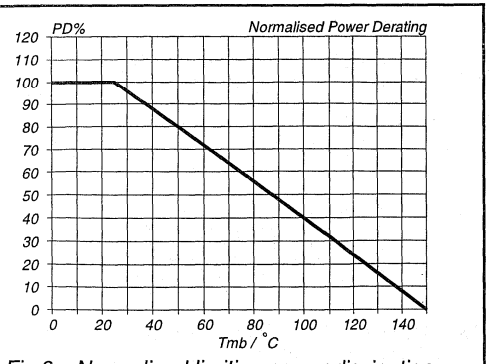


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

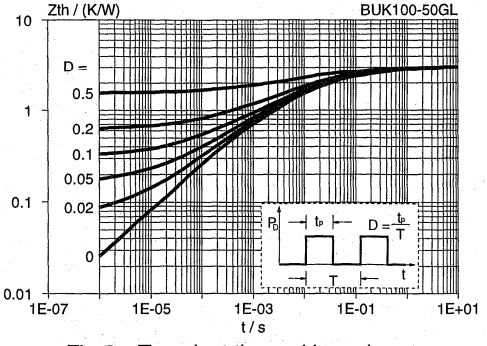


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

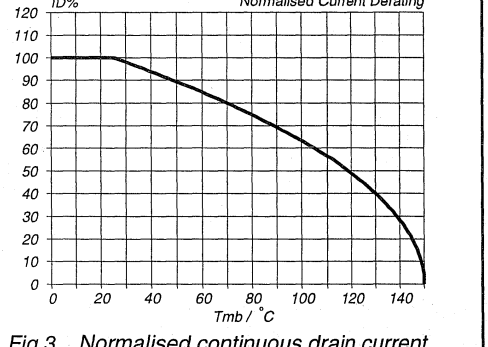


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

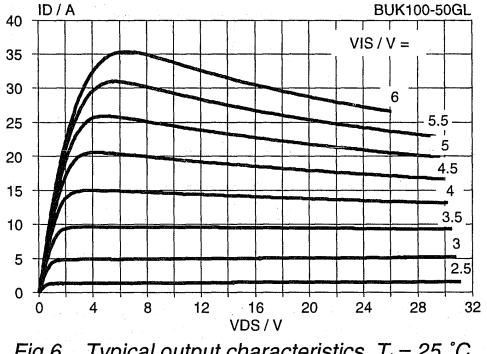


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

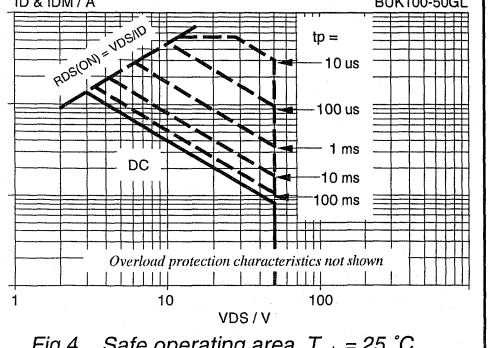


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

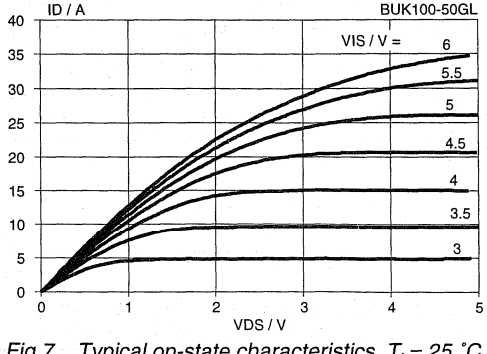


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

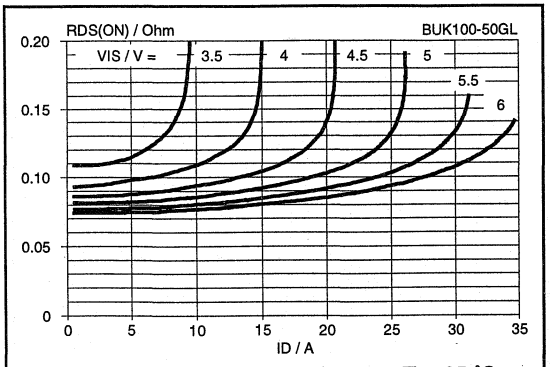


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

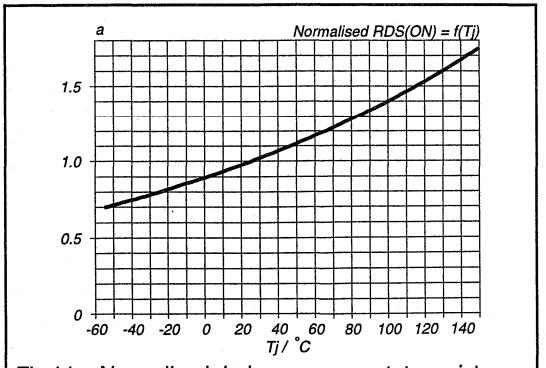


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 7.5 A; V_{IS} = 5 V

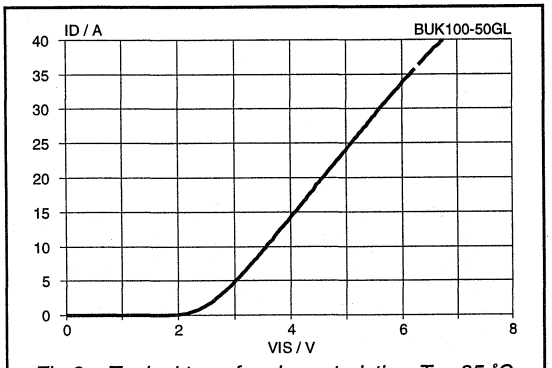


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

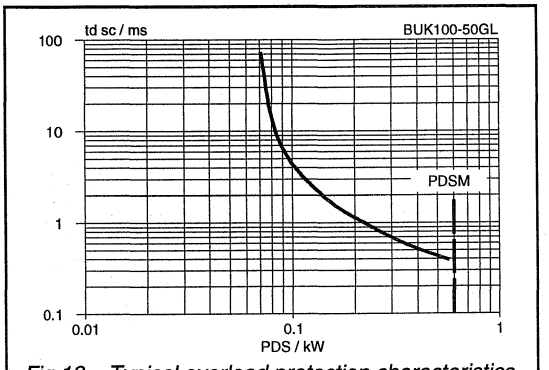


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 °C.

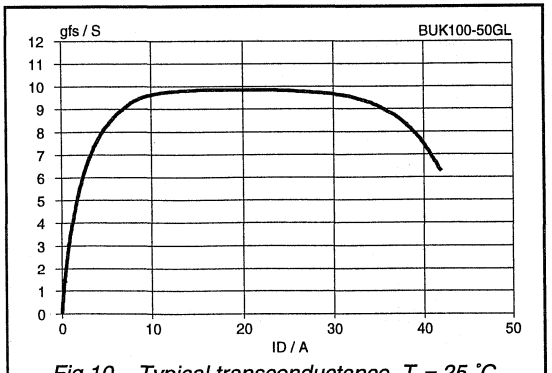


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

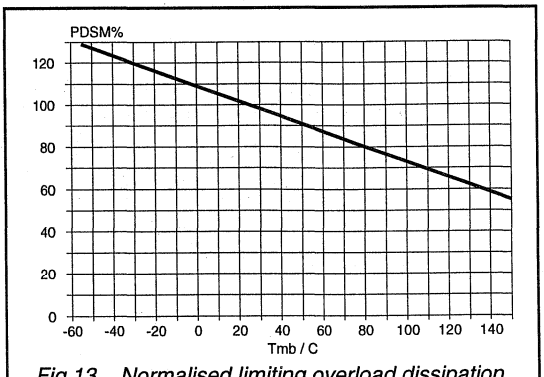


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

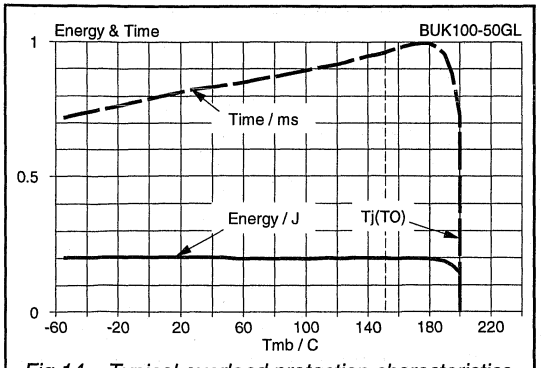


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

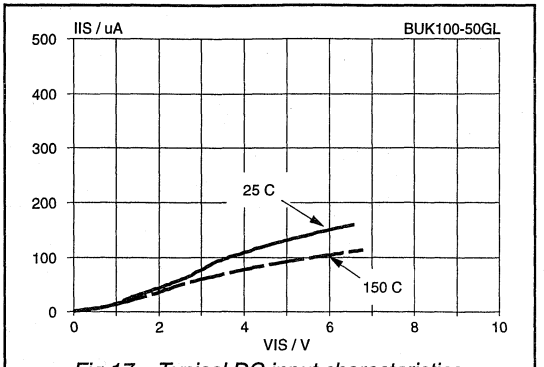


Fig.17. Typical DC input characteristics. $I_{IS} = f(V_{IS})$; normal operation, parameter: T_j

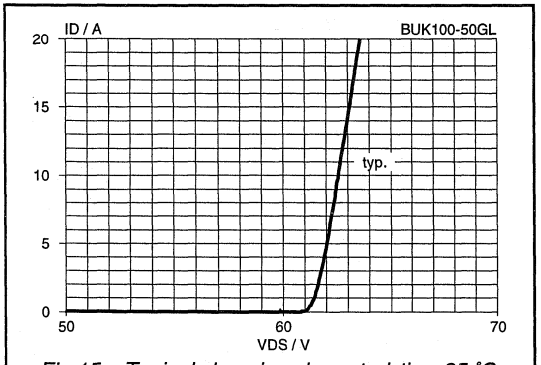


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

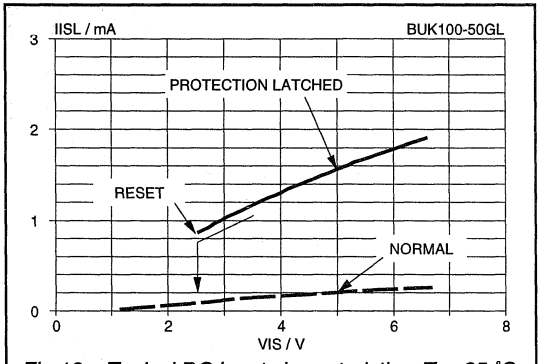


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

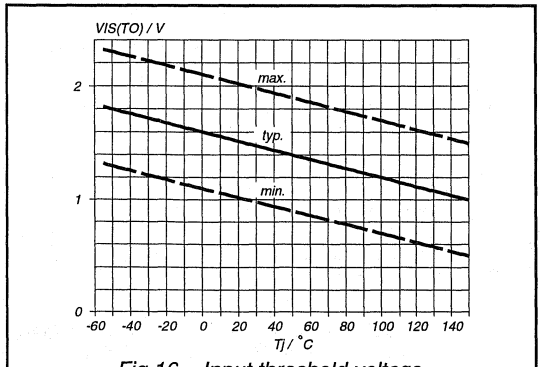


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

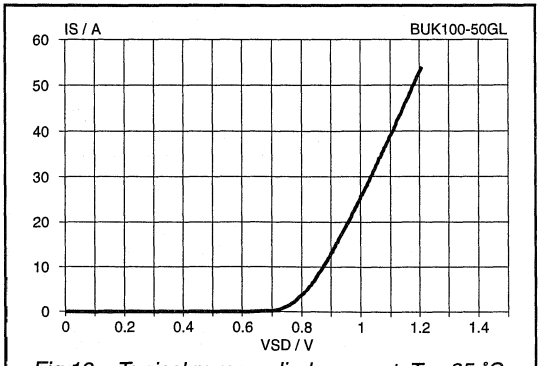


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

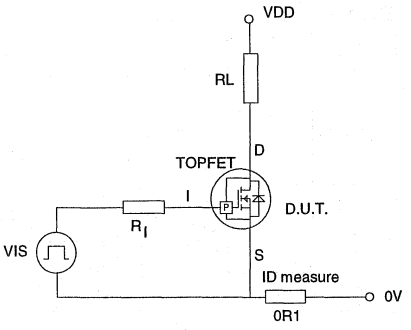


Fig.20. Test circuit for resistive load switching times.

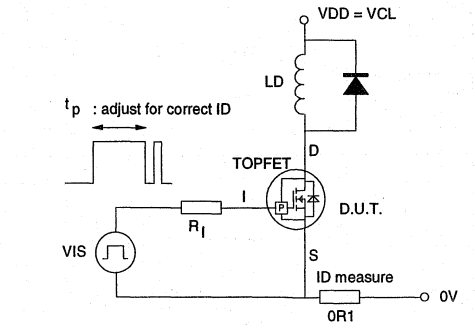


Fig.23. Test circuit for inductive load switching times.

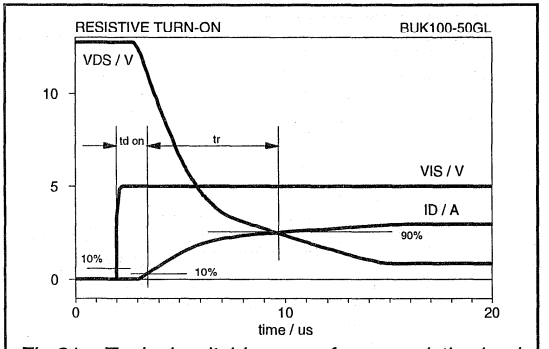


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

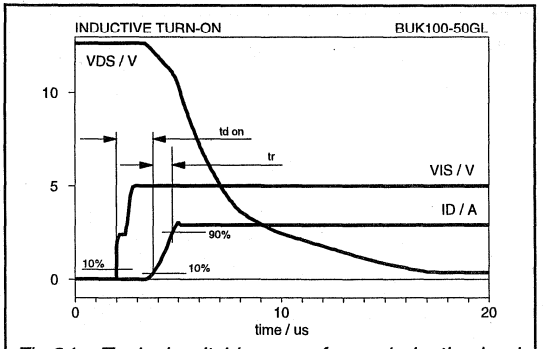


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

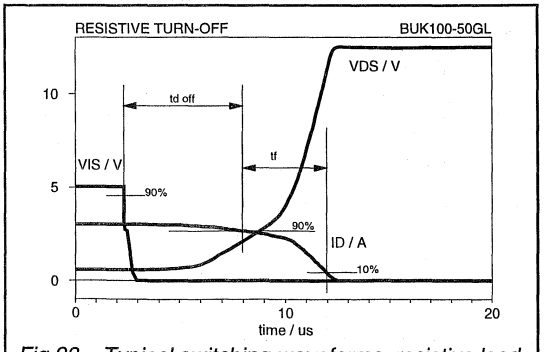


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

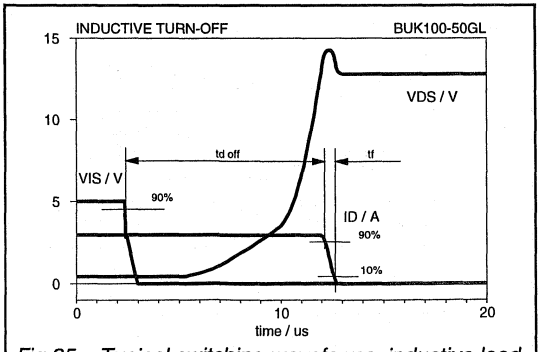


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

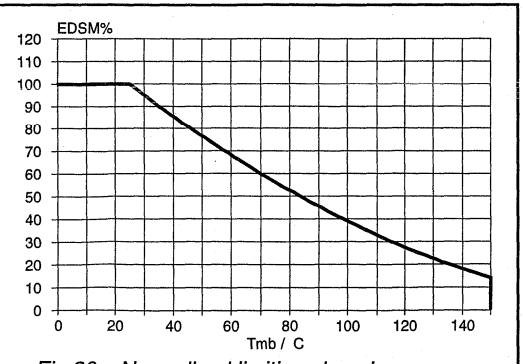


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

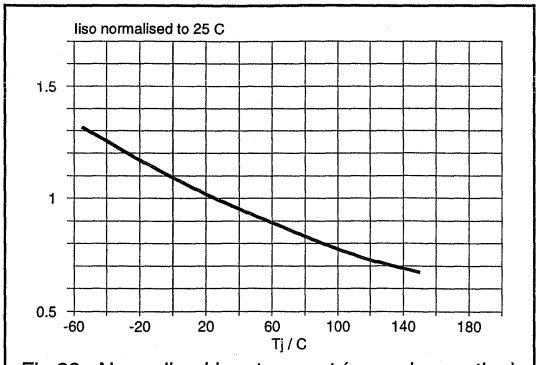


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

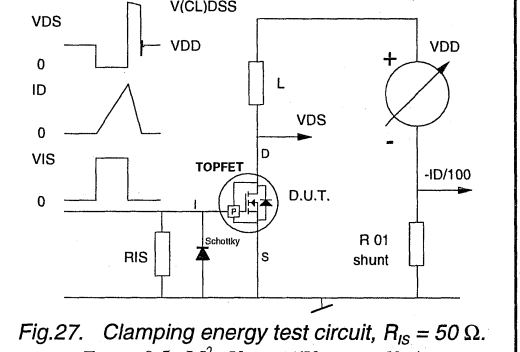


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

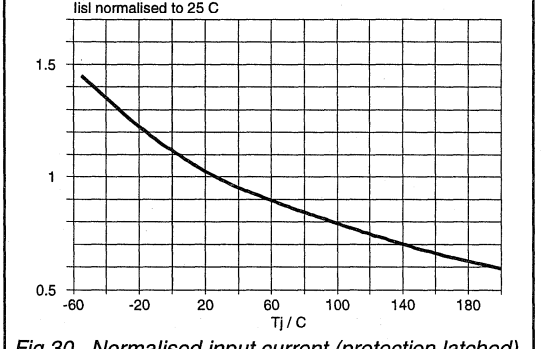


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

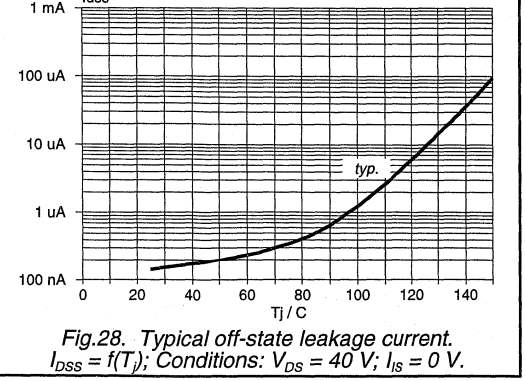


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK100-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	100	mΩ

FUNCTIONAL BLOCK DIAGRAM

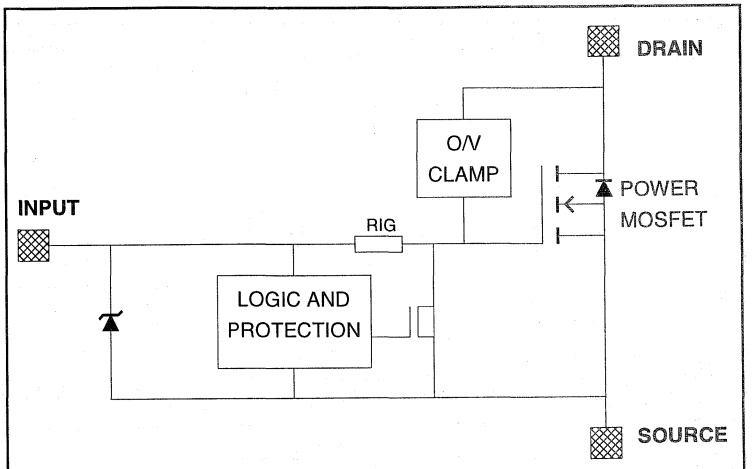
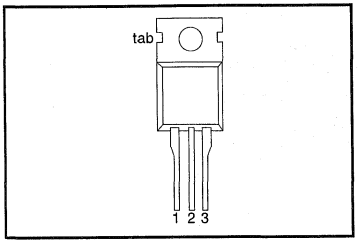


Fig.1. Elements of the TOPFET.

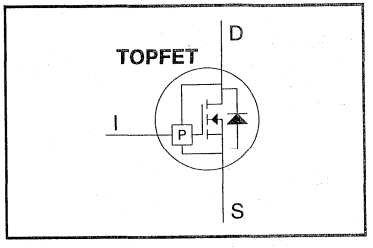
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	15	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	9.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	60	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	20	V
		V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \le 300$ µs; $\delta \le 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 7.5 A; $t_p \le 300$ µs; $\delta \le 0.01$	V_{IS} = 10 V	-	65	100	mΩ
			V_{IS} = 5 V	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \ge 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	1.0	2.5	5.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 10 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	0.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	15	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

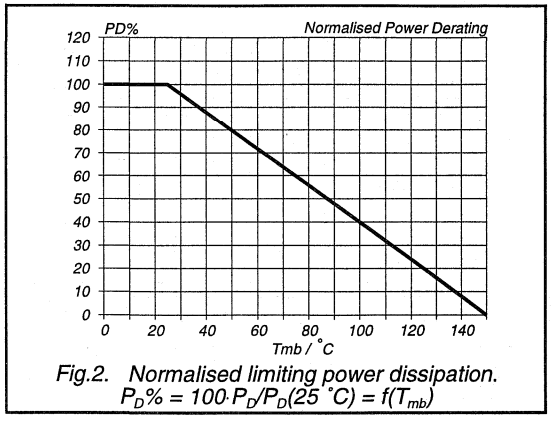


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

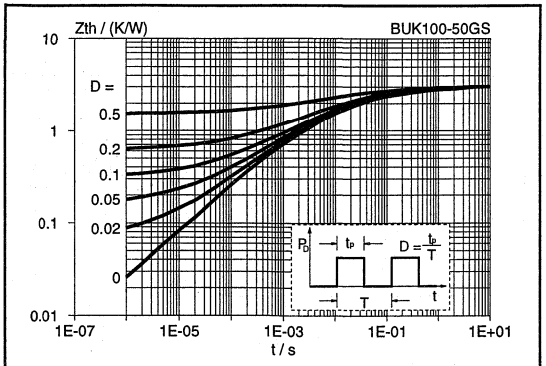


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

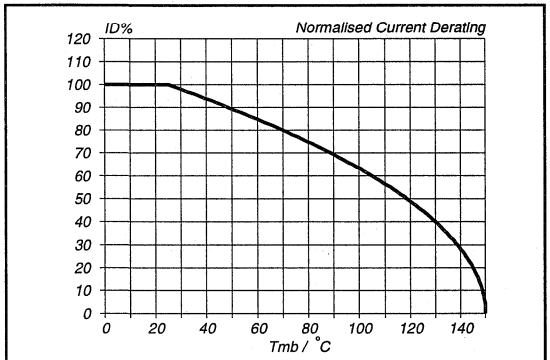


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

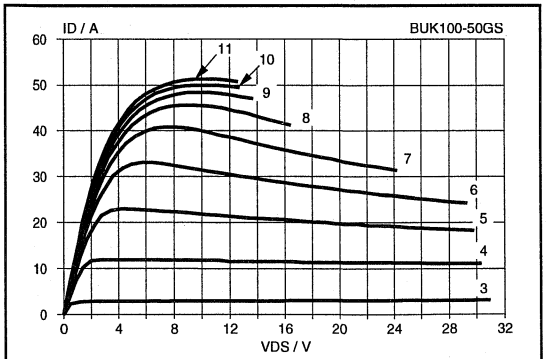


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

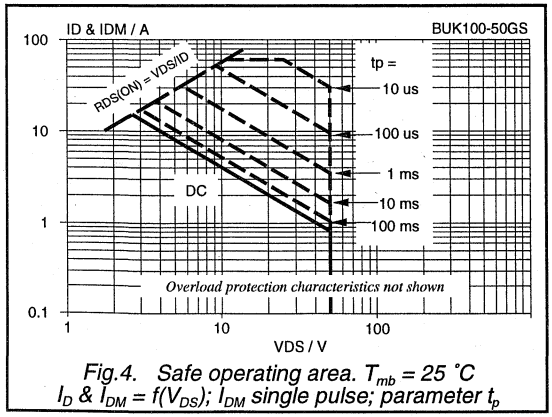


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

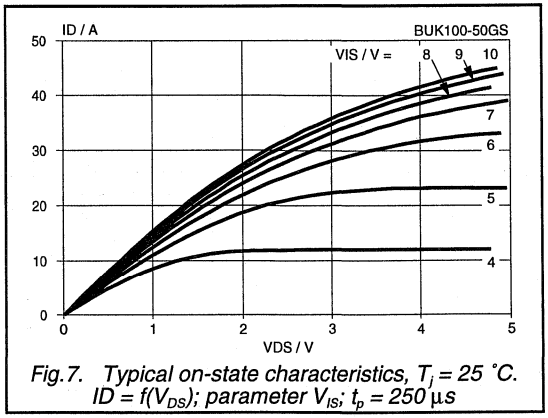


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

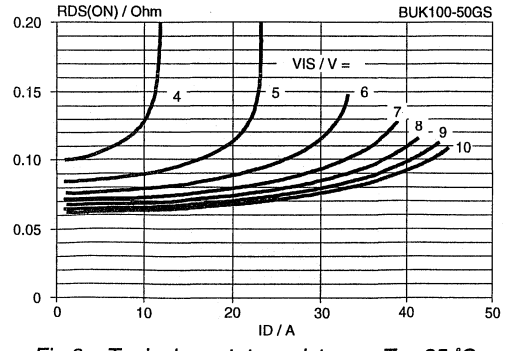


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

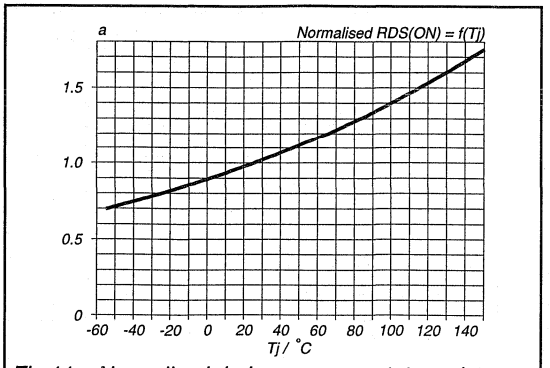


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 7.5 A; V_{IS} = 5 V

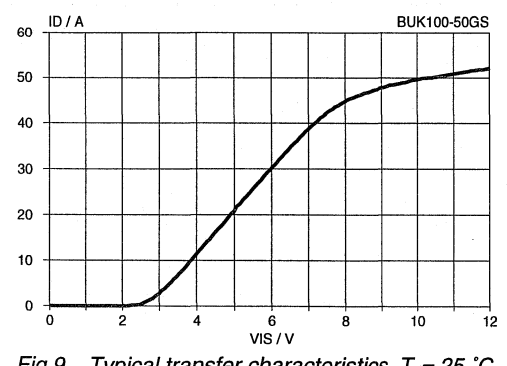


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

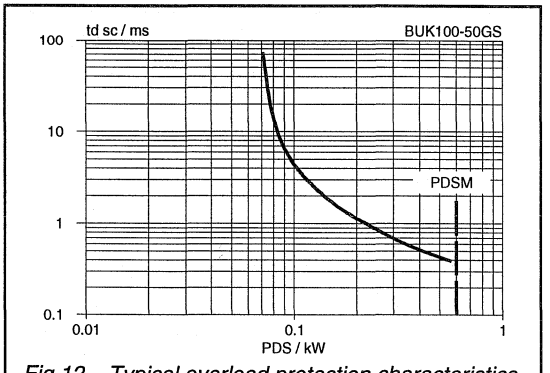


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 5$ V; T_j = 25 °C.

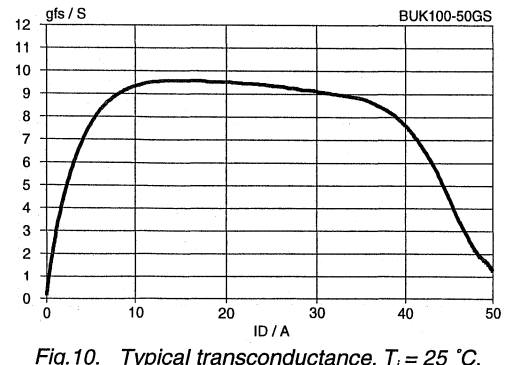


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

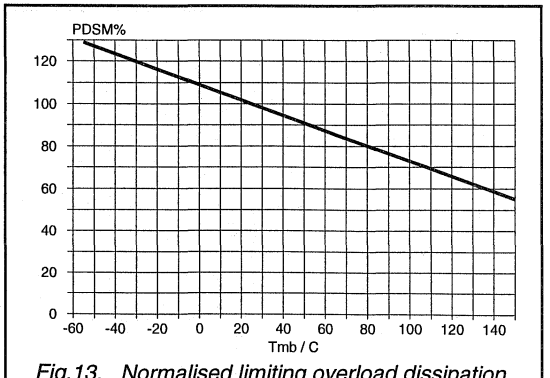


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

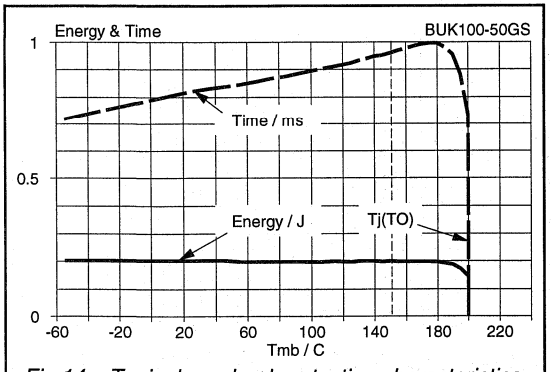


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 10 V; SC load = 30 mΩ

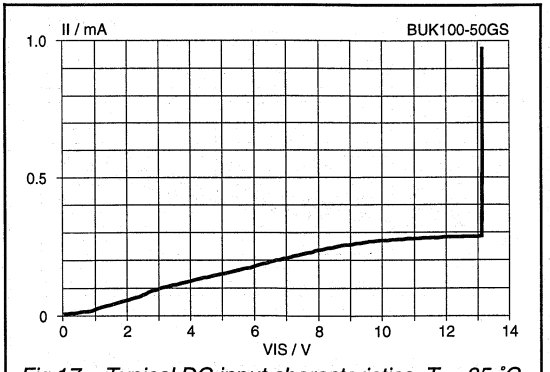


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

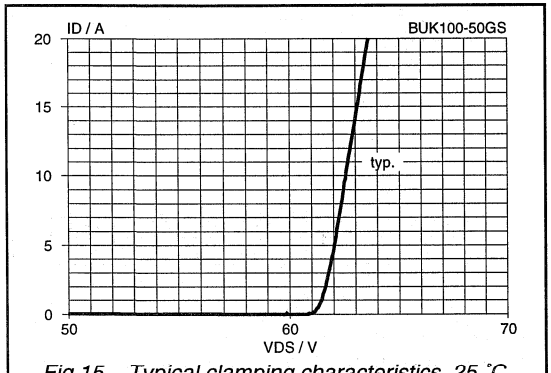


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

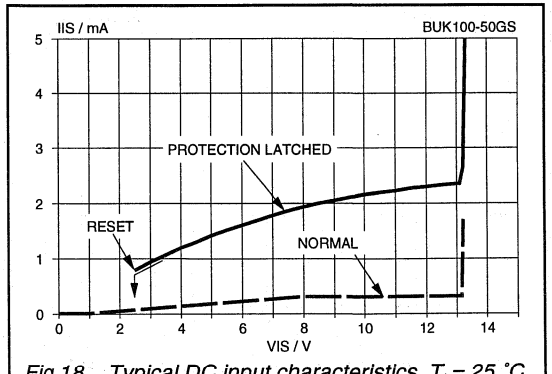


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

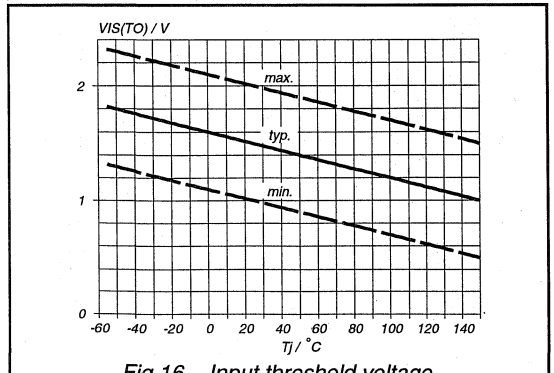


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

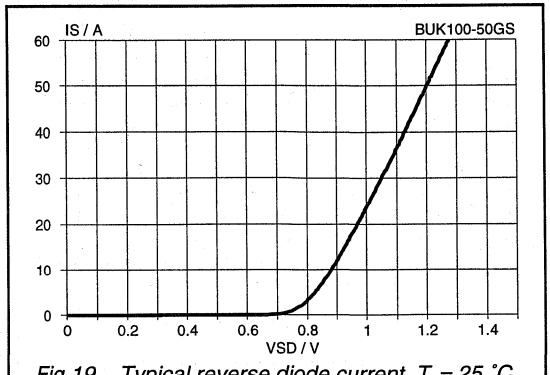


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

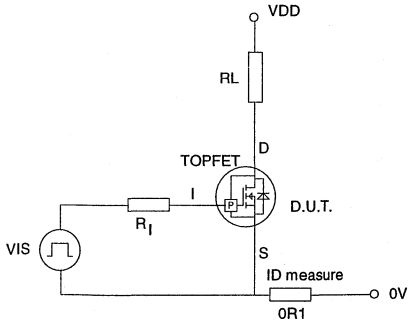


Fig.20. Test circuit for resistive load switching times.

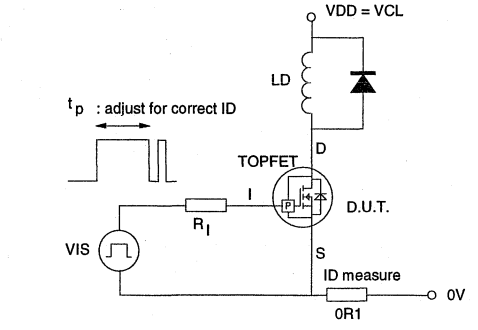


Fig.23. Test circuit for inductive load switching times.

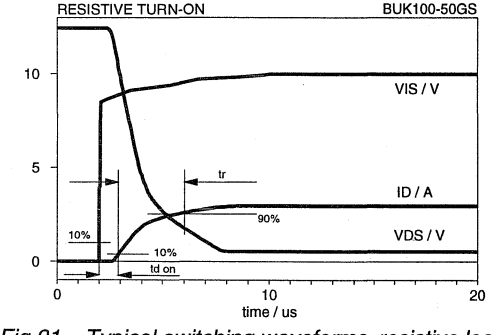


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

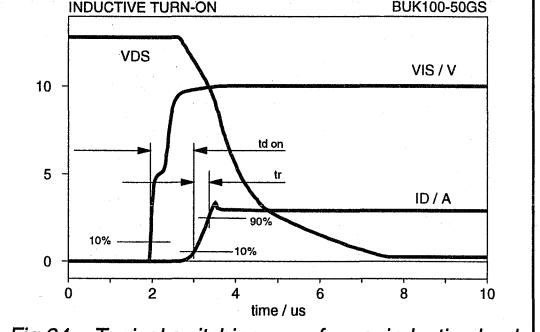


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

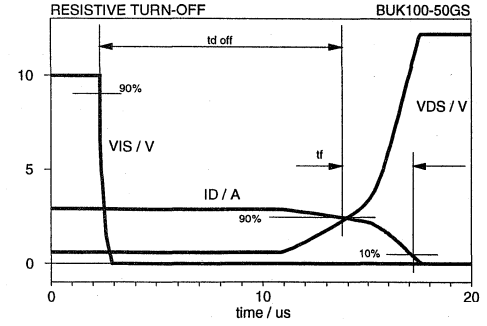


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

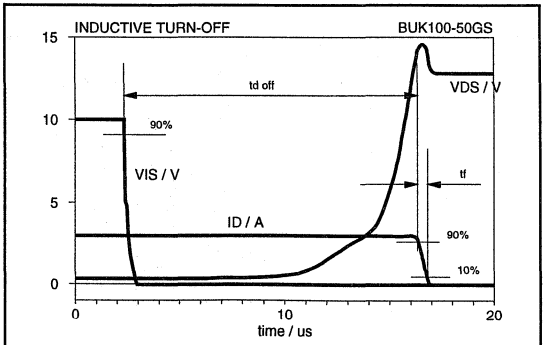


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

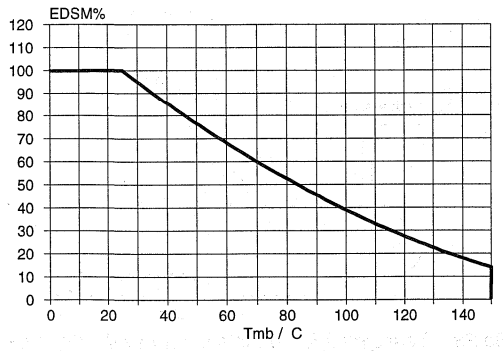


Fig.26. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 15 A; V_{IS} = 10 V

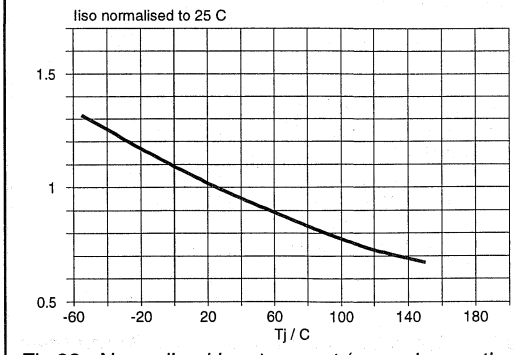


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

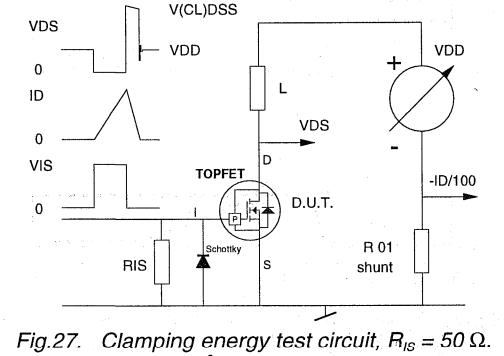


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

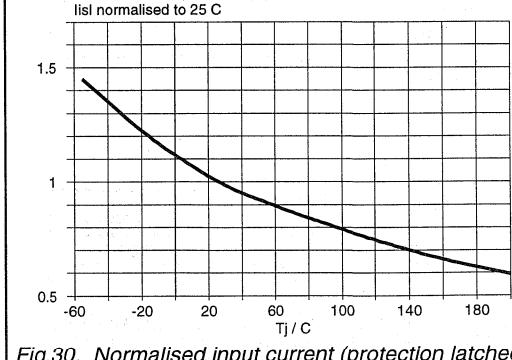


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

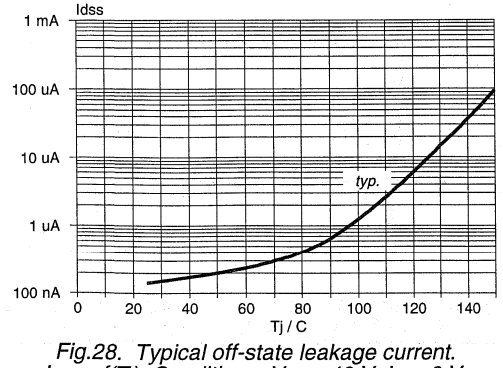


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

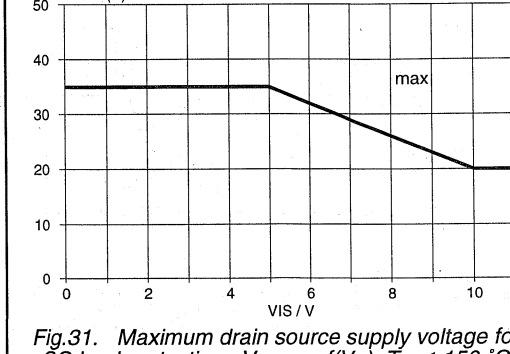


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^{\circ}C$

PowerMOS transistor Logic level TOPFET

BUK101-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		26	A
P_D	Total power dissipation		75	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		60	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	μA

FUNCTIONAL BLOCK DIAGRAM

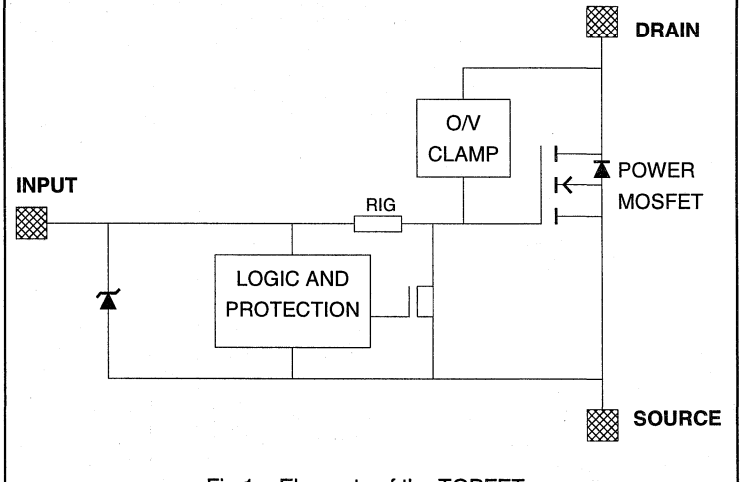
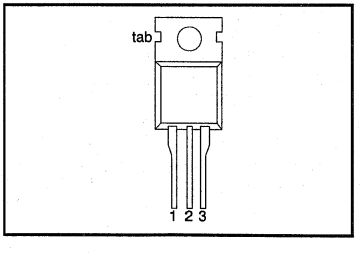


Fig.1. Elements of the TOPFET.

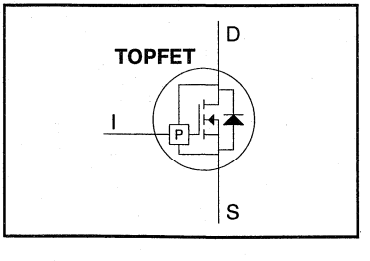
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	20	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 26$ A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	45	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	105	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω . Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	17	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	75	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	60	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	70	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

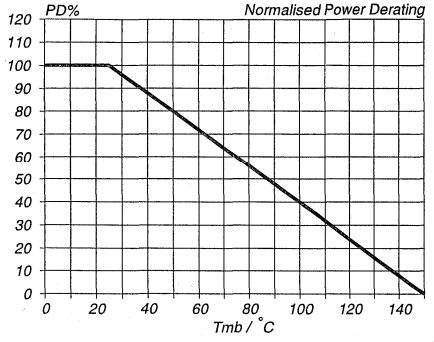


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

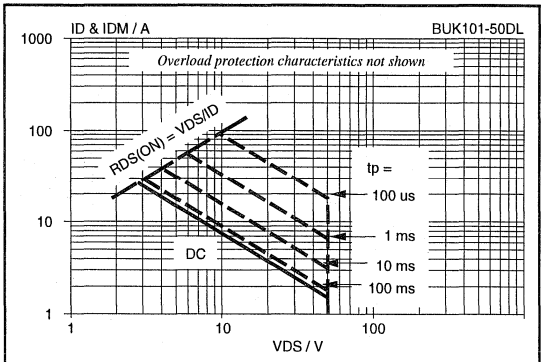


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

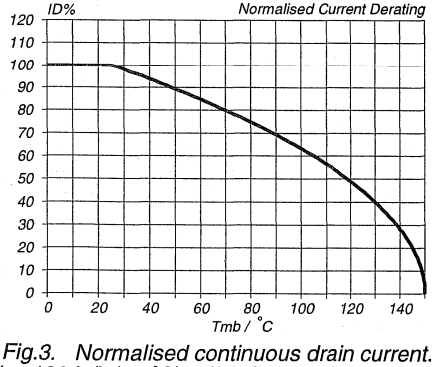


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: V_{IS} = 5 V

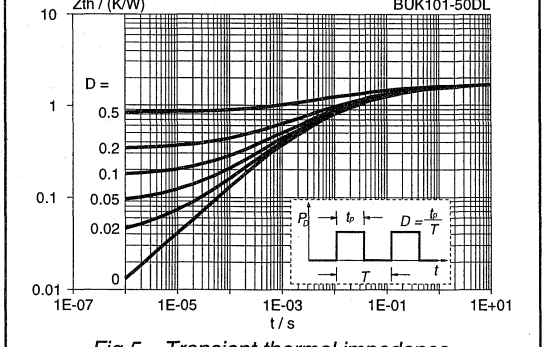


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

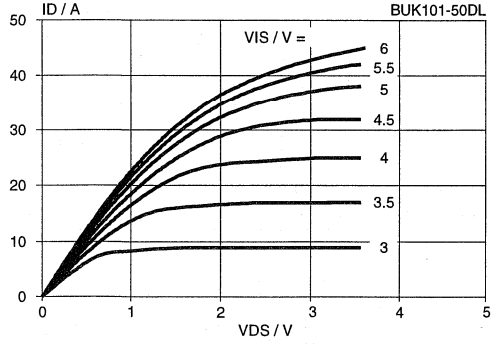


Fig.6. Typical on-state characteristics, T_j = 25 ˚C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

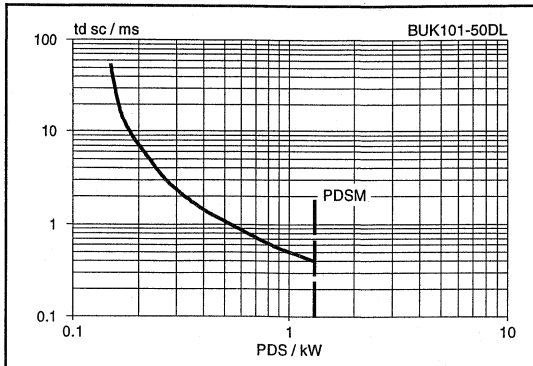


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

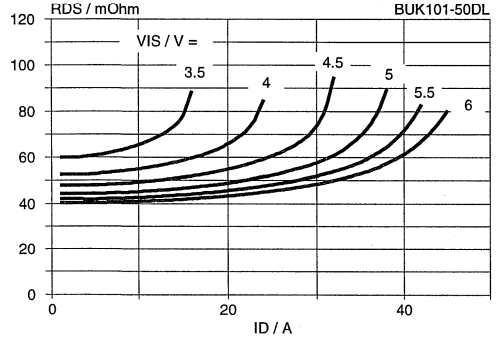


Fig.7. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

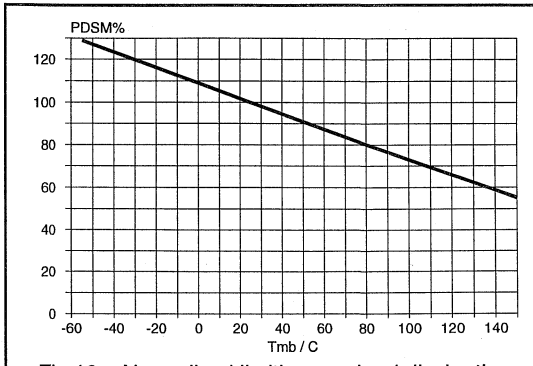


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 ˚C) = f(T_{mb})

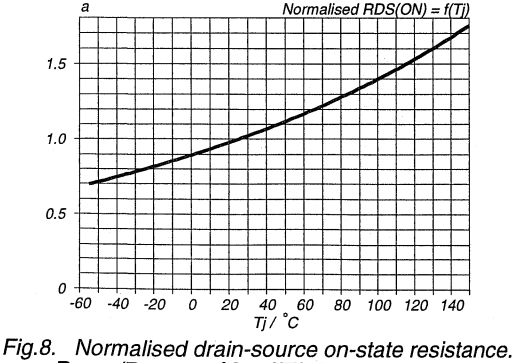


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 ˚C = f(T_j); I_D = 13 A; V_{IS} = 5 V

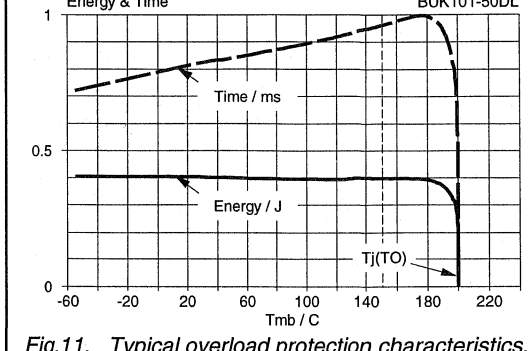


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

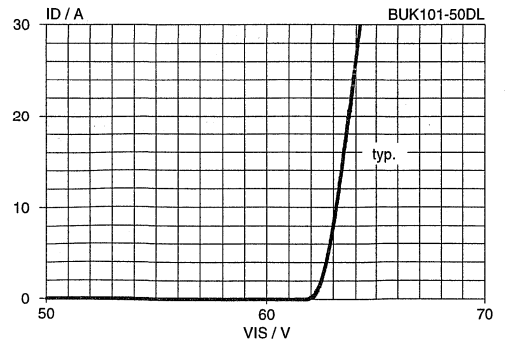


Fig.12. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

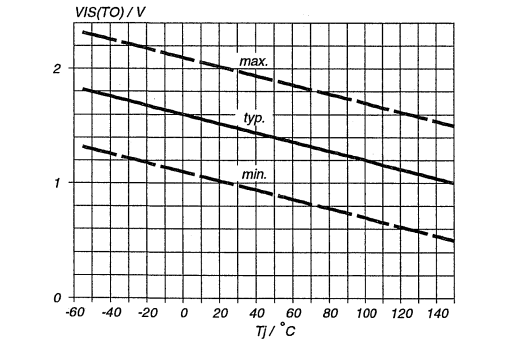


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

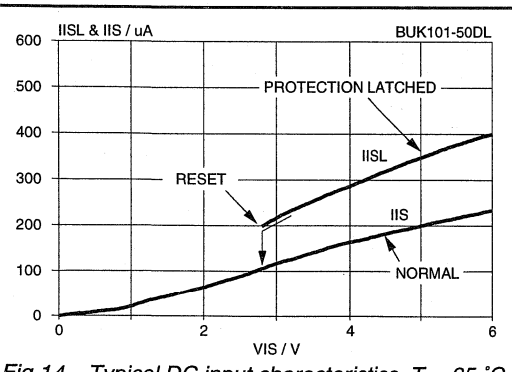


Fig.14. Typical DC input characteristics, $T_j = 25$ ˚C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

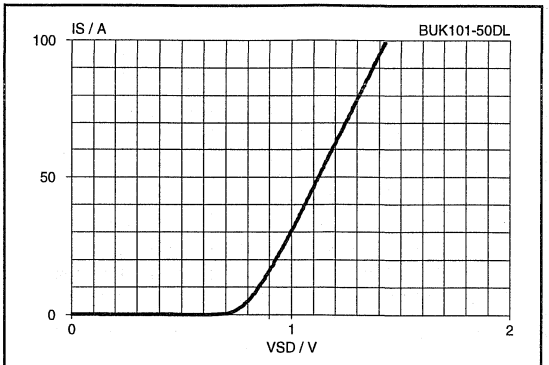


Fig.15. Typical reverse diode current, $T_j = 25$ ˚C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V

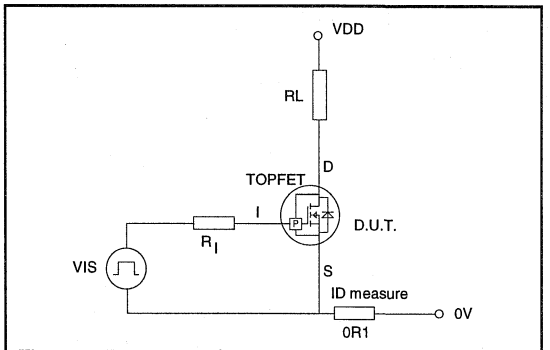


Fig.16. Test circuit for resistive load switching times.

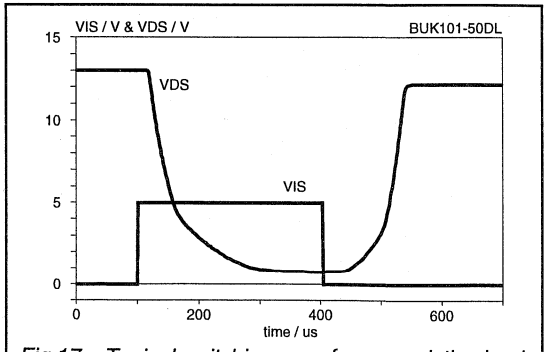


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 2.1$ Ω; $R_I = 50$ Ω, $T_j = 25$ ˚C.

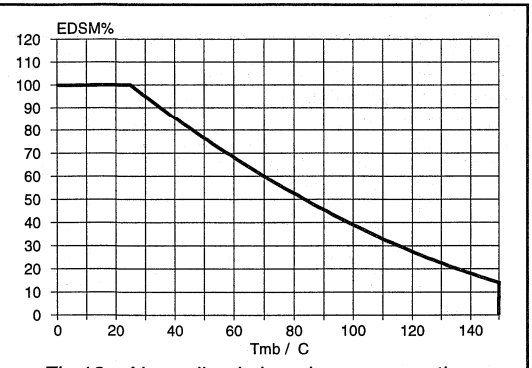


Fig.18. Normalised clamping energy rating. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 26 A; V_{IS} = 5 V

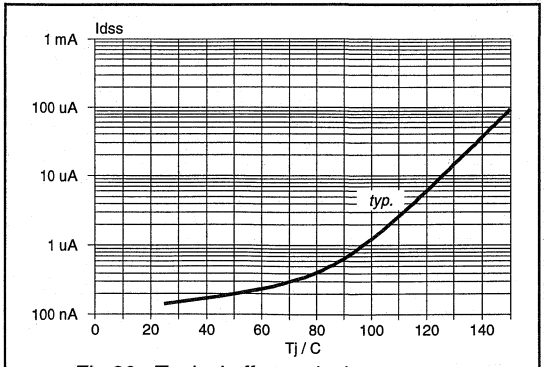


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

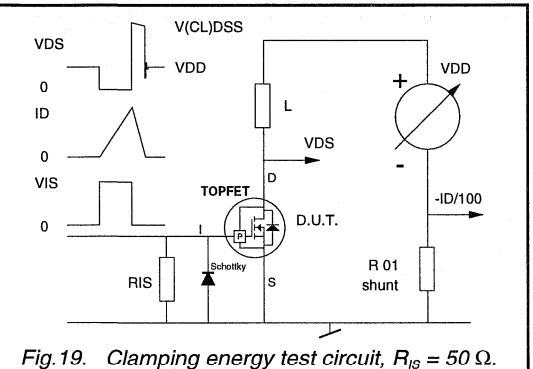


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

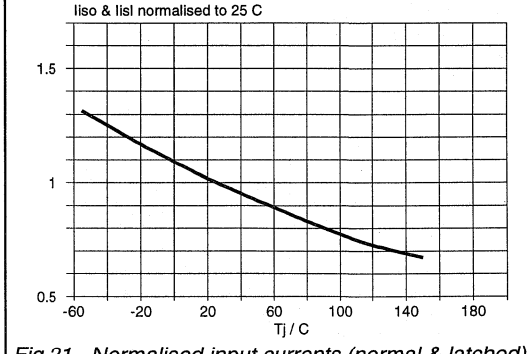


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK101-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	26	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	60	mΩ

FUNCTIONAL BLOCK DIAGRAM

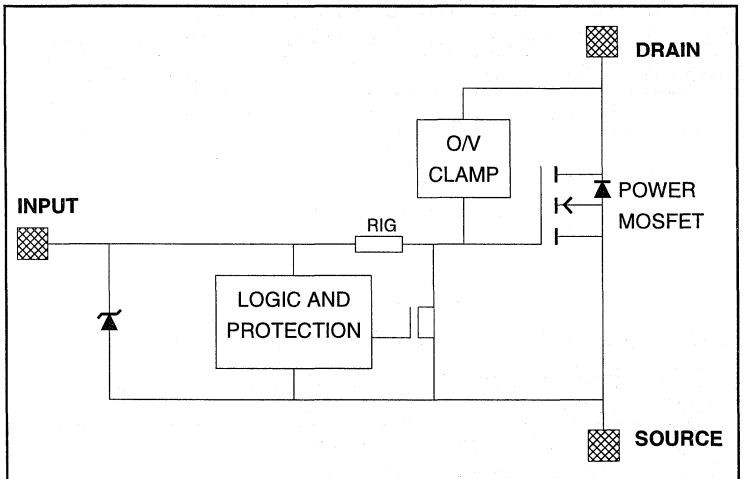
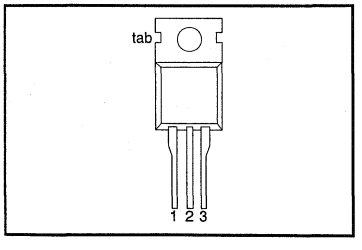


Fig.1. Elements of the TOPFET.

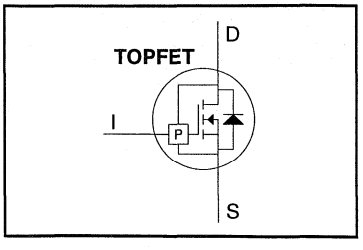
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[1]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[2]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[3]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 26 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

2 The input voltage for which the overload protection circuits are functional.

3 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	7	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	15	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	7	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

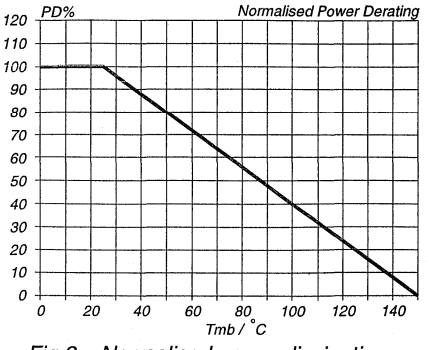


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

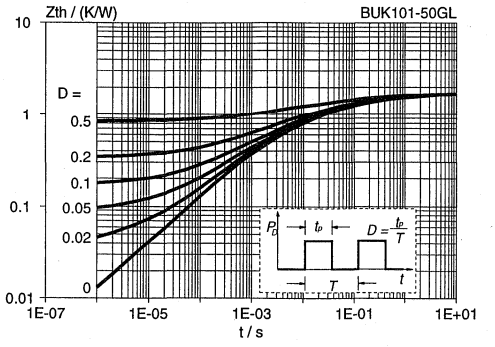


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

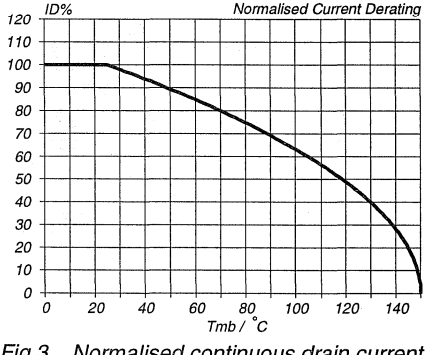


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

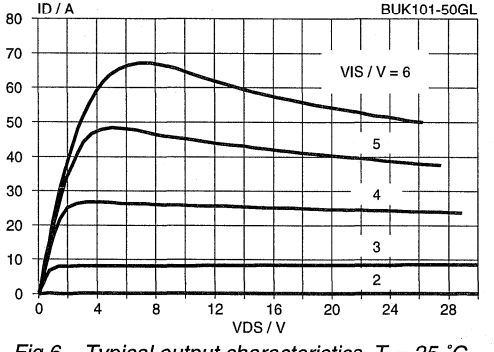


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

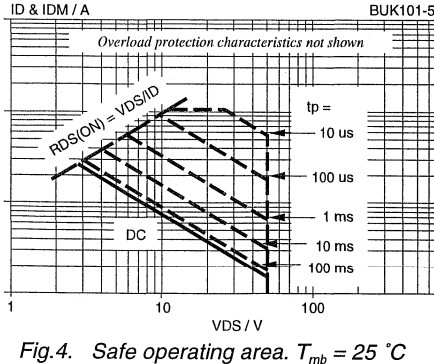


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

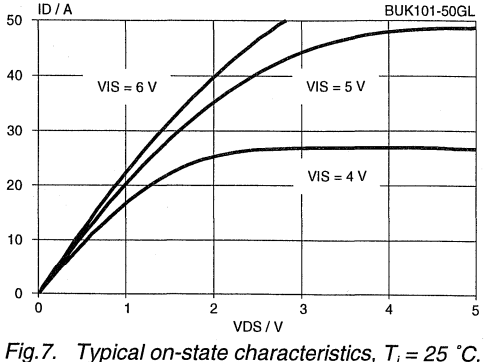


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

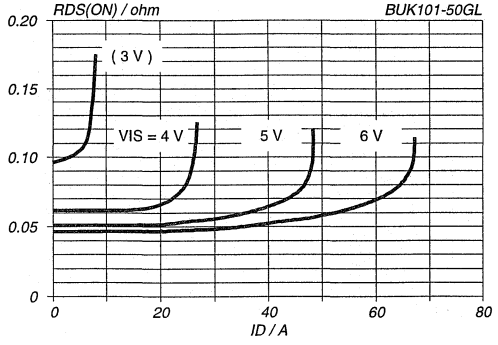


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

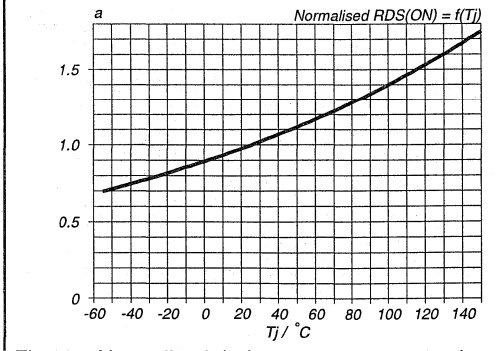


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C $= f(T_j)$; I_D = 13 A; V_{IS} = 5 V

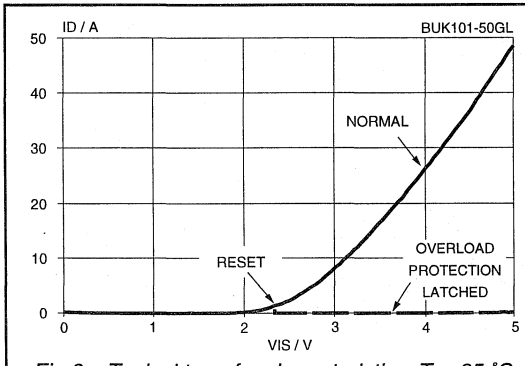


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

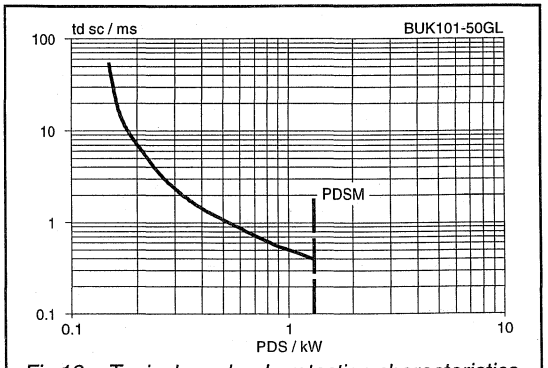


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

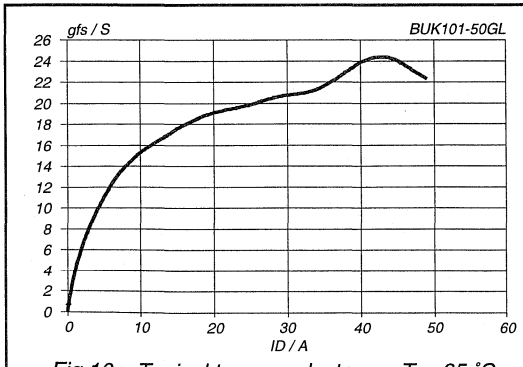


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

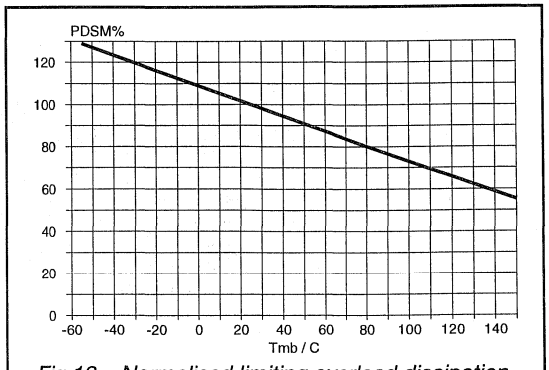


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

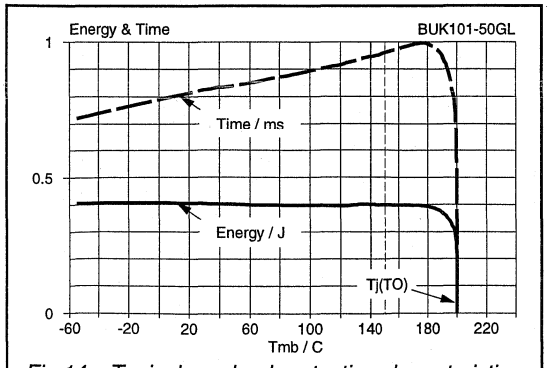


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

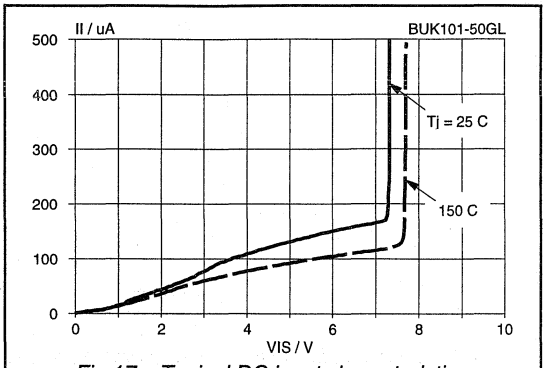


Fig.17. Typical DC input characteristics. $I_I = f(V_{IS})$; normal operation; parameter: T_j

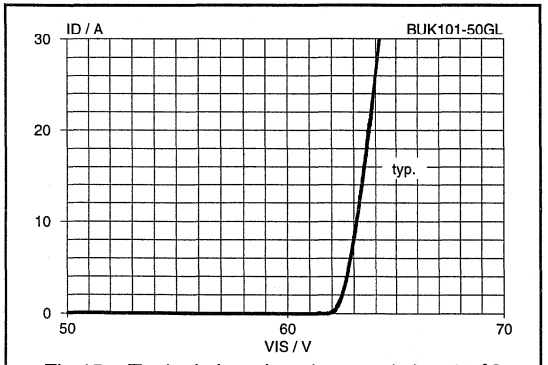


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

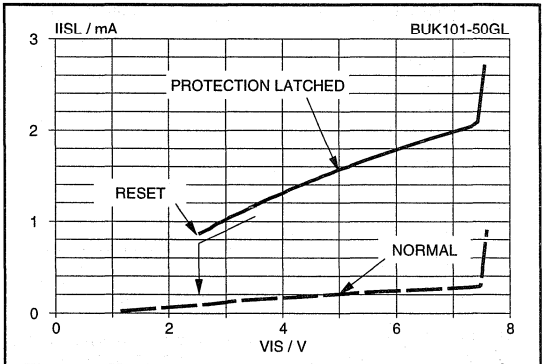


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

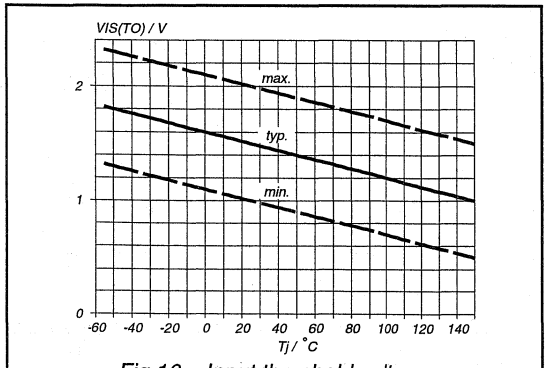


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

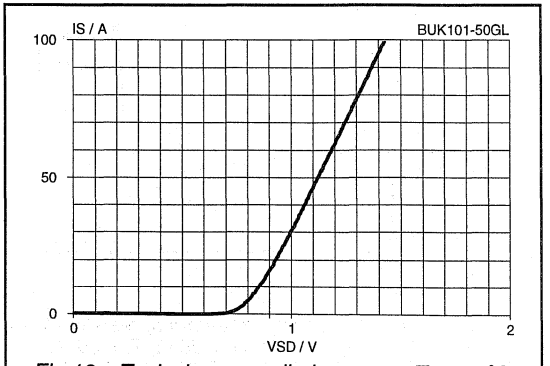


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V

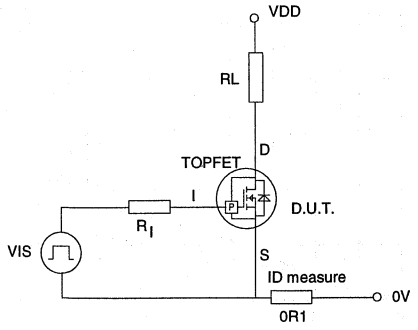


Fig.20. Test circuit for resistive load switching times.

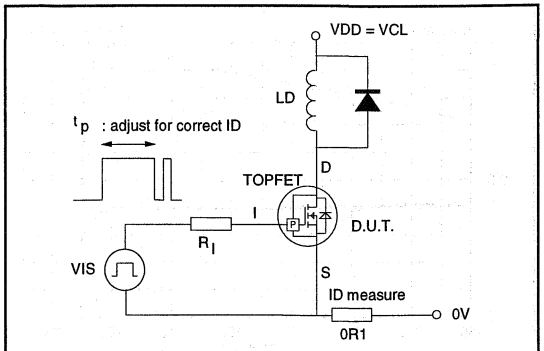


Fig.23. Test circuit for inductive load switching times.

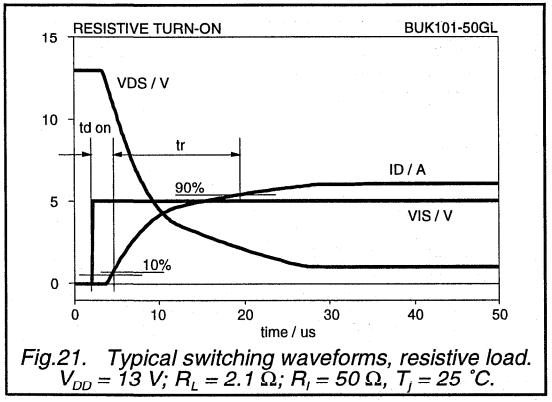


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

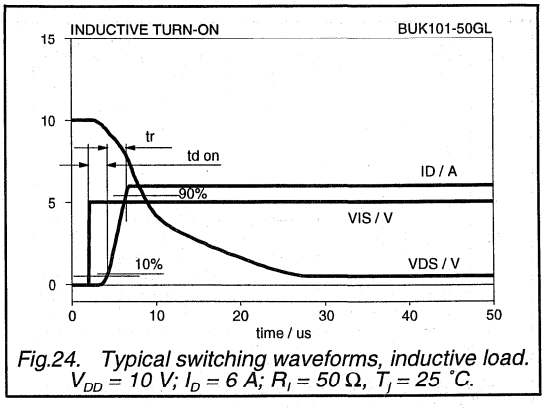


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 ˚C.

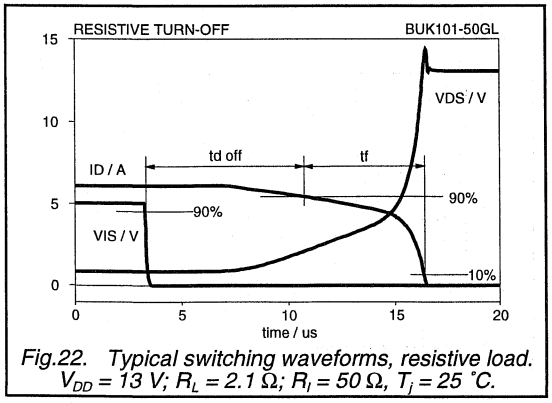


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

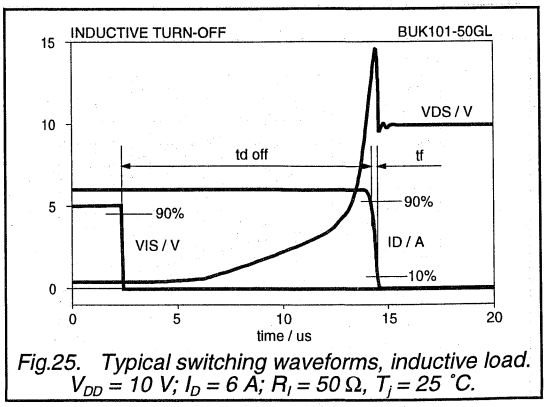


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 ˚C.

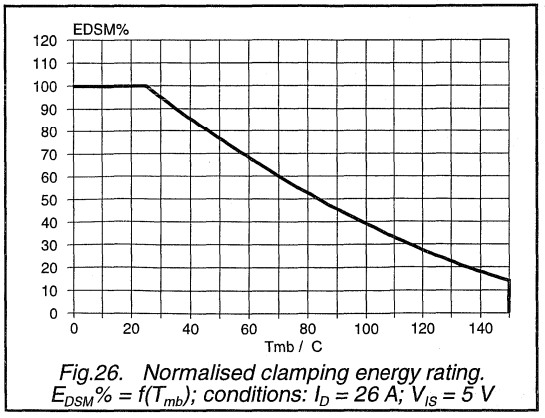


Fig.26. Normalised clamping energy rating. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 26 A; V_{IS} = 5 V

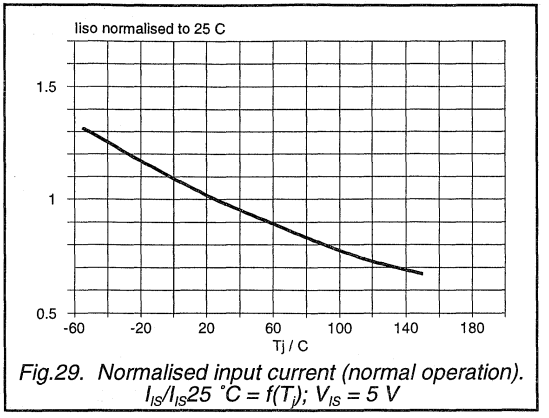


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

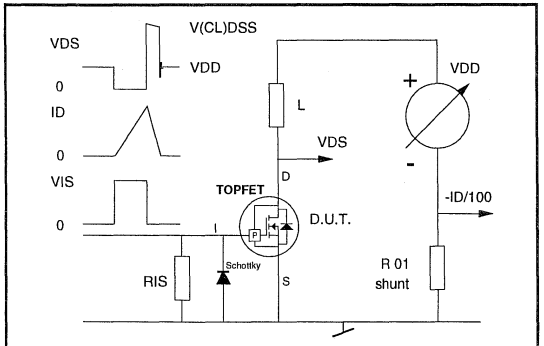


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

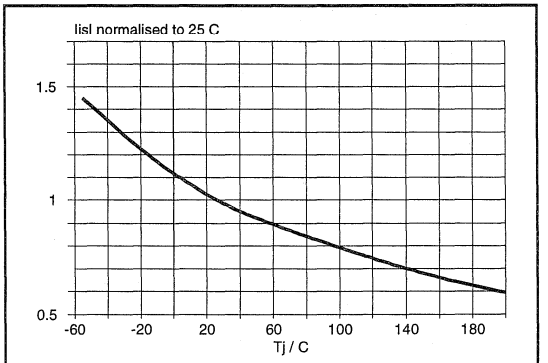


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

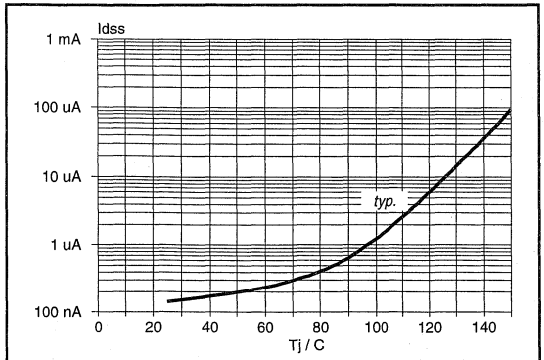


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK101-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	29	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	50	mΩ

FUNCTIONAL BLOCK DIAGRAM

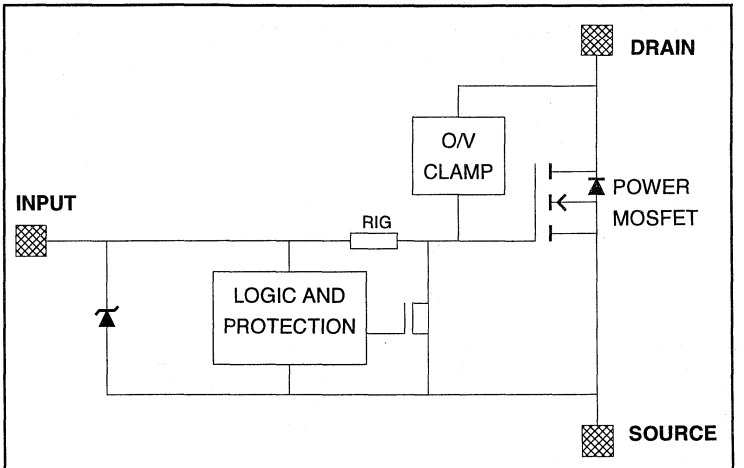
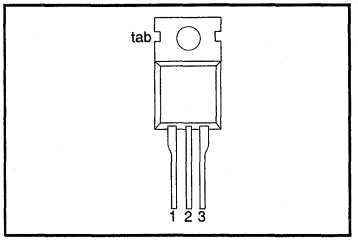


Fig.1. Elements of the TOPFET.

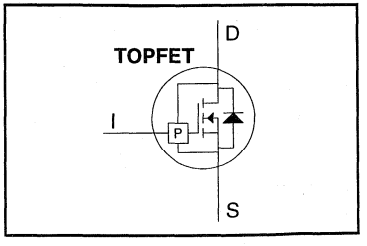
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	29	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	18	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	120	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	20	V
		V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	29	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 27 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \le 300$ µs; $\delta \le 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 13 A; $t_p \le 300$ µs; $\delta \le 0.01$	V_{IS} = 10 V	-	35	50	mΩ
			V_{IS} = 5 V	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \ge 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	1.0	2.5	4.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 10 V	-	80	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_i = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	6	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	18	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	9	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 10 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	22	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	29	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 29 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

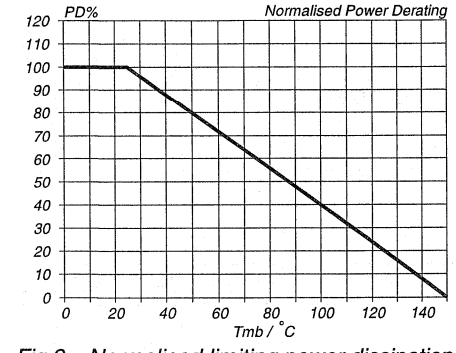


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

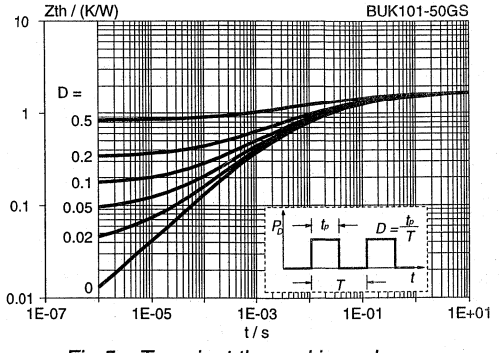


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

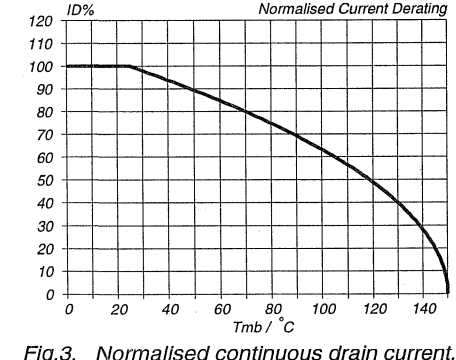


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; *conditions:* $V_{IS} = 5$ V

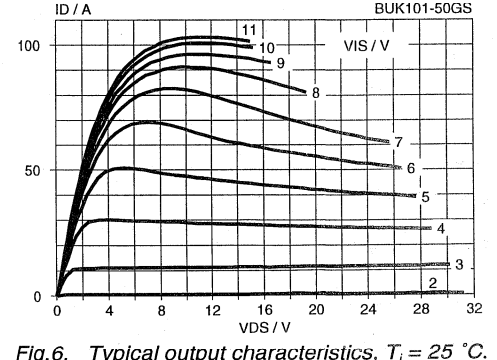


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

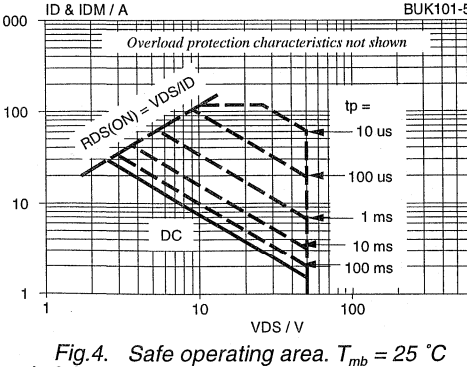


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

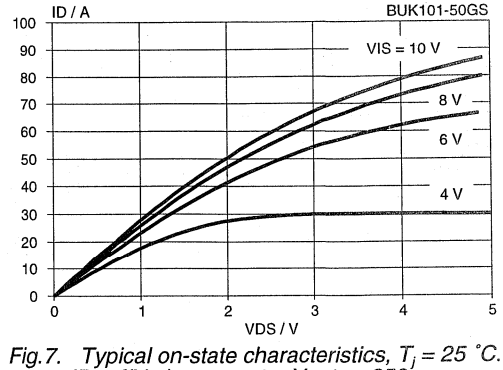


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 250\ \mu s$

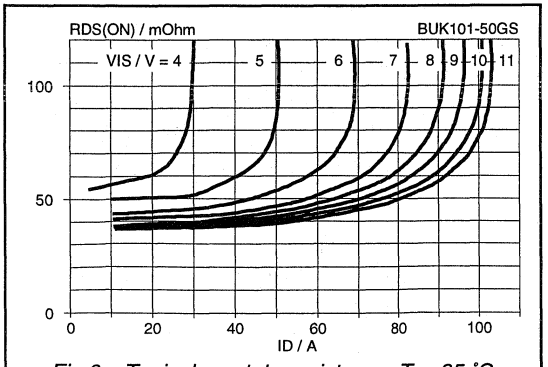


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

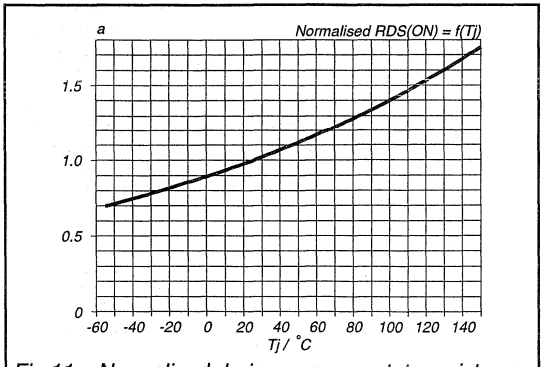


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 13 A; V_{IS} = 10 V

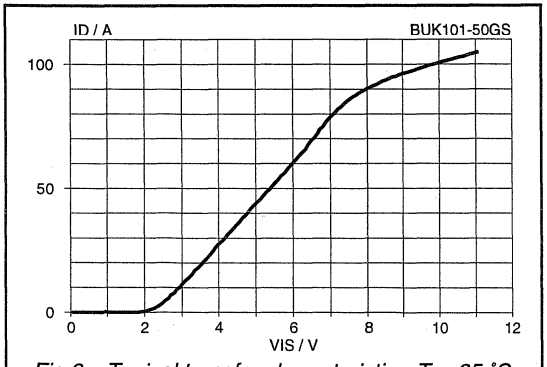


Fig.9. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

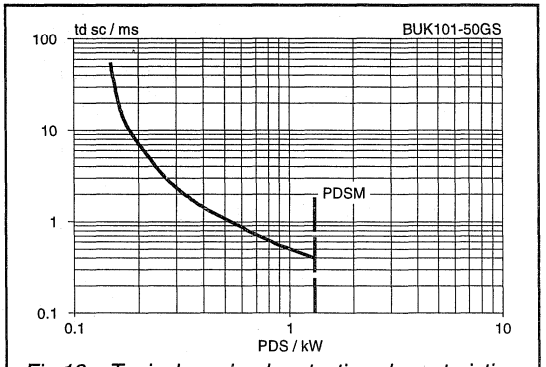


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq$ 5 V; T_j = 25 °C.

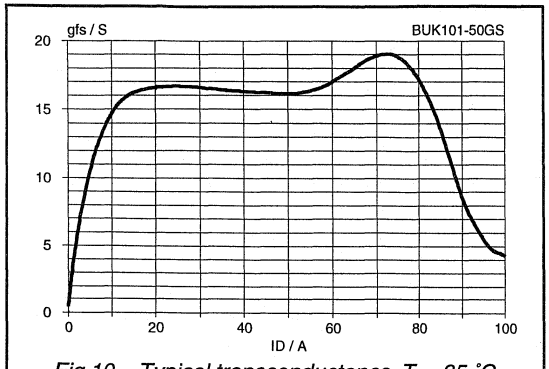


Fig.10. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

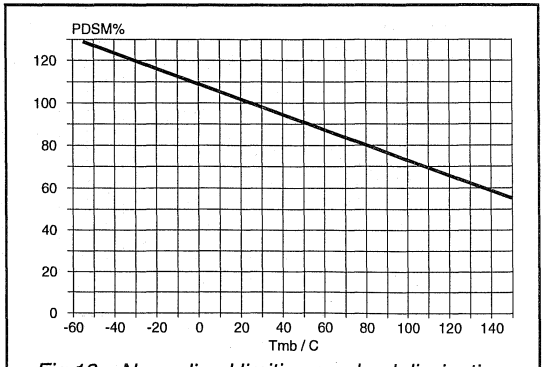


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

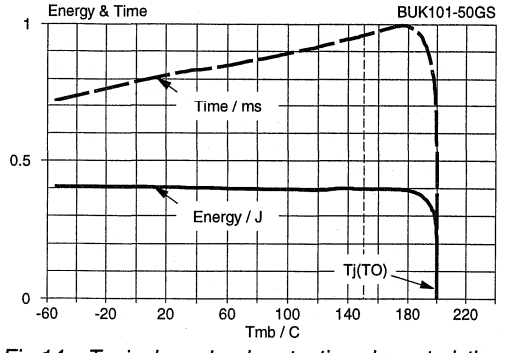


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 10 V; SC load = 30 mΩ

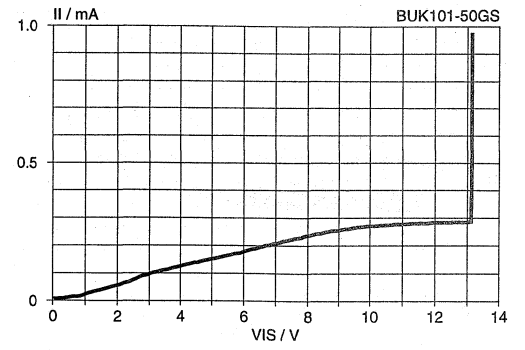


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

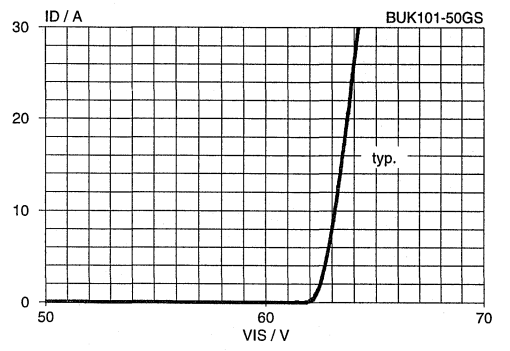


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

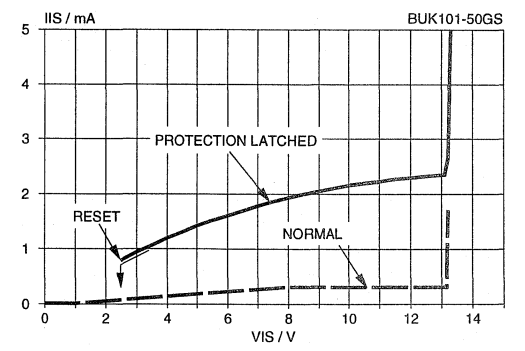


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

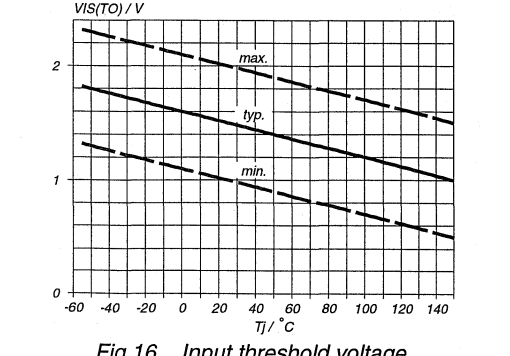


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

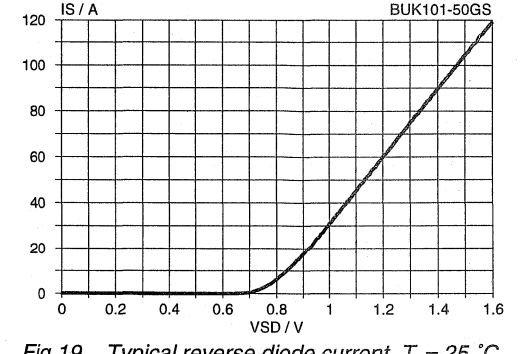


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

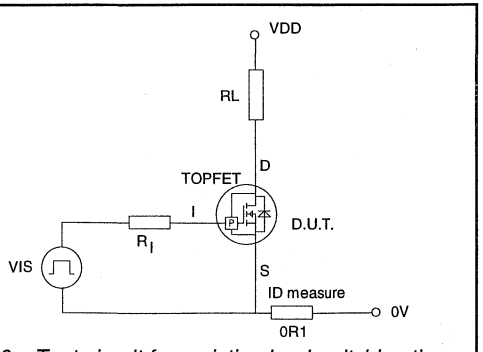


Fig.20. Test circuit for resistive load switching times.

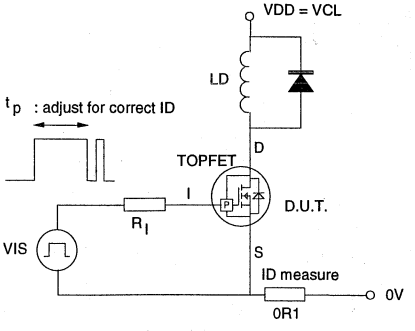


Fig.23. Test circuit for inductive load switching times.

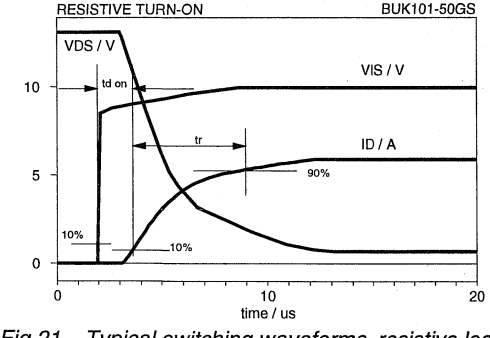


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

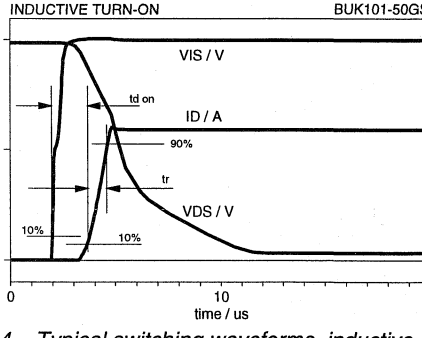


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 ˚C.

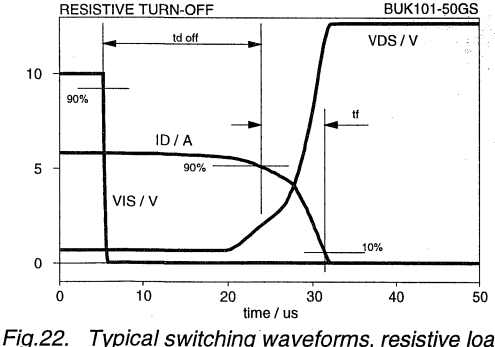


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

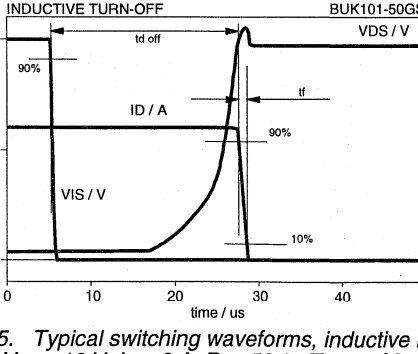


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 ˚C.

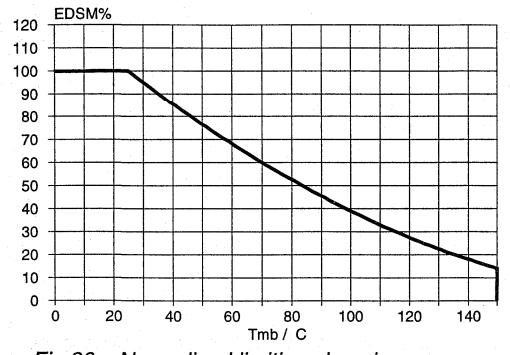


Fig.26. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 27 A; V_{IS} = 10 V

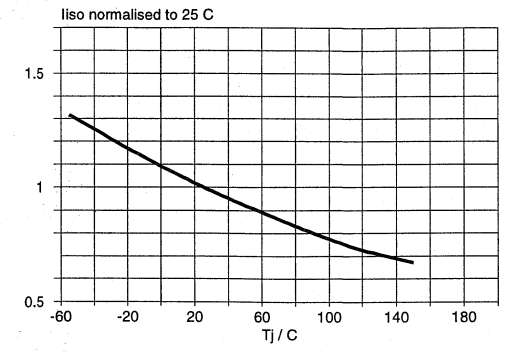


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

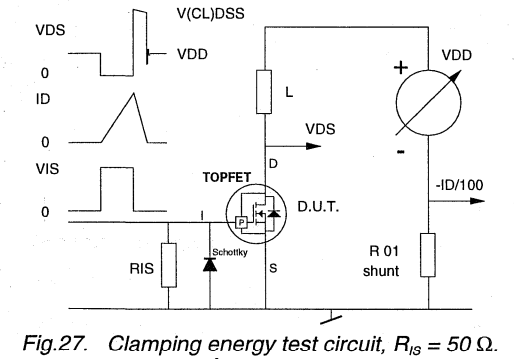


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

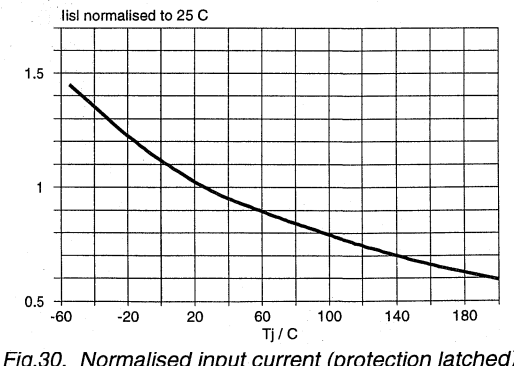


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

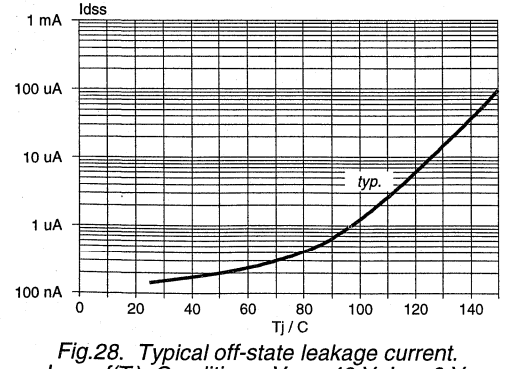


Fig.28. Typical off-state leakage current. I_{DSS} = f(T_j); Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

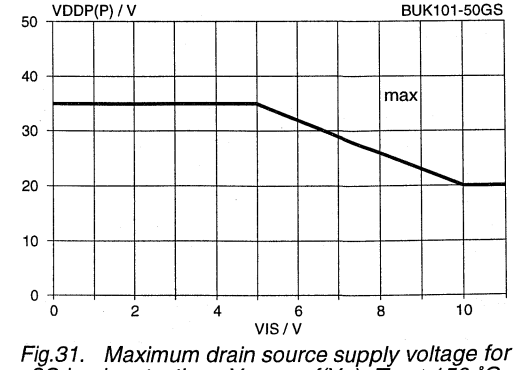


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)}$ = f(V_{IS}); $T_{mb} \leq 150\ ^{\circ}C$

PowerMOS transistor
Logic level TOPFET

BUK102-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		45	A
P_D	Total power dissipation		125	W
T_j	Continuous junction temperature		150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance		35	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

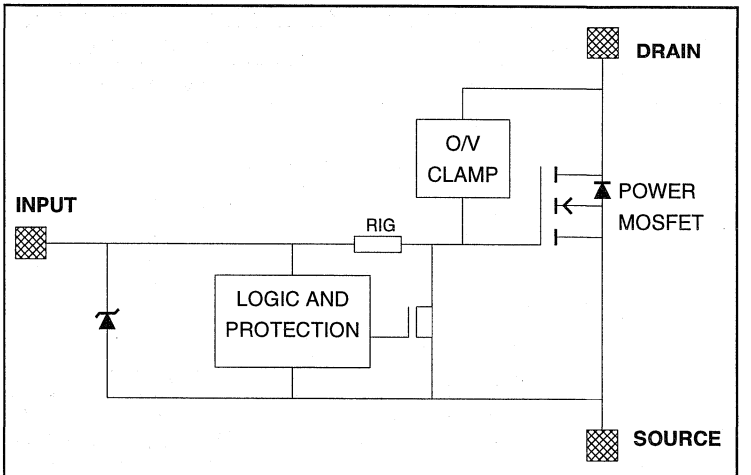
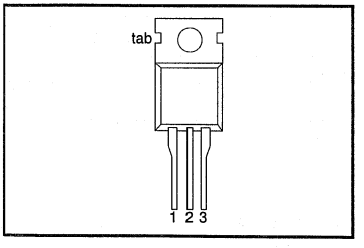


Fig.1. Elements of the TOPFET.

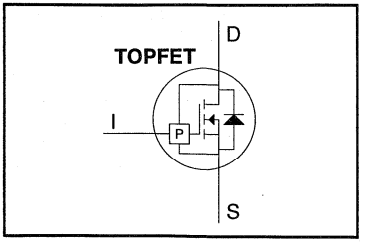
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	16	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 25$ A; $V_{DD} \leq 20$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 25 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	75	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	200	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	17	28	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω . Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	30	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	150	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	120	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	120	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	45	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 45 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

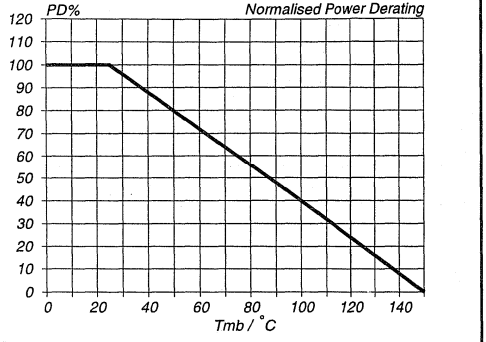


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

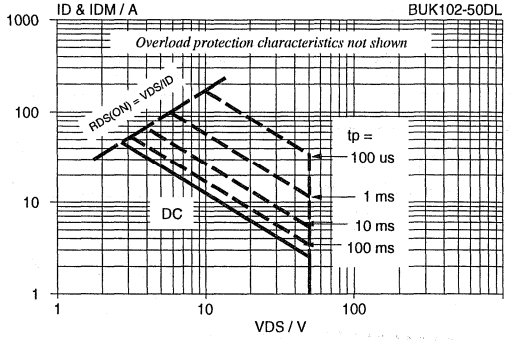


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

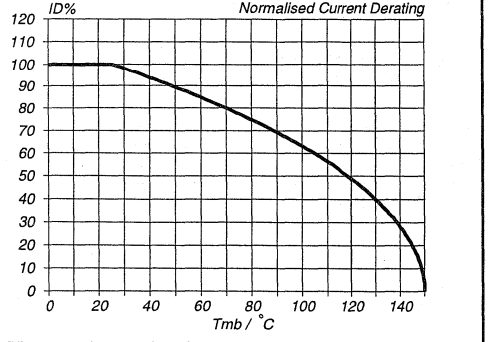


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: V_{IS} = 5 V

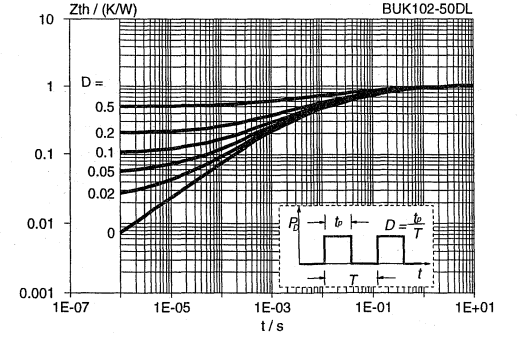


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

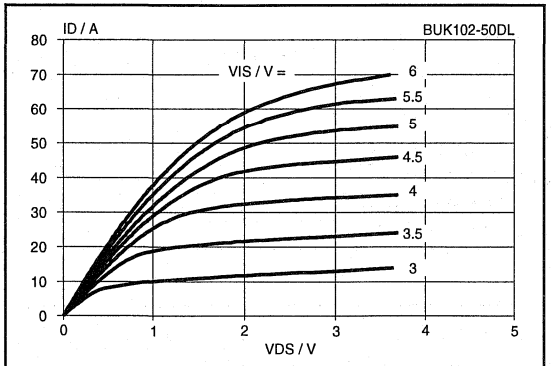


Fig.6. Typical on-state characteristics, T_j = 25 °C. ID = f(V_{DS}); parameter V_{IS}; t_p = 2 ms

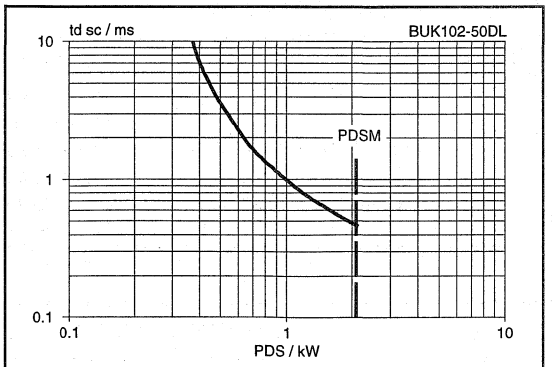


Fig.9. Typical overload protection characteristics. $t_{d\,sc}$ = f(P_{DS}); conditions: $V_{IS} \geq$ 4 V; T_j = 25 °C.

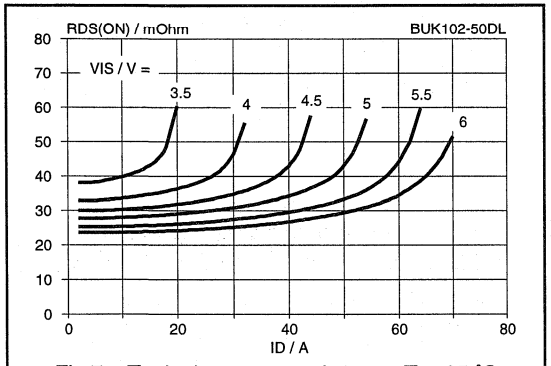


Fig.7. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 2 ms

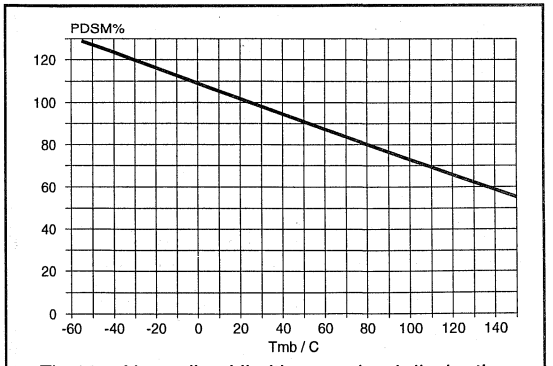


Fig.10. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 °C) = f(T_{mb})

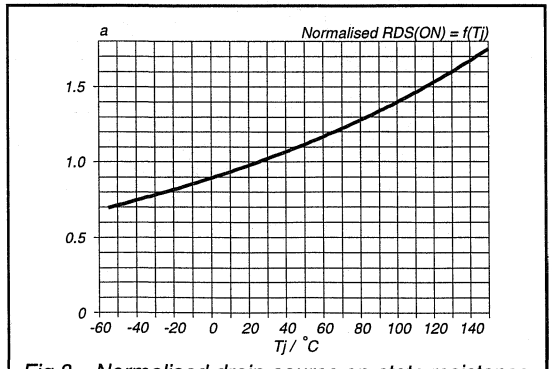


Fig.8. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 °C = f(T_j); I_D = 25 A; V_{IS} = 5 V

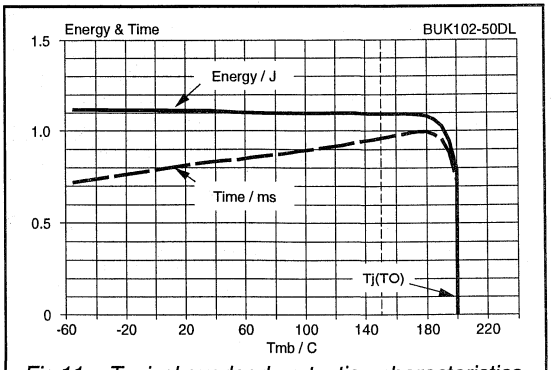


Fig.11. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

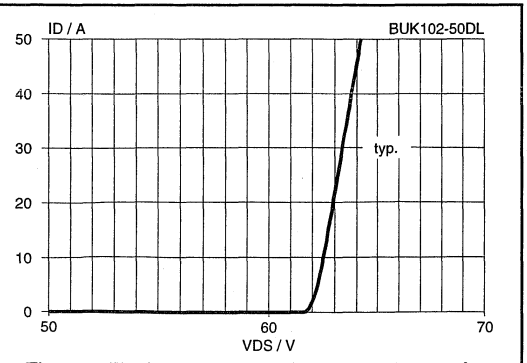


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

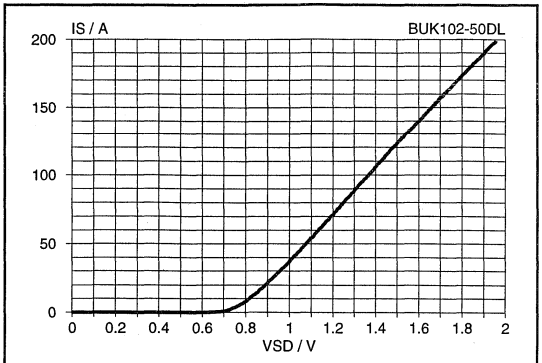


Fig.15. Typical reverse diode current, $T_j = 25$ °C. $I_S = f(V_{SDS})$; conditions: $V_{IS} = 0$ V; $t_p = 250$ µs

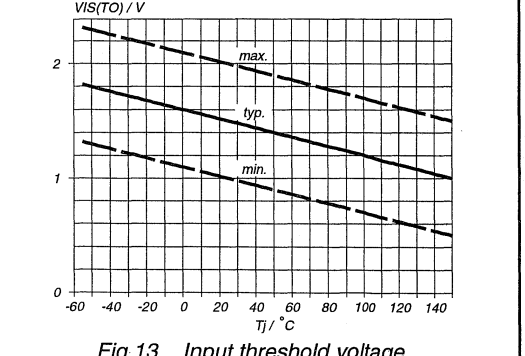


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

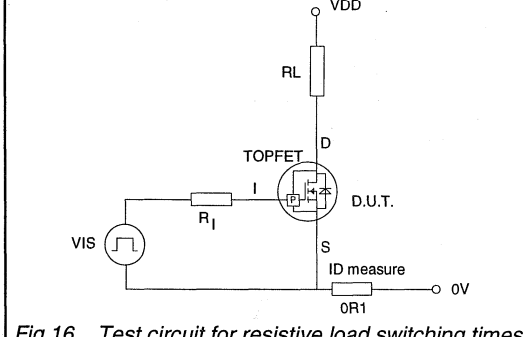


Fig.16. Test circuit for resistive load switching times.

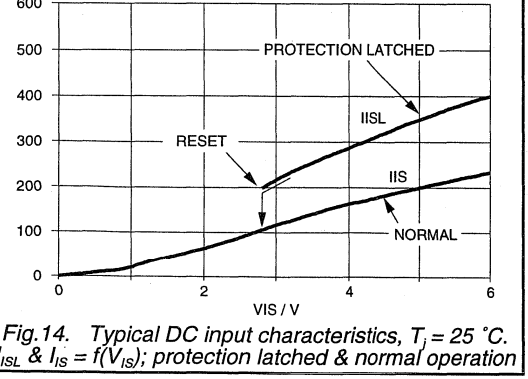


Fig.14. Typical DC input characteristics, $T_j = 25$ °C. I_{ISL} & $I_{IS} = f(V_{IS})$; protection latched & normal operation

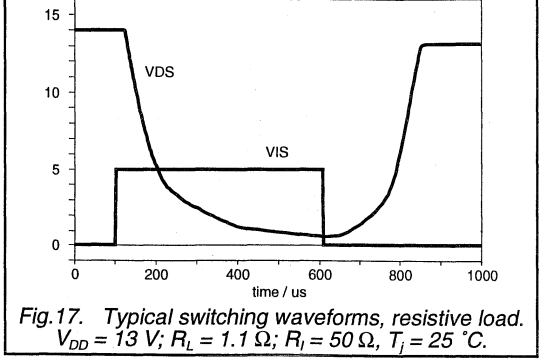


Fig.17. Typical switching waveforms, resistive load. $V_{DD} = 13$ V; $R_L = 1.1$ Ω; $R_I = 50$ Ω, $T_j = 25$ °C.

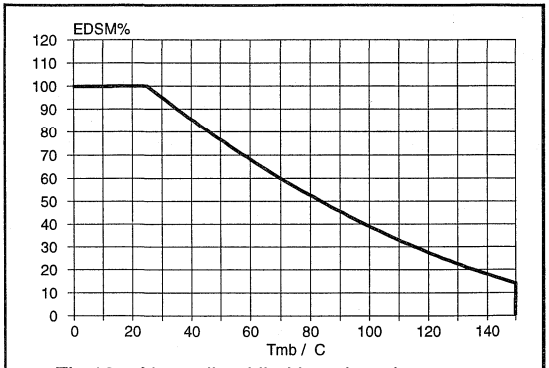


Fig.18. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

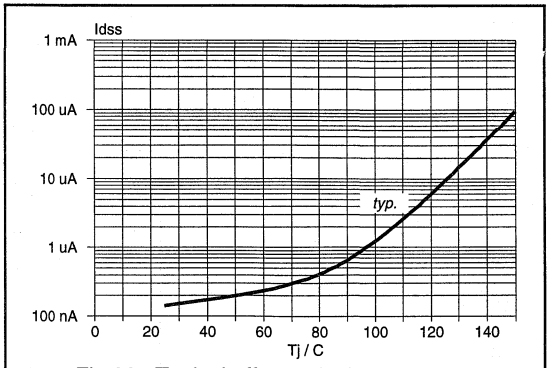


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

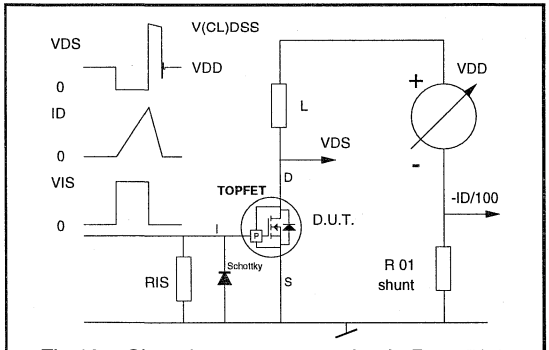


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

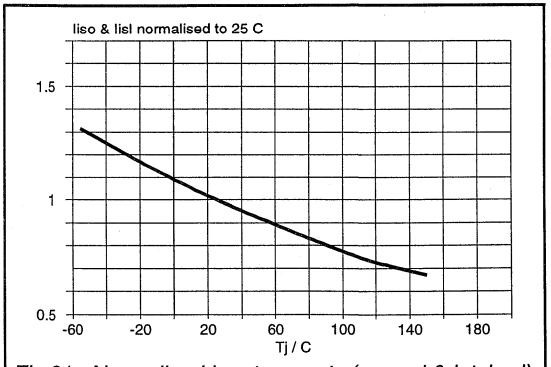


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25°C$ & $I_{ISL}/I_{ISL}25°C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK102-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	45	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	35	mΩ

FUNCTIONAL BLOCK DIAGRAM

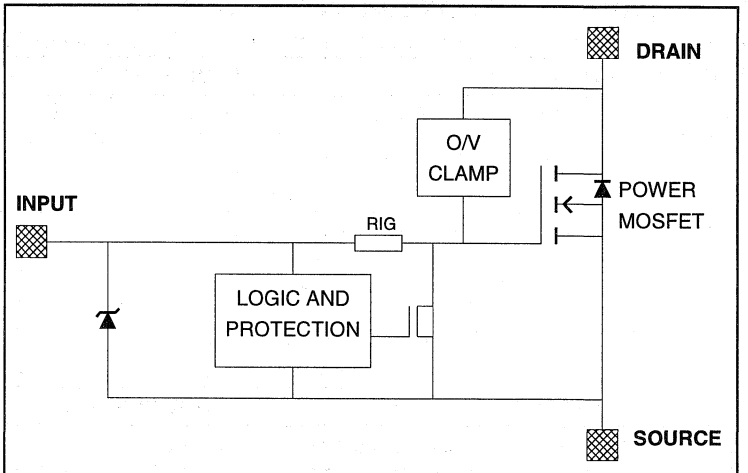
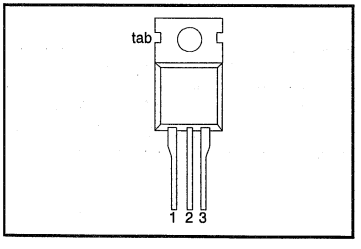


Fig.1. Elements of the TOPFET.

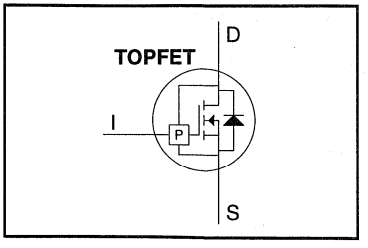
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; V_{IS} = 5 V; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\,sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	2	3.8	10	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	60	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω . Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	8	-	µs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	3.7	-	µs
t_r	Rise time	inductive load I_{DM} = 11 A	-	3.7	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	µs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

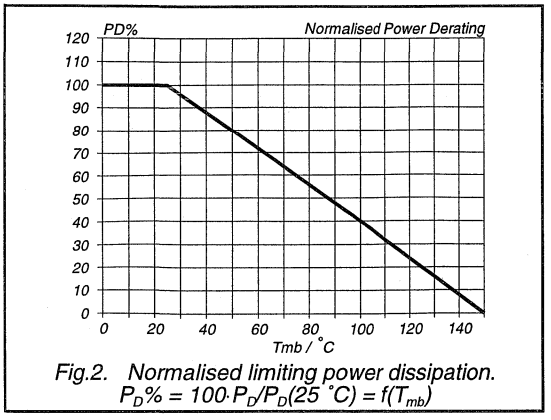


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

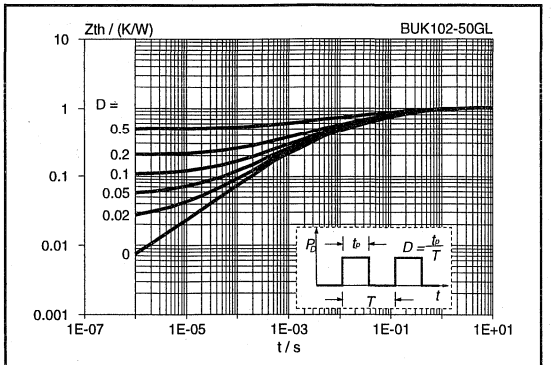


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

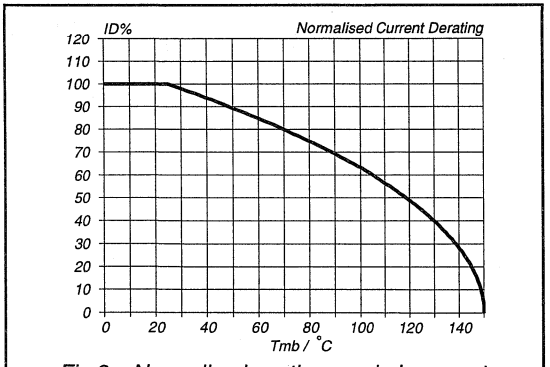


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

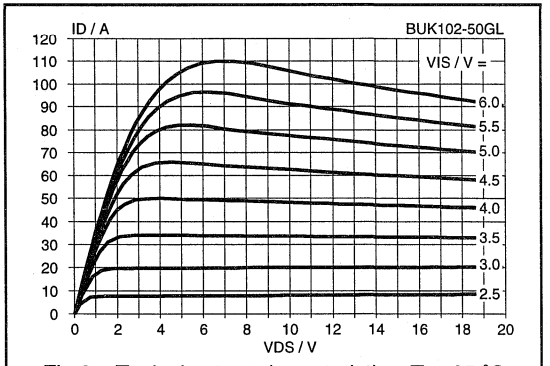


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

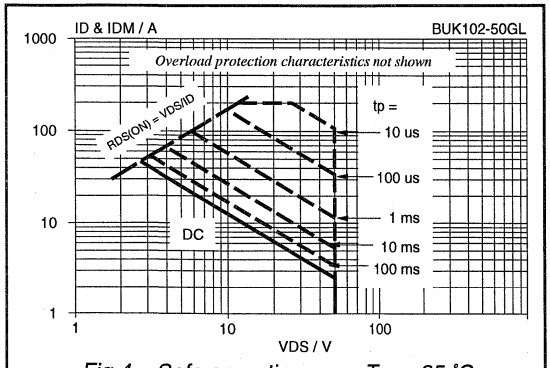


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

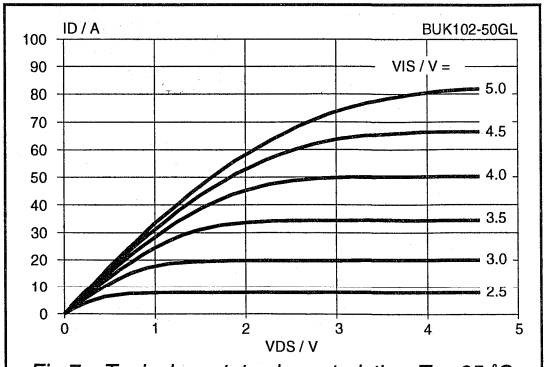


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

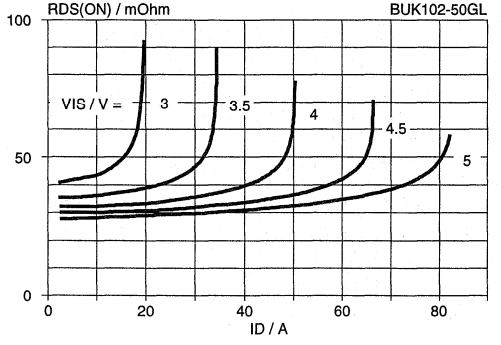


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

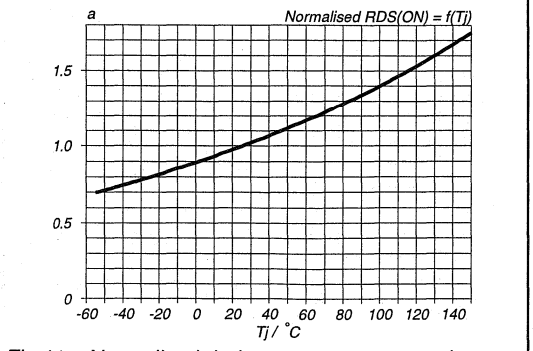


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C $= f(T_j)$; I_D = 25 A; V_{IS} = 5 V

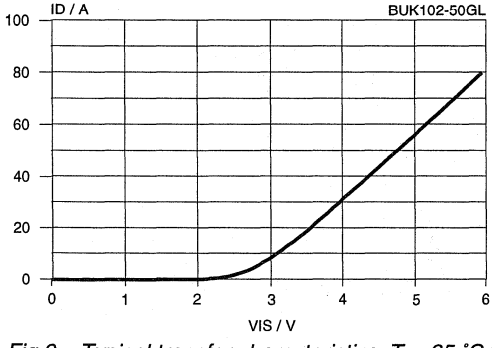


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

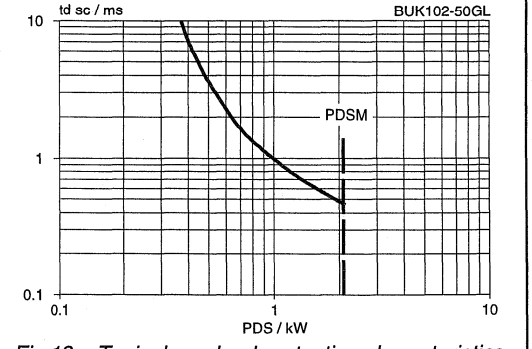


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

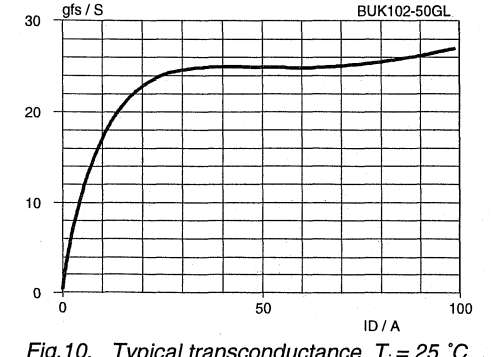


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

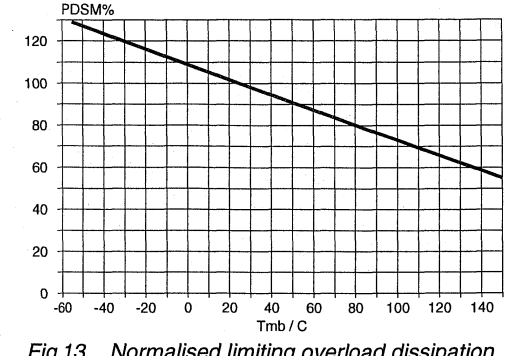


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

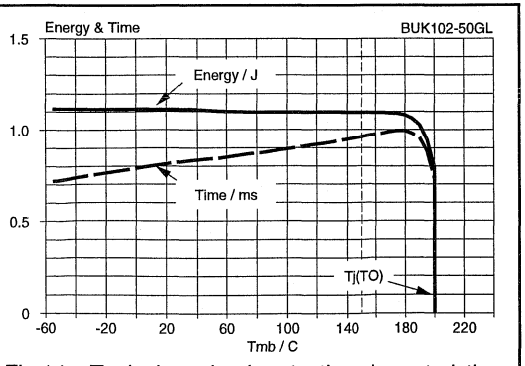


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

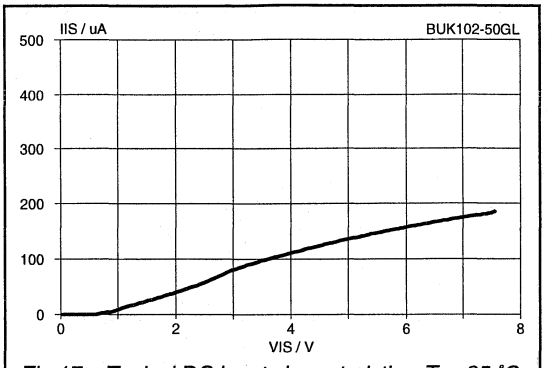


Fig.17. Typical DC input characteristics, T_j = 25 ˚C. $I_{IS} = f(V_{IS})$; normal operation

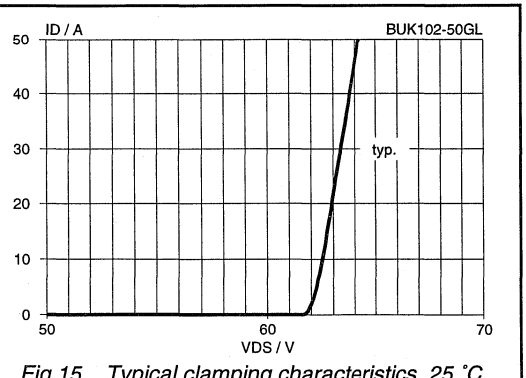


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

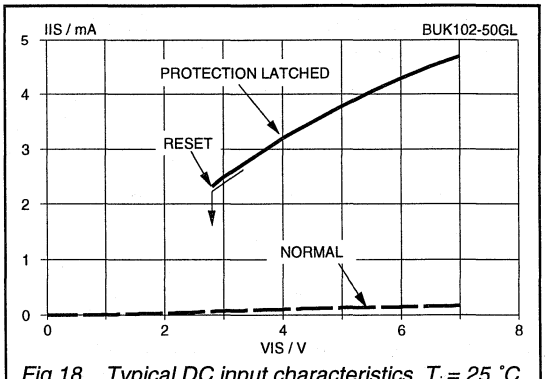


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

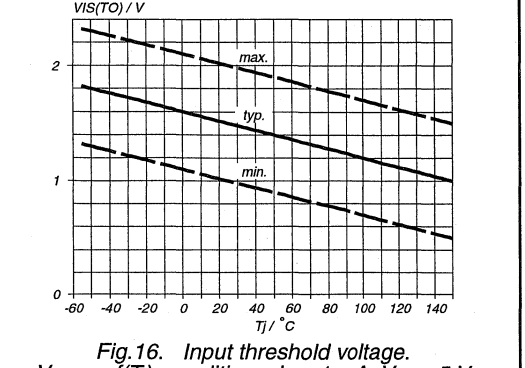


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

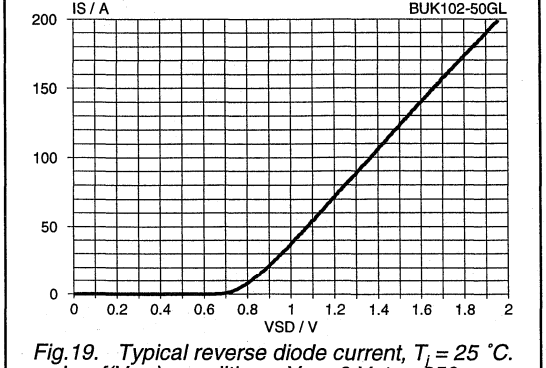


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

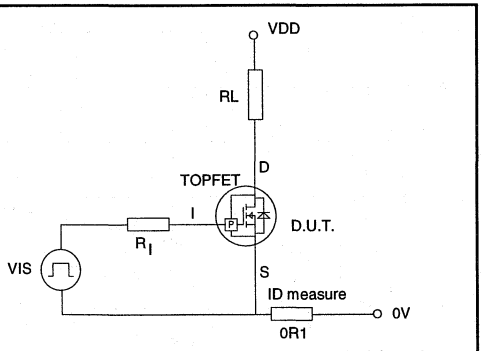


Fig.20. Test circuit for resistive load switching times.

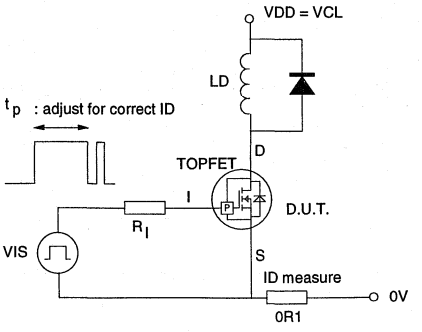


Fig.23. Test circuit for inductive load switching times.

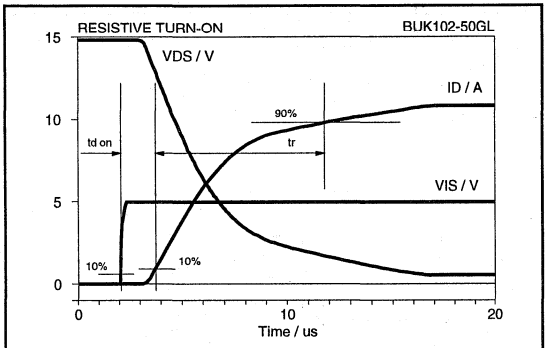


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

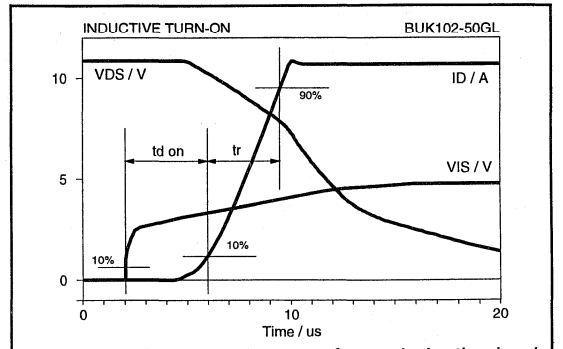


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

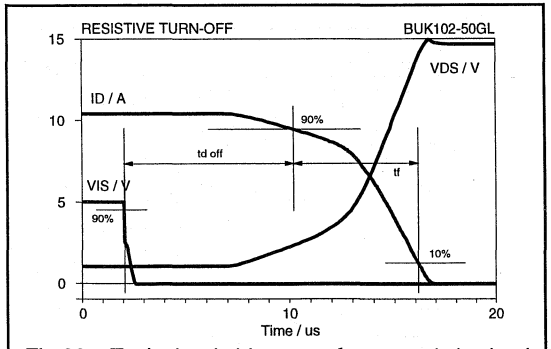


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

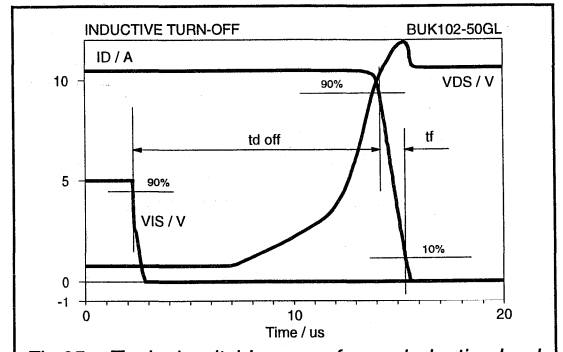


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 °C.

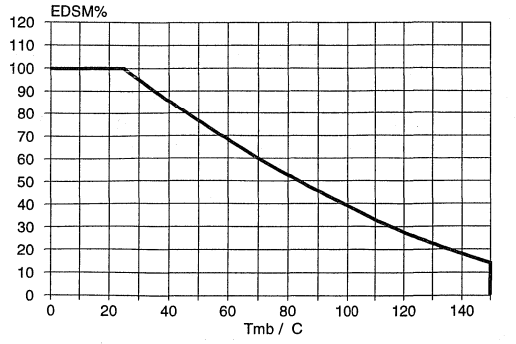


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

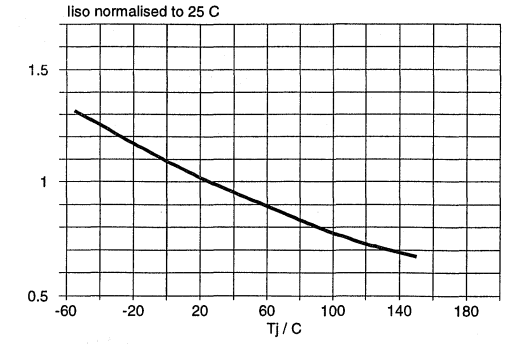


Fig.29. Normalised input current (normal operation). I_{IS}/I_{IS}25 °C = $f(T_j)$; V_{IS} = 5 V

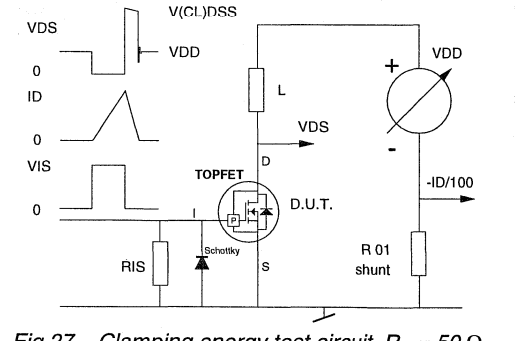


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

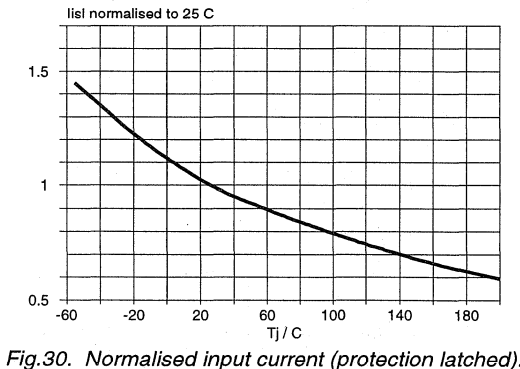


Fig.30. Normalised input current (protection latched). I_{ISL}/I_{ISL}25 °C = $f(T_j)$; V_{IS} = 5 V

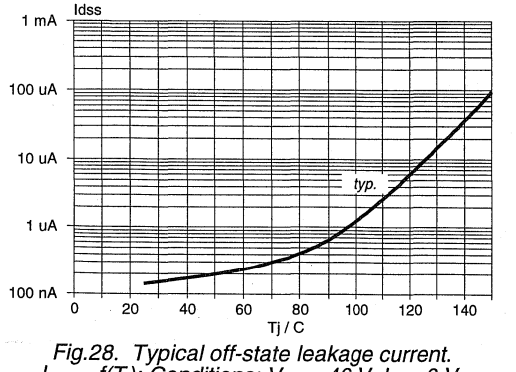


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK102-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	28	mΩ

FUNCTIONAL BLOCK DIAGRAM

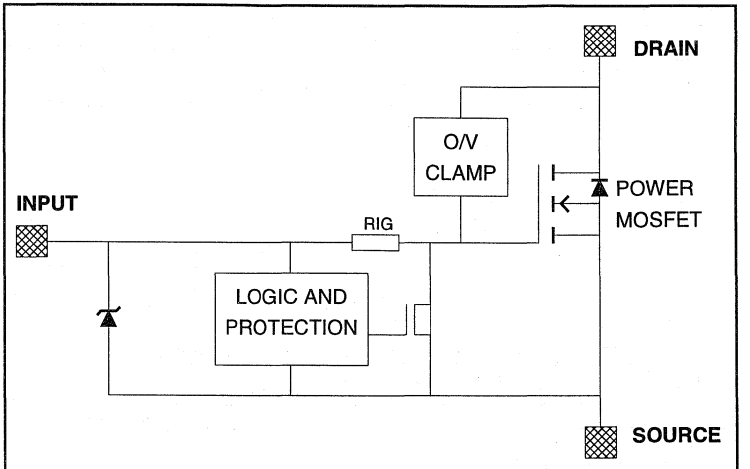
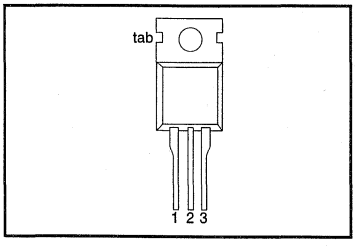


Fig.1. Elements of the TOPFET.

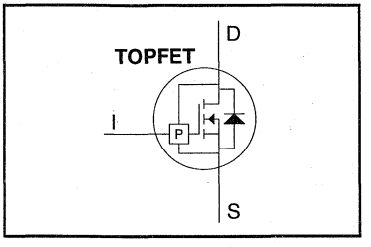
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	50	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	31	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	200	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	16	V
		V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	50	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \le 300$ µs; $\delta \le 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; $t_p \le 300$ µs; $\delta \le 0.01$	V_{IS} = 10 V	-	22	28	mΩ
			V_{IS} = 5 V	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	1.1	-	J
$t_{d\,sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \ge 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	2	6	20	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq$ 300 µs; $\delta \leq$ 0.01	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 10 V	-	150	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	5.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	µs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	9	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 11 A	-	1.3	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	18	-	µs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

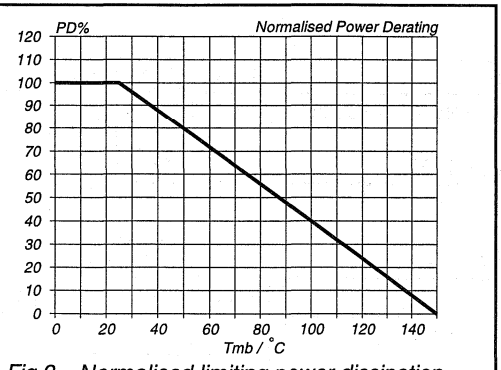


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

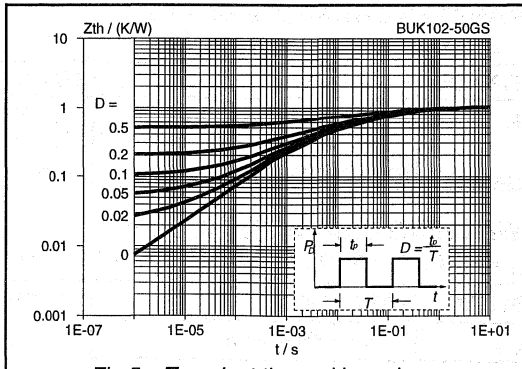


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

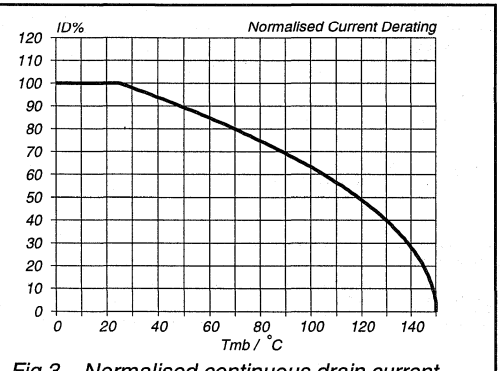


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

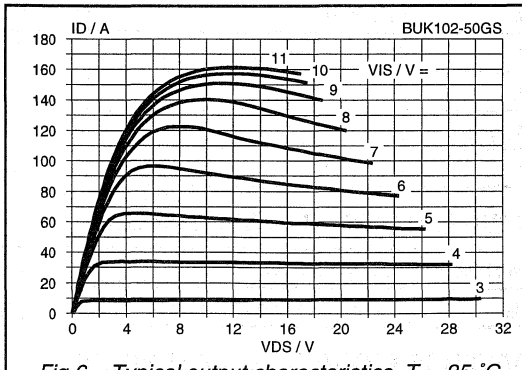


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
ID = $f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

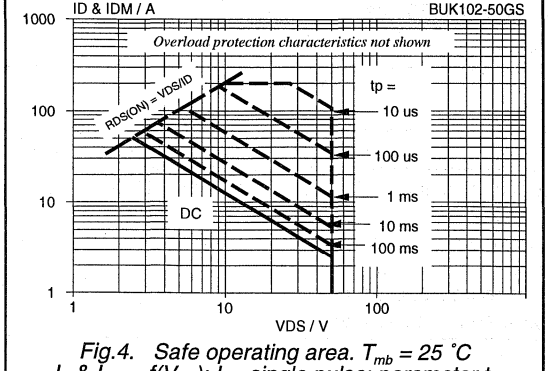


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

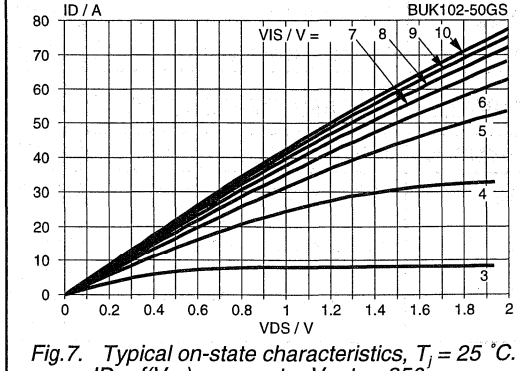


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
ID = $f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

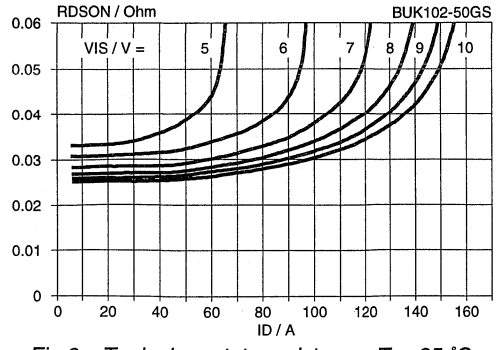


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

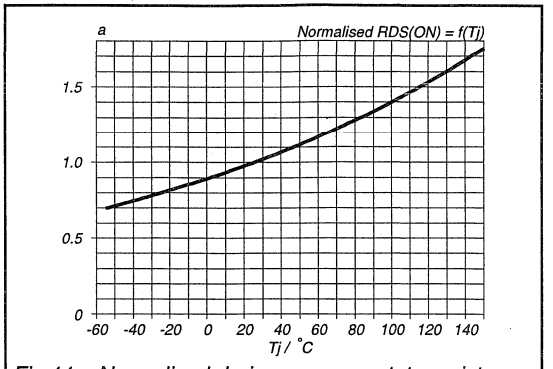


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^{\circ}C = f(T_j)$; I_D = 25 A; V_{IS} = 10 V

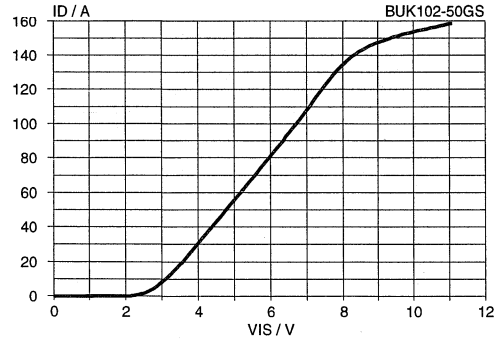


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

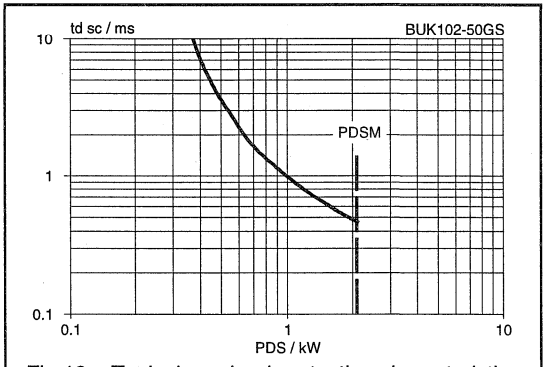


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 5$ V; T_j = 25 ˚C.

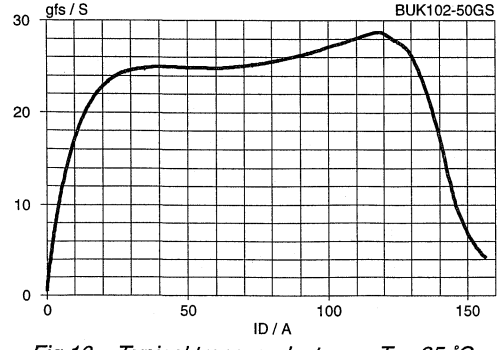


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

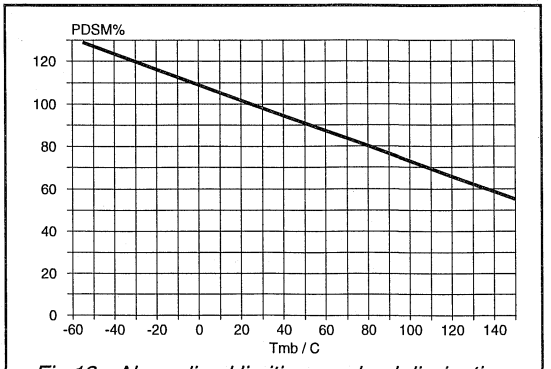


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^{\circ}C) = f(T_{mb})$

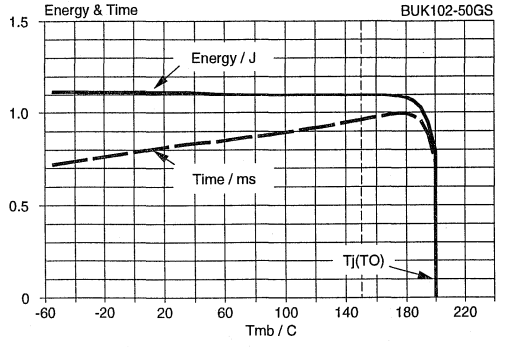


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 10 V; SC load = 30 mΩ

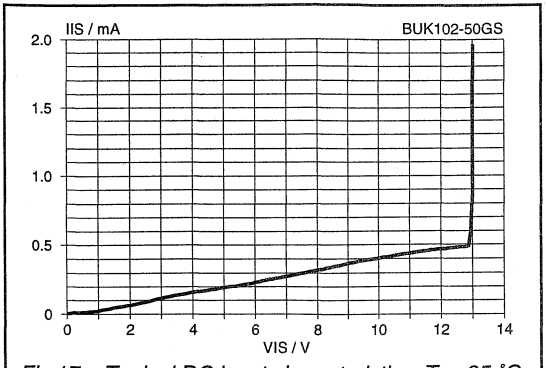


Fig.17. Typical DC input characteristics, T_j = 25 ˚C. $I_{IS} = f(V_{IS})$; normal operation

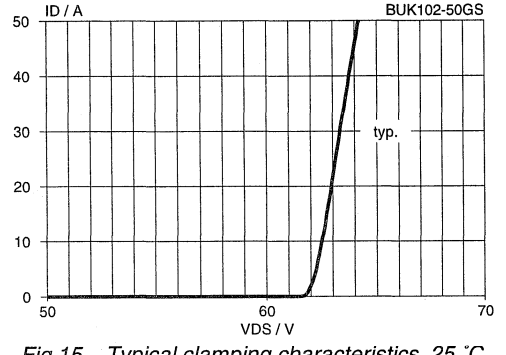


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

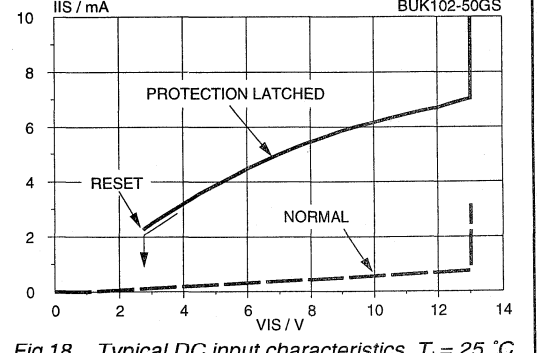


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

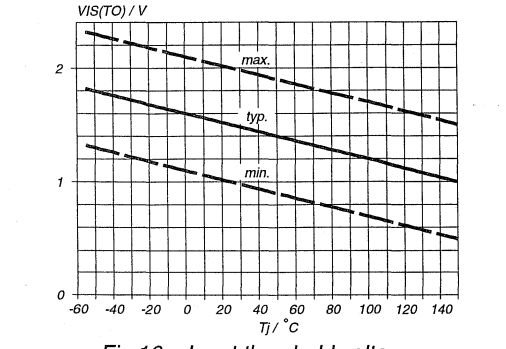


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

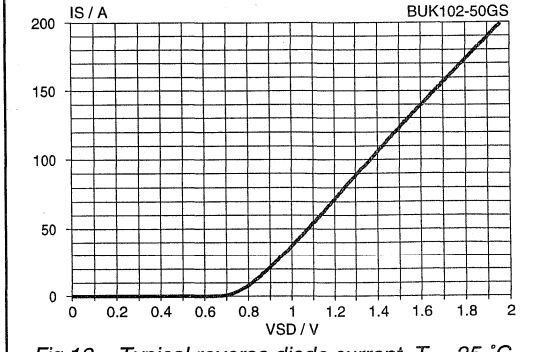


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

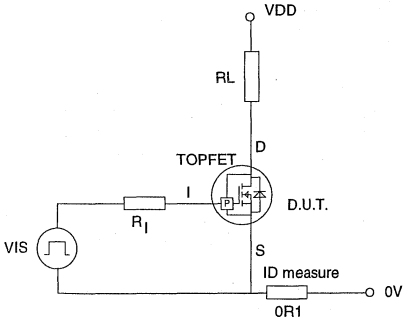


Fig.20. Test circuit for resistive load switching times.

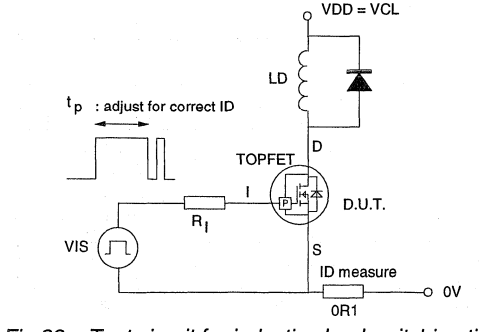


Fig.23. Test circuit for inductive load switching times.

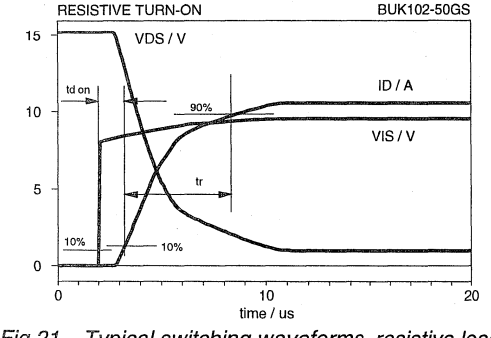


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

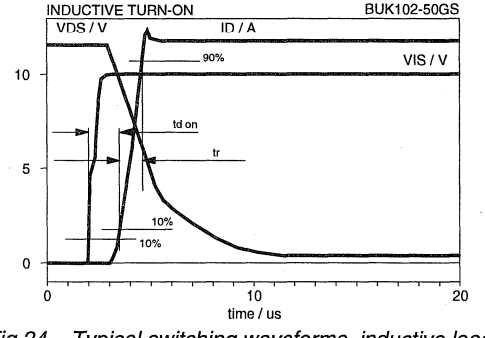


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 ˚C.

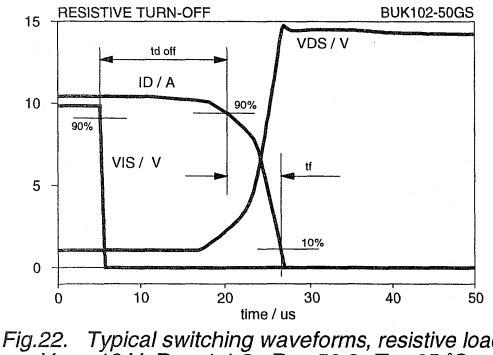


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

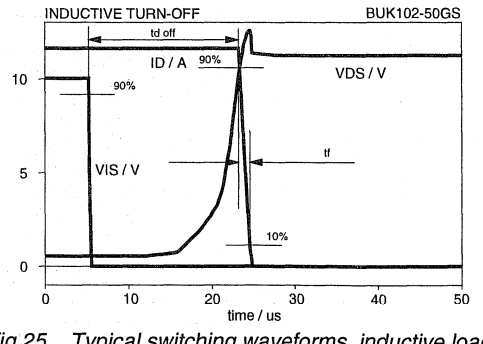


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 ˚C.

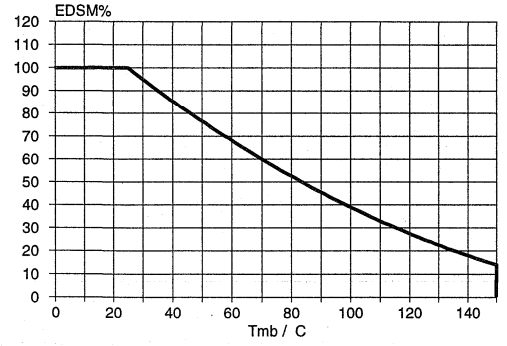


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

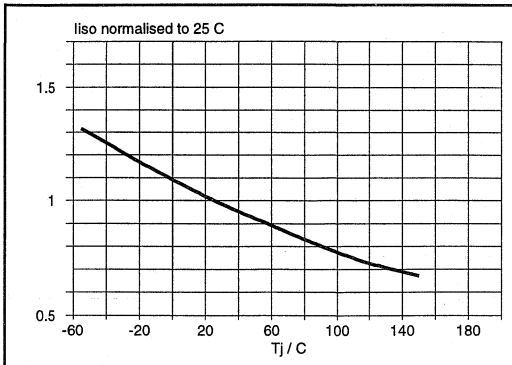


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

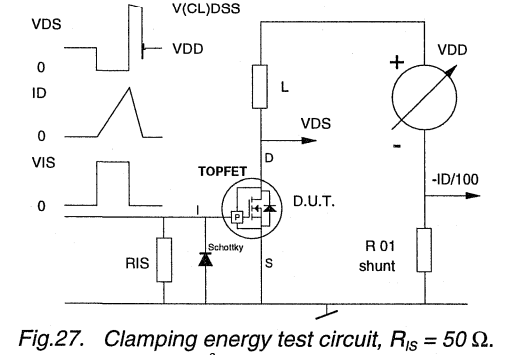


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

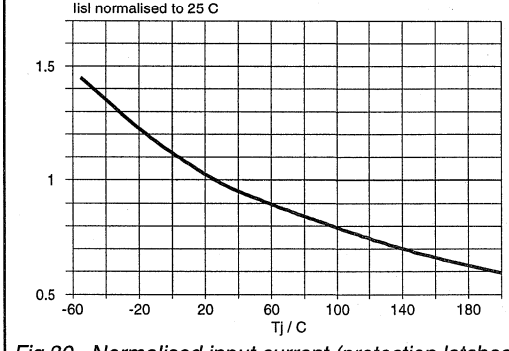


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

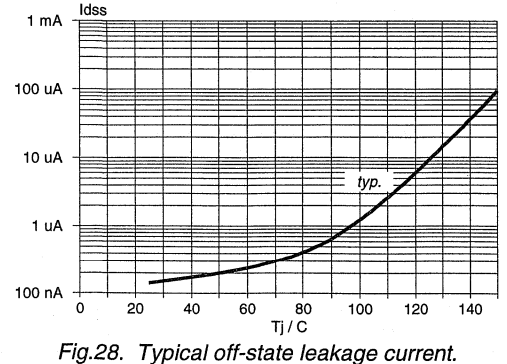


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

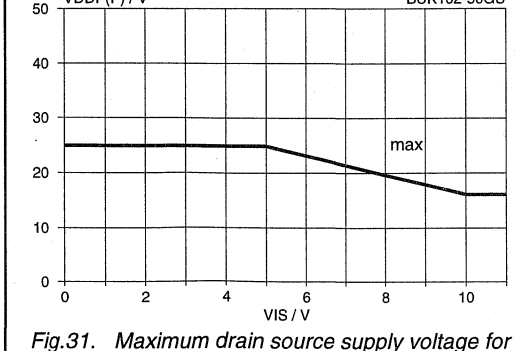


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^{\circ}C$

PowerMOS transistor
Logic level TOPFET

BUK104-50L/S
BUK104-50LP/SP

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_{tot}	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	125	mΩ
	V_{IS} = 7 V	100	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK104-50L	5	V
	BUK104-50S	10	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

FUNCTIONAL BLOCK DIAGRAM

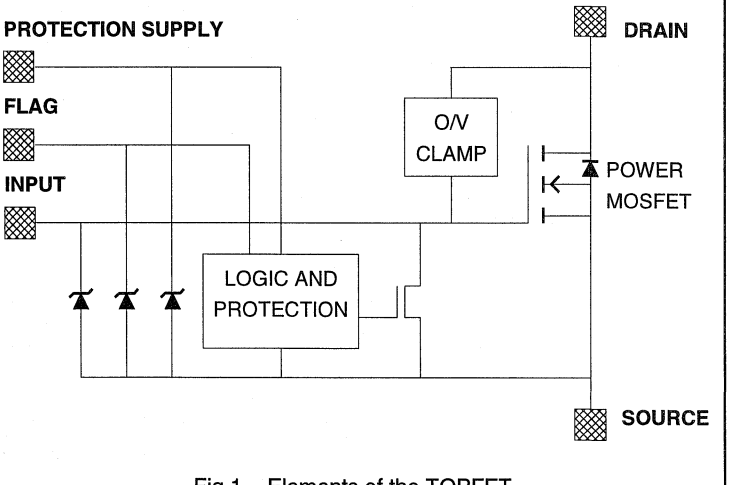


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

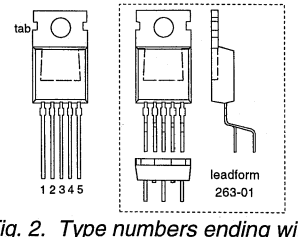


Fig. 2. Type numbers ending with suffix P refer to leadform 263-01.

SYMBOL

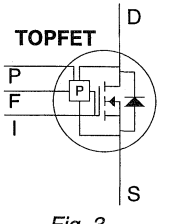


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Voltages				
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
V_{FS}	Continuous flag voltage	-	0	11	V
V_{PS}	Continuous supply voltage	-	0	11	V
	Currents	V_{IS} =	-	7 | 5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	15 | 13	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	9.5 | 8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	60 | 54	A
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		V_{IS} =	7 | 5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection			
		BUK104-50L	4.4 | 4	-	V
		BUK104-50S	5.4 | 5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$			
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; $L \leq 10$ µH			
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	25	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	45	V
P_{DSM}	Instantaneous overload dissipation		-	0.8	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	15	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 15$ A; $R_{IS} \geq 100\ \Omega$	-	200	mJ
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 95$ °C; $I_{DM} = 4$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	15	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 7.5$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$	$V_{IS} = 7$ V	-	75	100	mΩ
			$V_{IS} = 5$ V	-	95	125	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH; $R_I \geq 2$ kΩ				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	150	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	375	-	µs
	Over temperature protection	$V_{PS} = V_{PSN}$; $R_I \geq 2$ kΩ				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 0.65$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10$ V; $I_{DM} = 7.5$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	25	-	A
		$V_{IS} = 10$ V		40	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK104-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK104-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 15$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	8	-	ns
t_r	Rise time		-	13	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	100	-	ns
t_f	Fall time		-	45	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	415	600	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	275	400	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	55	80	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK104-50L	2.5	3.3	4	V
		BUK104-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

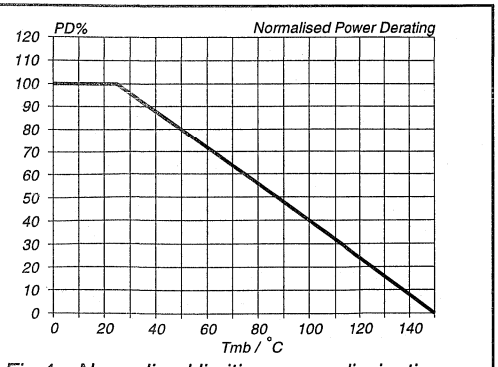


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

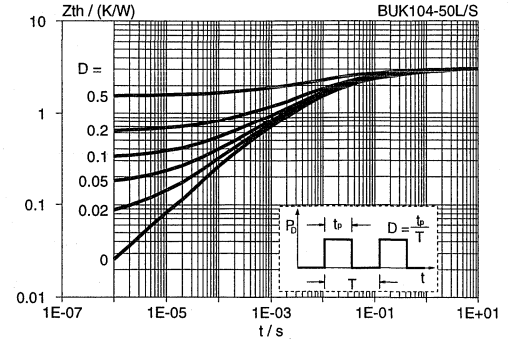


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

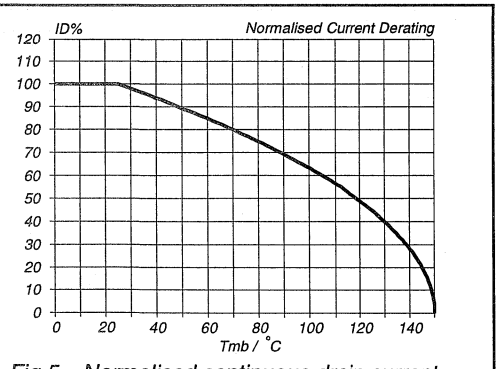


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

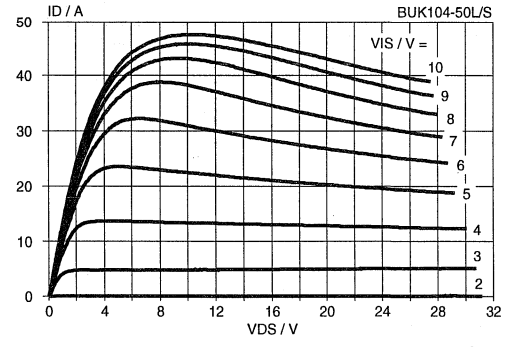


Fig.8. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

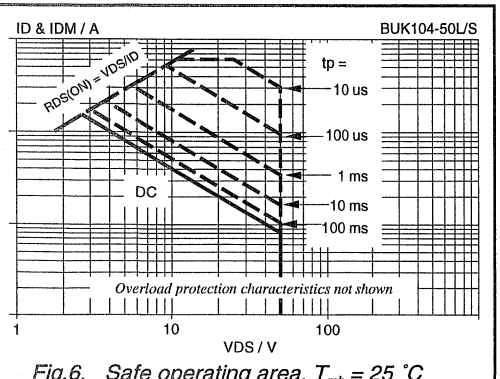


Fig.6. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

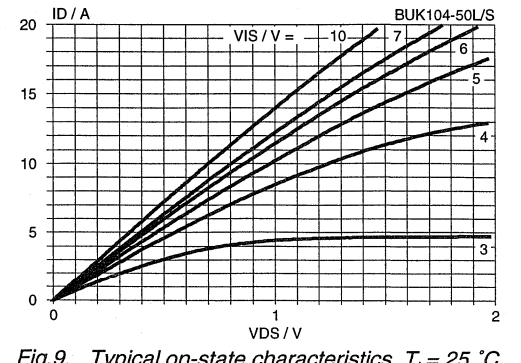


Fig.9. Typical on-state characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

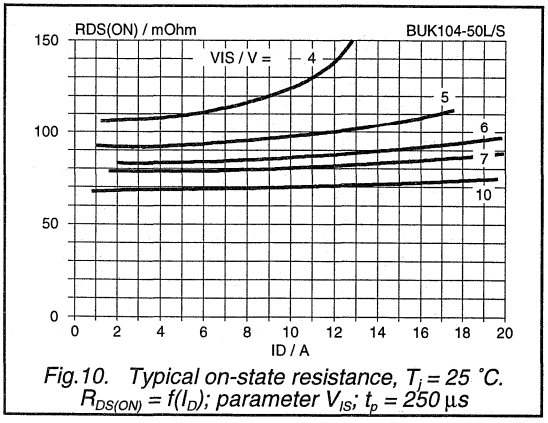


Fig.10. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

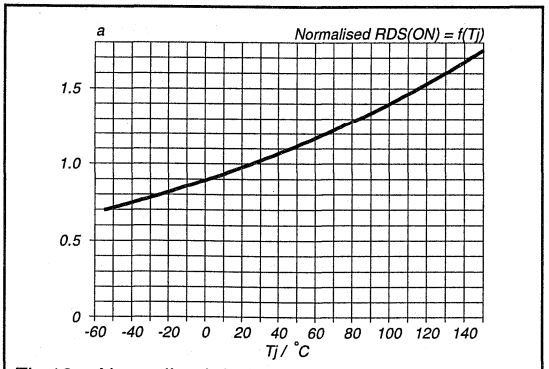


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}$25 ˚C = $f(T_j)$; I_D = 7.5 A; $V_{IS} \geq$ 5 V

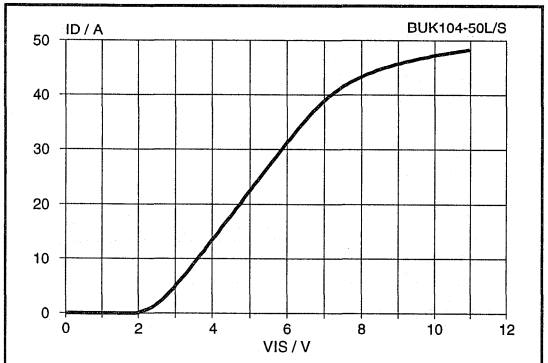


Fig.11. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

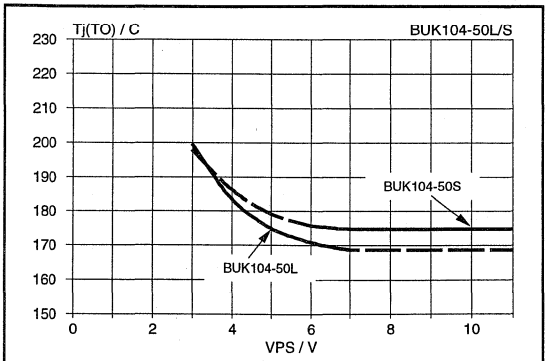


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

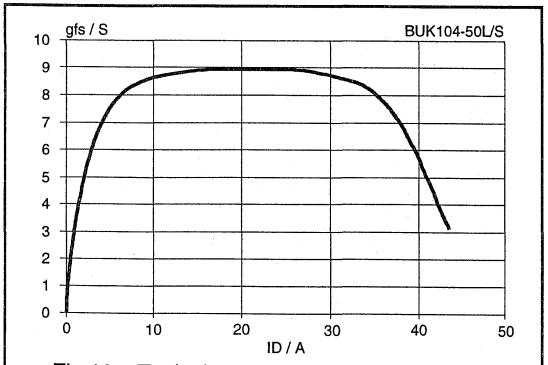


Fig.12. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

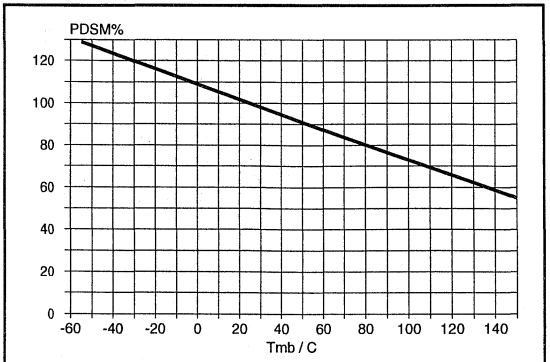


Fig.15. Normalised limiting overload dissipation. P_{DSM}% =100·P_{DSM}/P_{DSM}(25 ˚C) = $f(T_{mb})$

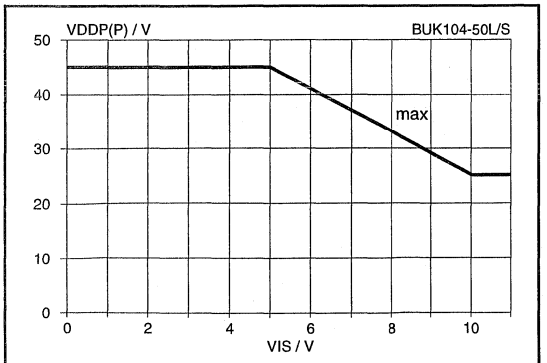


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

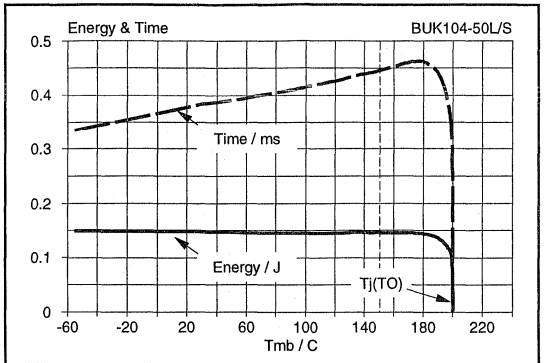


Fig.19. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{PS} = V_{PSN}$, $V_{IS} = 7$ V; SC load

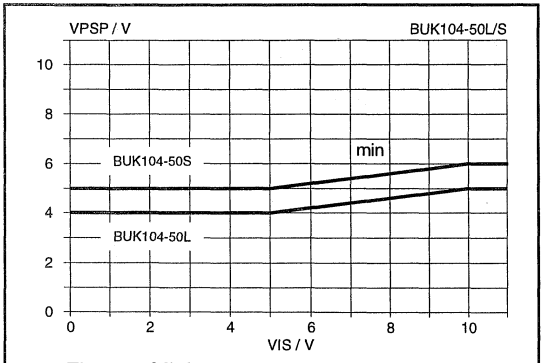


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

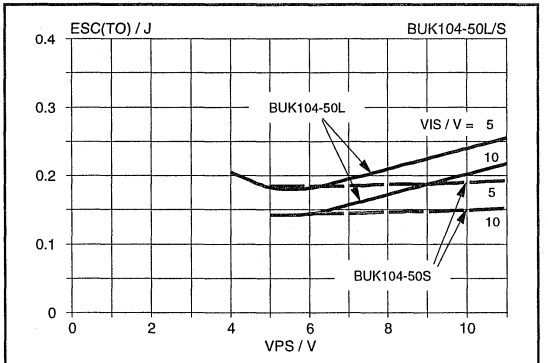


Fig.20. Typical overload protection energy, $T_j = 25$ °C $E_{SC(TO)} = f(V_{PS})$; conditions: $V_{DS} = 13$ V, parameter V_{IS}

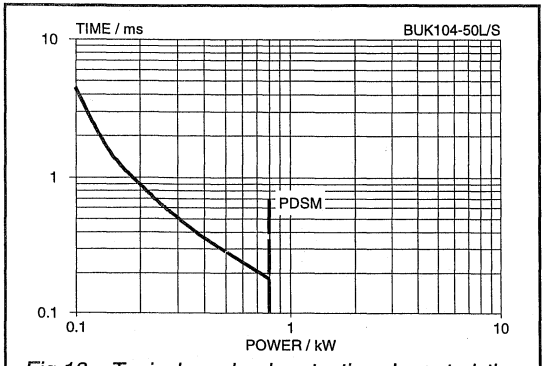


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

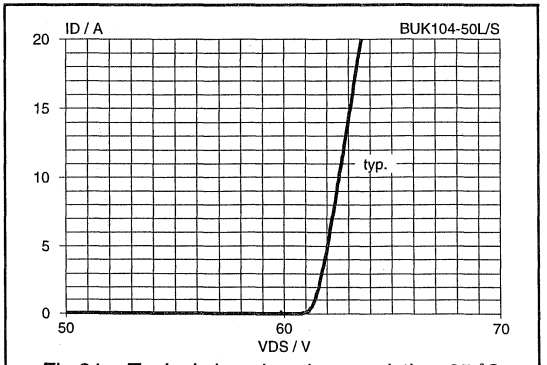


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $R_{IS} = 100\ \Omega$; $t_p \leq 50\ \mu s$

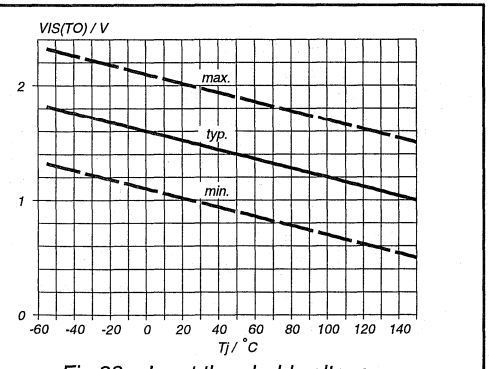


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; *conditions:* $I_D = 1$ *mA;* $V_{DS} = 5$ *V*

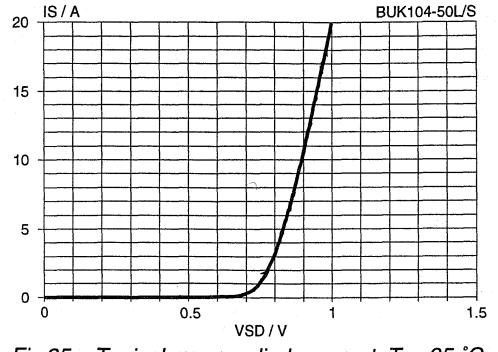


Fig.25. Typical reverse diode current, $T_j = 25$ *°C.*
$I_S = f(V_{SDS})$; *conditions:* $V_{IS} = 0$ *V;* $t_p = 250$ *µs*

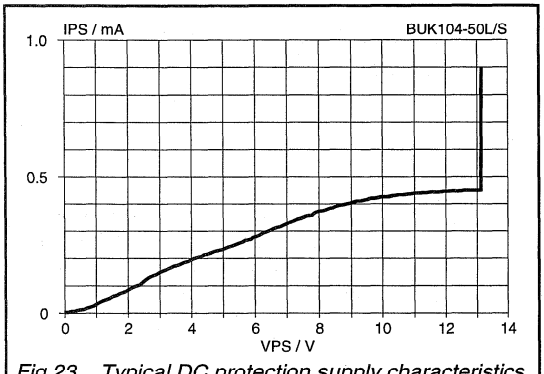


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; *normal or overload operation;* $T_j = 25$ *°C*

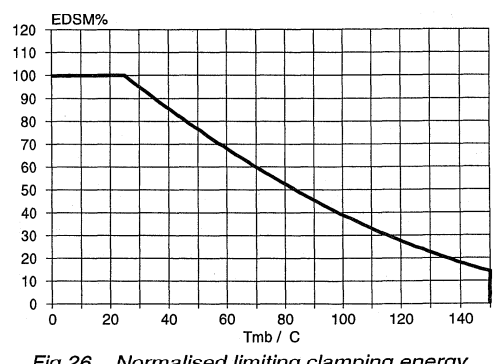


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; *conditions:* $I_D = 15$ *A*

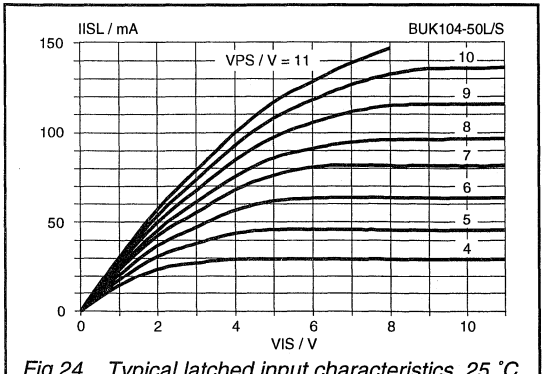


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; *after overload protection latched*

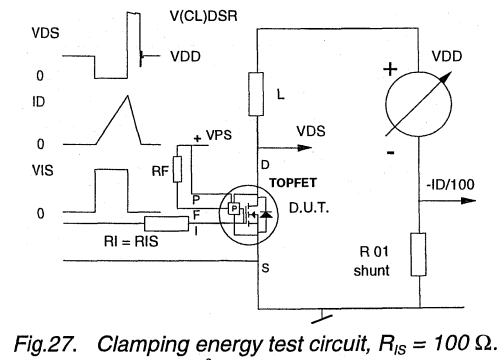


Fig.27. Clamping energy test circuit, $R_{IS} = 100\ \Omega$.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$$

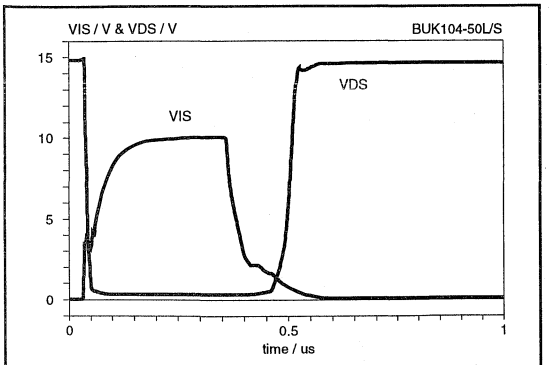


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

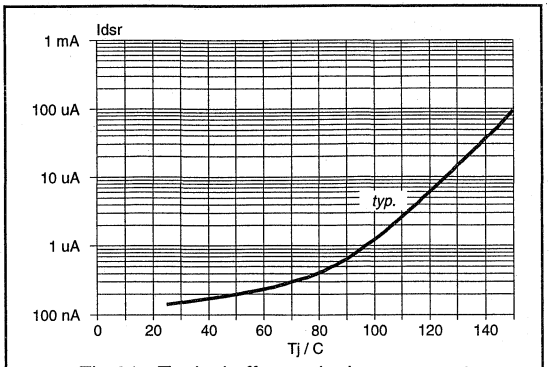


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

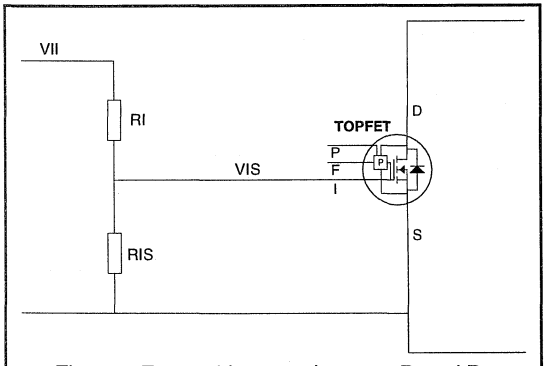


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

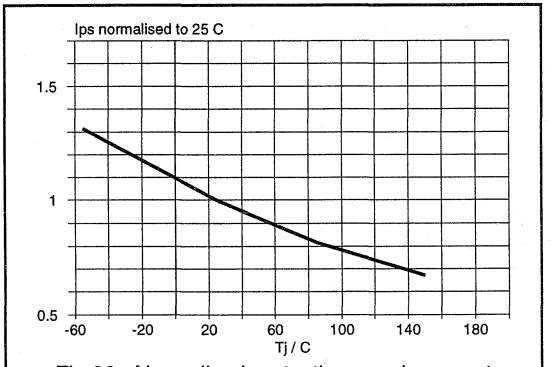


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ ^\circ C = f(T_j)$; $V_{PS} = V_{PSN}$

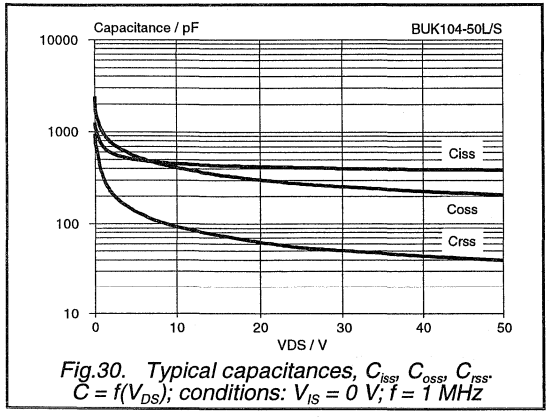


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor
Logic level TOPFET

BUK106-50L/S
BUK106-50LP/SP

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_{tot}	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	35	mΩ
	V_{IS} = 8 V	28	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK106-50L	5	V
	BUK106-50S	10	V

FUNCTIONAL BLOCK DIAGRAM

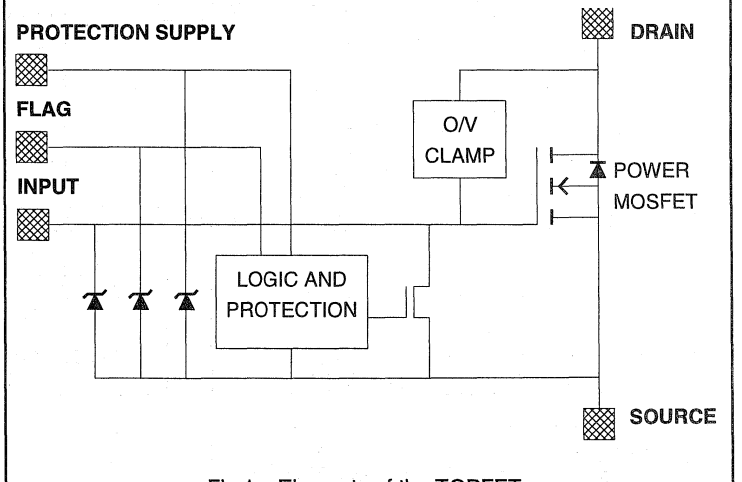


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

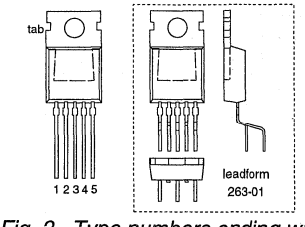


Fig. 2. Type numbers ending with suffix P refer to leadform 263-01.

SYMBOL

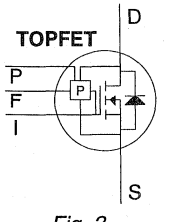


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
	Voltages					
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50		V
V_{IS}	Continuous input voltage	-	0	11		V
V_{FS}	Continuous flag voltage	-	0	11		V
V_{PS}	Continuous supply voltage	-	0	11		V
	Currents	V_{IS} =	-	8	5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	50	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	31	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	200	180	A
	Thermal					
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	-55	150		°C
T_j	Junction temperature[2]	continuous	-	150		°C
T_{sold}	Lead temperature	during soldering	-	250		°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.	UNIT
		V_{IS} =	8	5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection				
		BUK106-50L	4.4	4	-	V
		BUK106-50S	5.4	5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_l \geq 2$ kΩ	-		50	V
		V_{IS} = 5 V; $R_l \geq 1$ kΩ	-		50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_l \geq 2$ kΩ	-		24	V
		V_{IS} = 5 V; $R_l \geq 1$ kΩ	-		45	V
P_{DSM}	Instantaneous overload dissipation		-		4	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	50	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 27$ A; $R_{IS} \geq 100\ \Omega$	-	1	J
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	50	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 25$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$	$V_{IS} = 8$ V	-	22	28	mΩ
			$V_{IS} = 5$ V	-	28	35	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	550	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	0.4	-	ms
	Over temperature protection	$V_{PS} = V_{PSN}$				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 2.5$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 12$ V; $I_{DM} = 25$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	80	-	A
		$V_{IS} = 10$ V		160	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK106-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK106-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 20$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	0.9	1.2	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	10	-	ns
t_r	Rise time		-	35	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	280	-	ns
t_f	Fall time		-	120	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	1250	1800	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	650	1000	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	150	250	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK106-50L	2.5	3.3	4	V
		BUK106-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

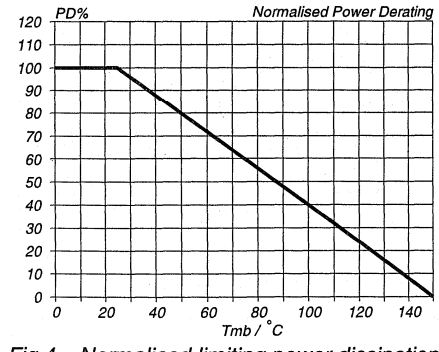


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

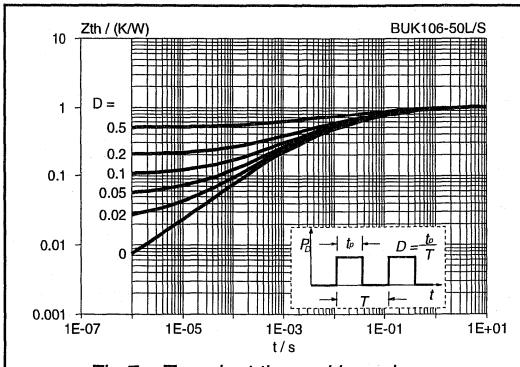


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

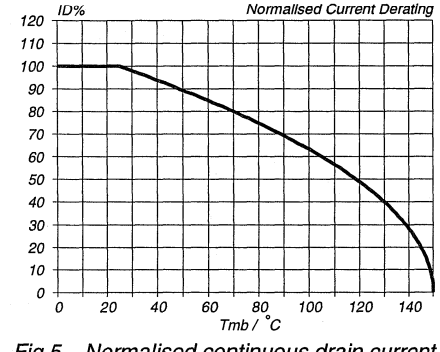


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

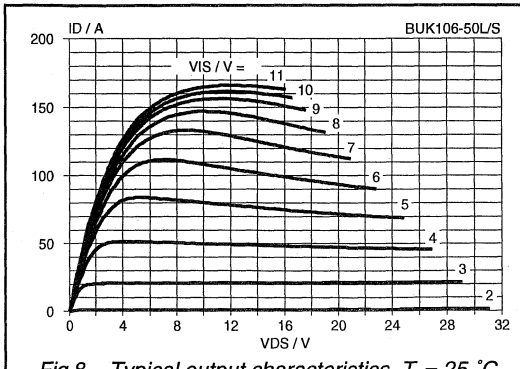


Fig.8. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

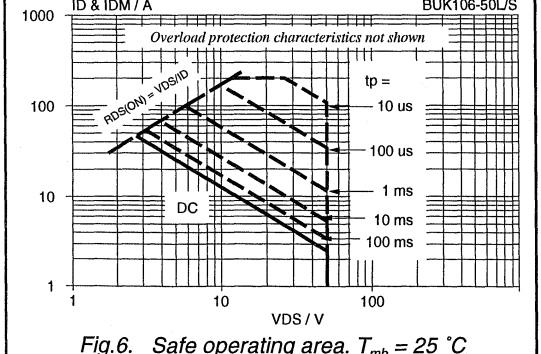


Fig.6. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

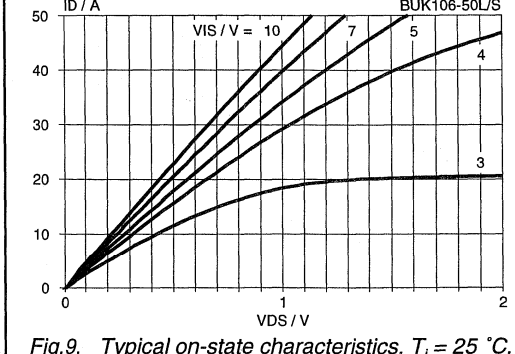


Fig.9. Typical on-state characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

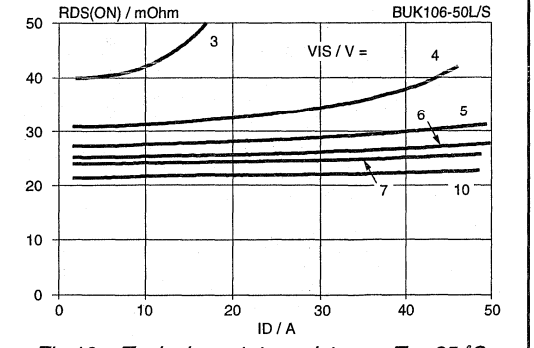


Fig.10. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

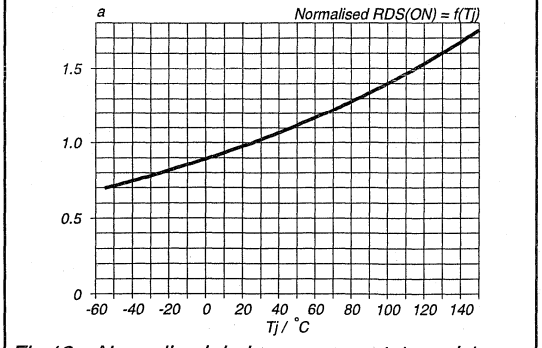


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 25 A; $V_{IS} \geq 5$ V

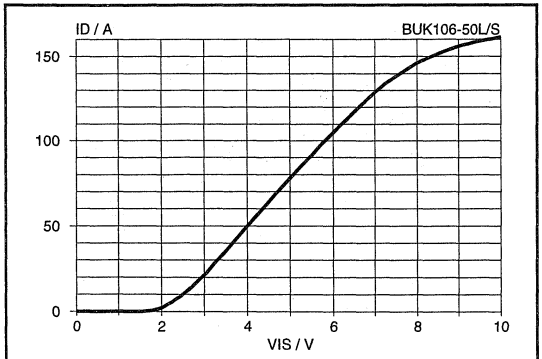


Fig.11. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 12 V; t_p = 250 µs

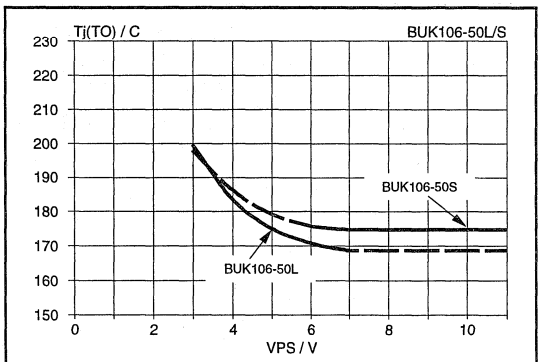


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

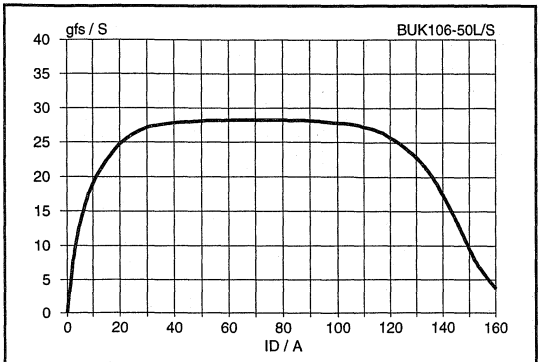


Fig.12. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 12 V; t_p = 250 µs

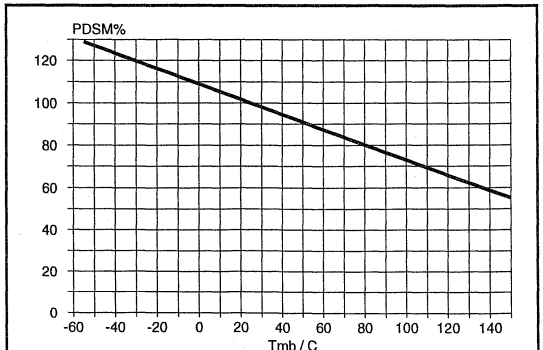


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

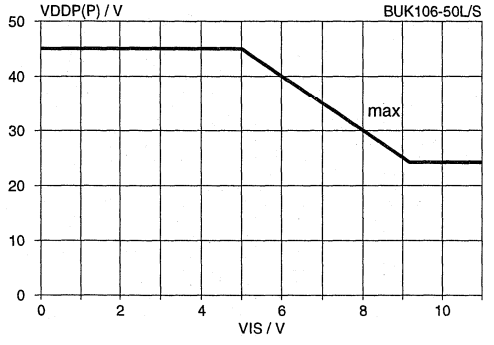


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

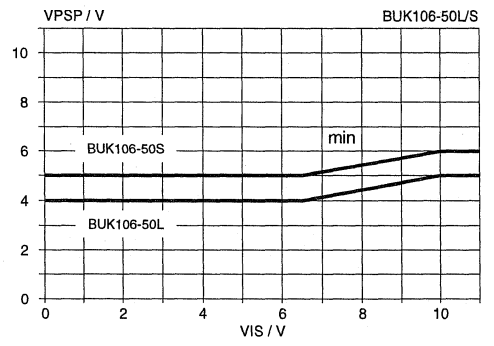


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

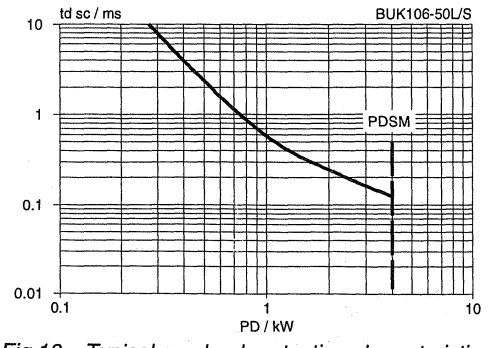


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

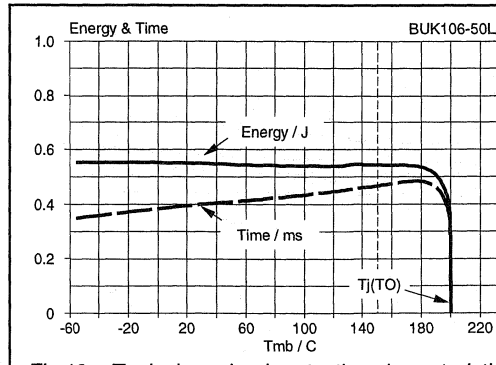


Fig.19. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{PS} = V_{PSN}$, $V_{IS} = 8$ V; SC load

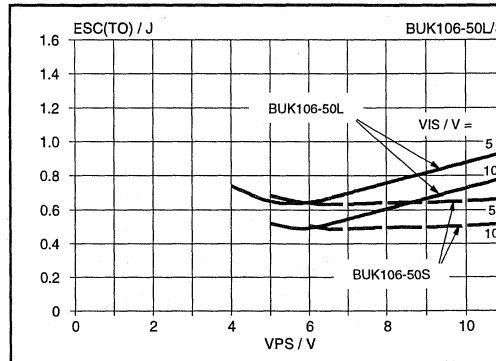


Fig.20. Typical overload protection energy, $T_j = 25$ °C $E_{SC(TO)} = f(V_{PS})$; conditions: $V_{DS} = 13$ V, parameter V_{IS}

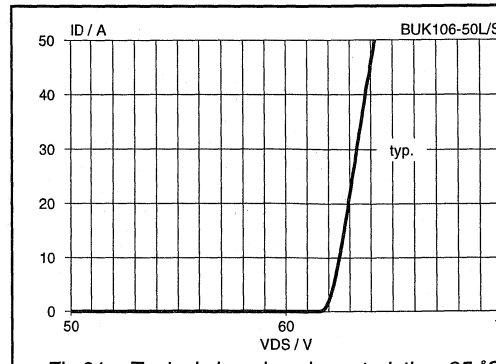


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $R_{IS} = 100\ \Omega$; $t_p \leq 50\ \mu$s

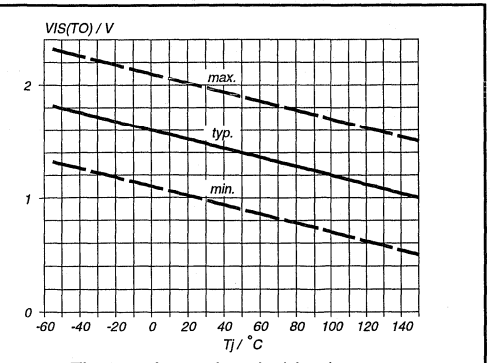


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

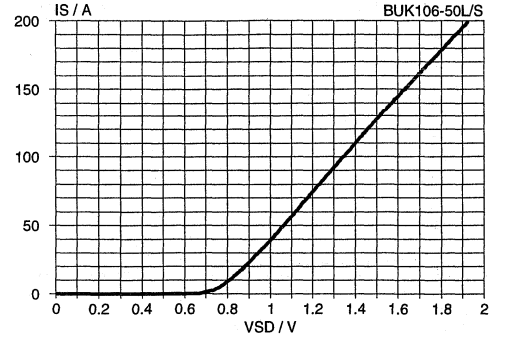


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

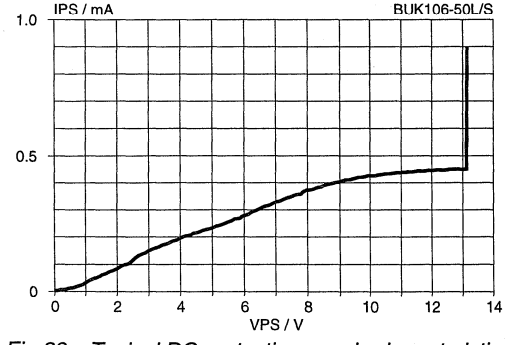


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

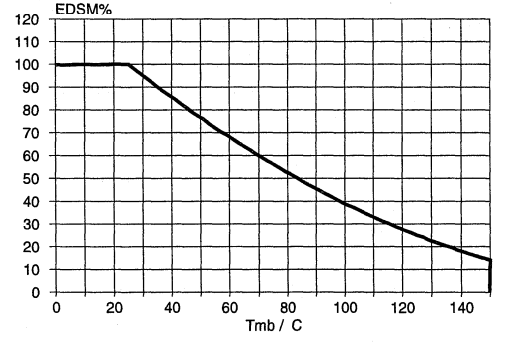


Fig.26. Normalised limiting clamping energy.
E_{DSM}% = $f(T_{mb})$; conditions: I_D = 27 A

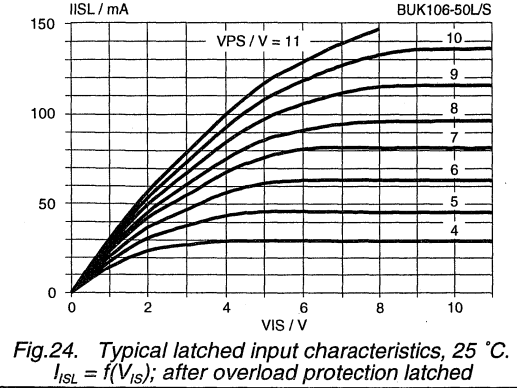


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

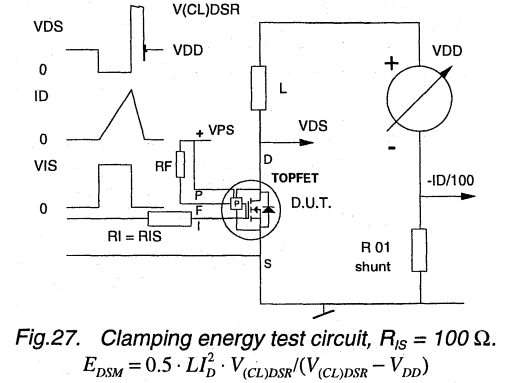


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$$

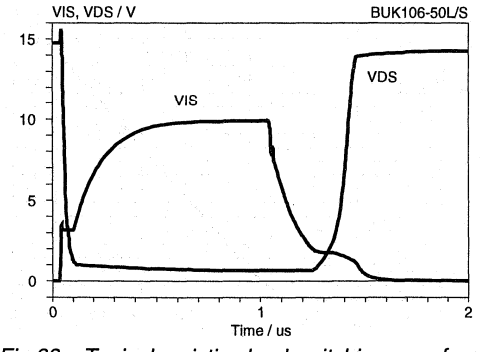


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

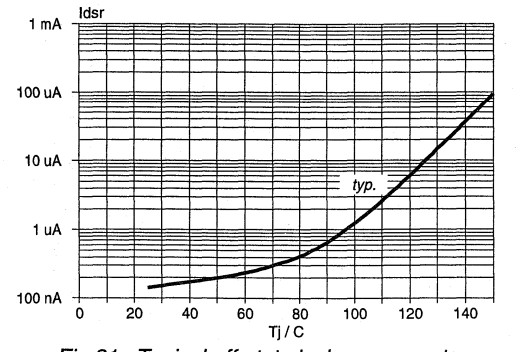


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

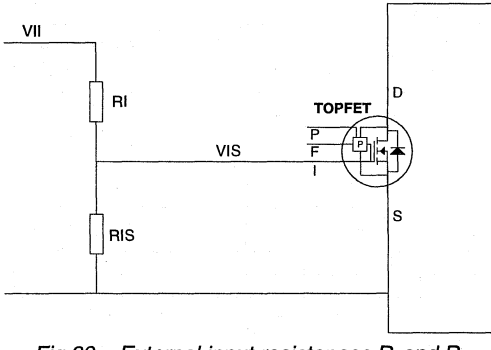


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

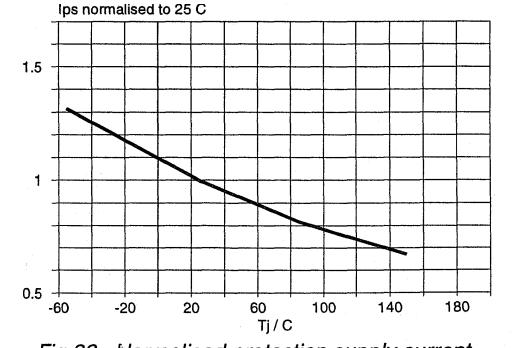


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ ^\circ C = f(T_j)$; $V_{PS} = V_{PSN}$

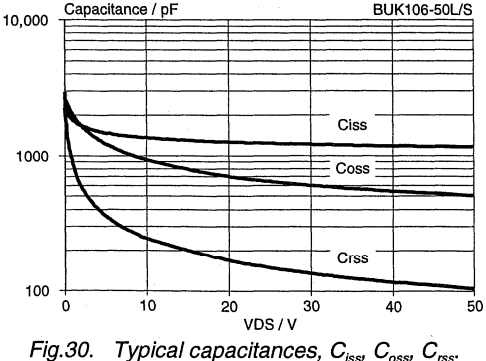


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor Logic level TOPFET

BUK107-50DL

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85˚C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	0.7	A
P_D	Total power dissipation	1.8	W
T_j	Continuous junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

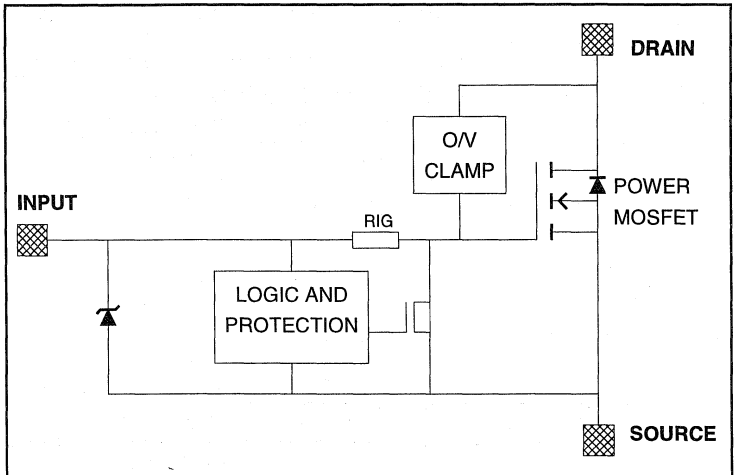
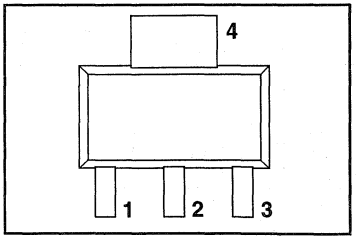


Fig.1. Elements of the TOPFET.

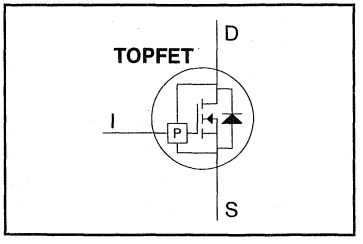
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current[2]	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{amb} = 25$ °C	-	1.8	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature	normal operation[3]	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[4]	for valid protection	4	-	V
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	$V_{IS} = 5$ V	0.7	1.1	1.5	A
	Overtemperature protection	only in drain current limiting				
$T_{j(TO)}$	Threshold junction temperature	$V_{IS} = 5$ V	100	130	160	°C

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 **Not** in an overload condition with drain current limiting.

4 The input voltage for which the overload protection circuits are functional.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}b}$	Junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	Mounted on PCB of fig. 19	-	-	70	K/W

STATIC CHARACTERISTICS

T_b = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 200 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	V_{DS} = 45 V; V_{IS} = 0 V	-	0.5	2	µA
I_{DSS}	Off-state drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Off-state drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 100 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[2]	V_{IS} = 5 V; I_{DM} = 100 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	150	200	mΩ

INPUT CHARACTERISTICS

T_b = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	-	330	450	µA
			V_{IS} = 4 V	-	170	270	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	500	650	µA
			V_{IS} = 3.5 V	-	250	400	µA
V_{ISR}	Protection latch reset voltage[3]			1	2.2	3.5	V
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET		-	33	-	kΩ

SWITCHING CHARACTERISTICS

T_{amb} = 25 °C; resistive load R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	V_{IS} = 0 V to V_{IS} = 5 V	-	8	-	µs
t_r	Rise time		-	30	-	µs
$t_{d\ off}$	Turn-off delay time	V_{IS} = 5 V to V_{IS} = 0 V	-	3	-	µs
t_f	Fall time		-	6	-	µs

1 Temperature measured 1.3 mm from tab.

2 Continuous input voltage. The specified pulse width is for the drain current.

3 The input voltage below which the overload protection circuits will be reset.

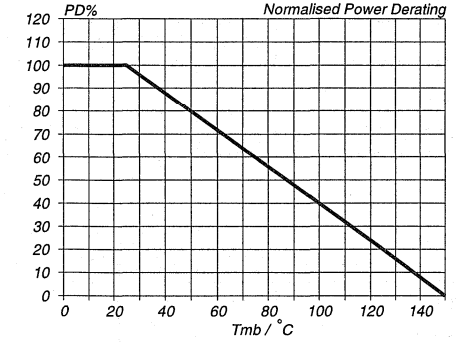


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

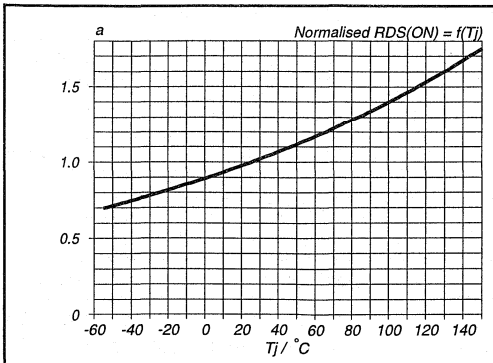


Fig.5. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; $I_D = 100$ mA; $V_{IS} = 5$ V

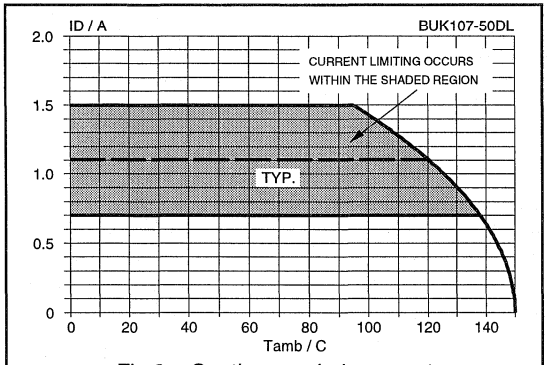


Fig.3. Continuous drain current.
$I_D = f(T_{amb})$; condition: $V_{IS} = 5$ V

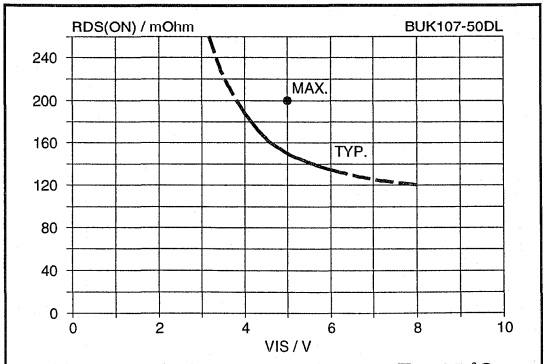


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(V_{IS})$; conditions: $I_D = 100$ mA, $t_p = 300\ \mu s$

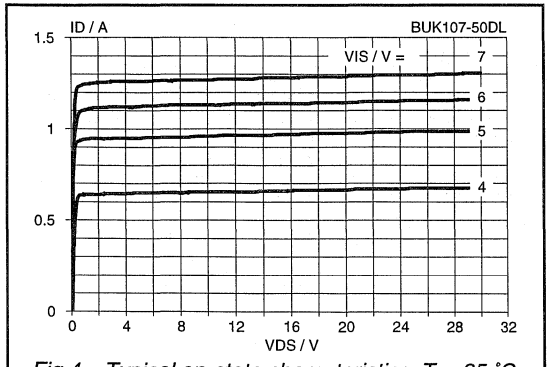


Fig.4. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 300\ \mu s$

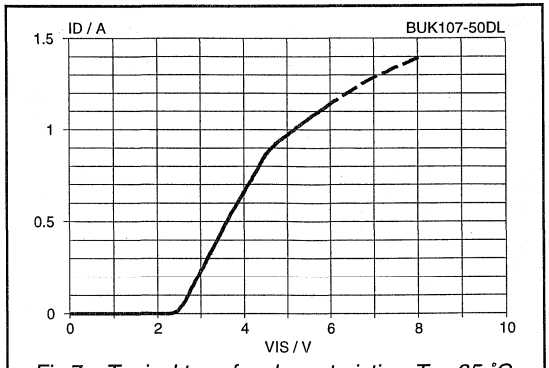


Fig.7. Typical transfer characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{IS})$; conditions: $V_{DS} = 10$ V, $t_p = 300\ \mu s$

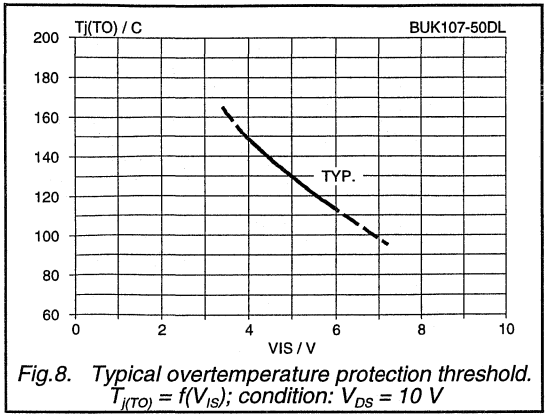


Fig.8. Typical overtemperature protection threshold. $T_{j(TO)} = f(V_{IS})$; condition: V_{DS} = 10 V

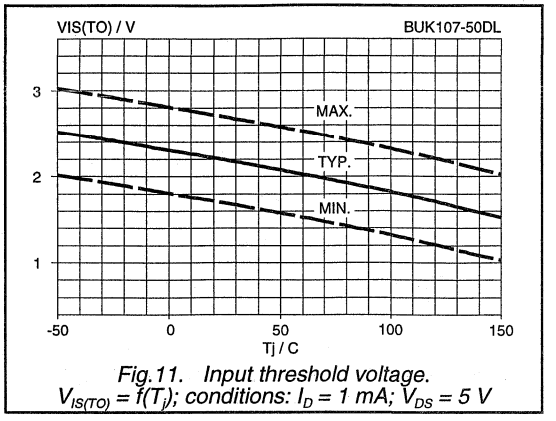


Fig.11. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

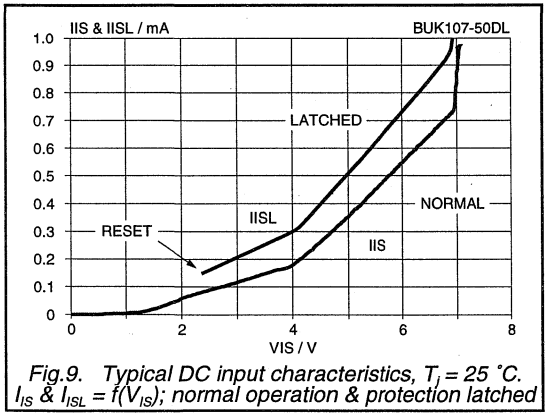


Fig.9. Typical DC input characteristics, T_j = 25 °C. I_{IS} & $I_{ISL} = f(V_{IS})$; normal operation & protection latched

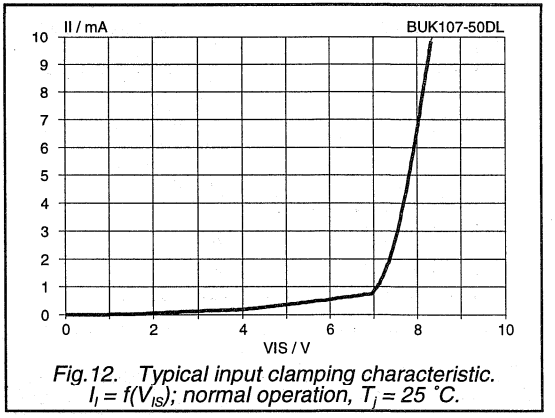


Fig.12. Typical input clamping characteristic. $I_I = f(V_{IS})$; normal operation, T_j = 25 °C.

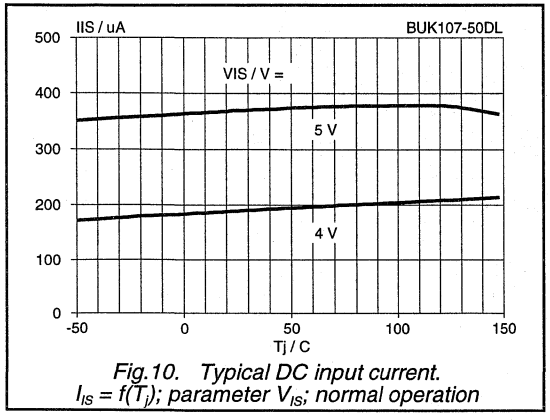


Fig.10. Typical DC input current. $I_{IS} = f(T_j)$; parameter V_{IS}; normal operation

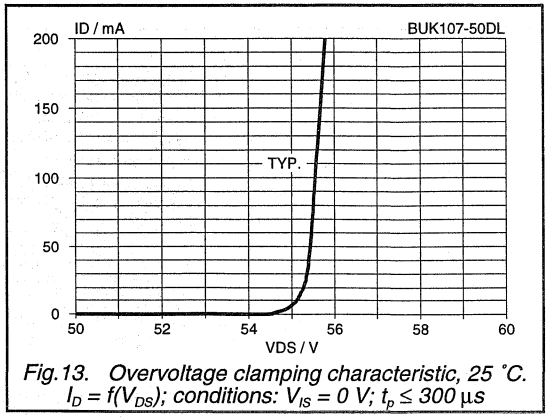


Fig.13. Overvoltage clamping characteristic, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 300$ µs

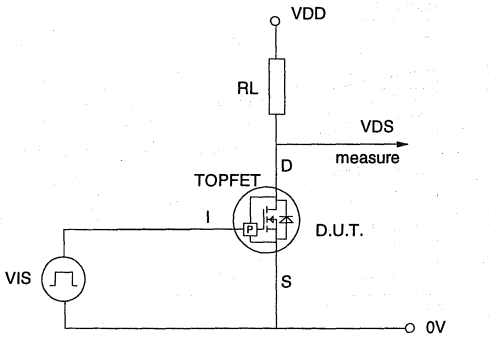


Fig.14. Test circuit for resistive load switching times. V_{IS} = 5 V

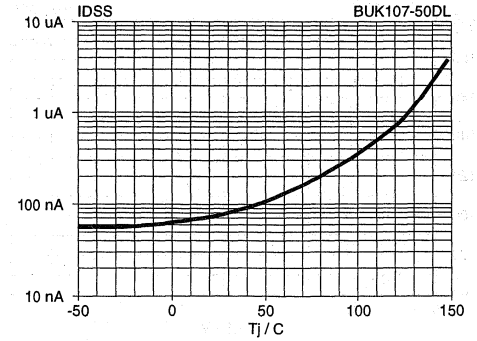


Fig.16. Typical drain source leakage current $I_{DSS} = f(T_j)$; conditions: V_{DS} = 40 V; V_{IS} = 0 V.

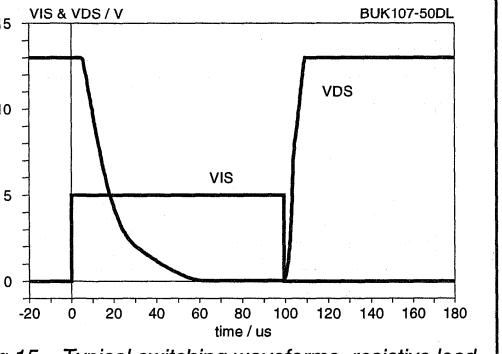


Fig.15. Typical switching waveforms, resistive load. R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; T_j = 25˚C

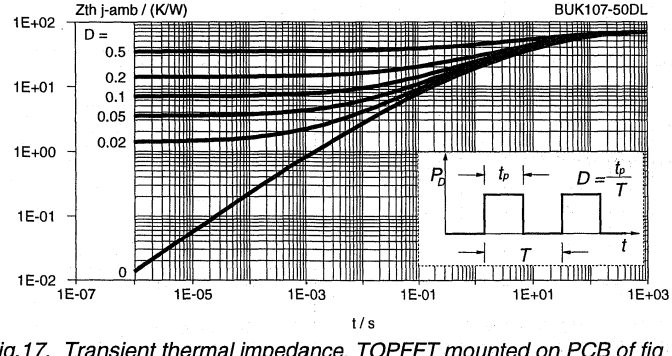


Fig.17. Transient thermal impedance, TOPFET mounted on PCB of fig 19. $Z_{th\ j\text{-}amb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor
Logic level TOPFET

BUK107-50DS

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85˚C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- Input clamping suitable for pull-up resistor drive circuit
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	0.7	A
P_D	Total power dissipation	1.8	W
T_j	Continuous junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance	175	mΩ

FUNCTIONAL BLOCK DIAGRAM

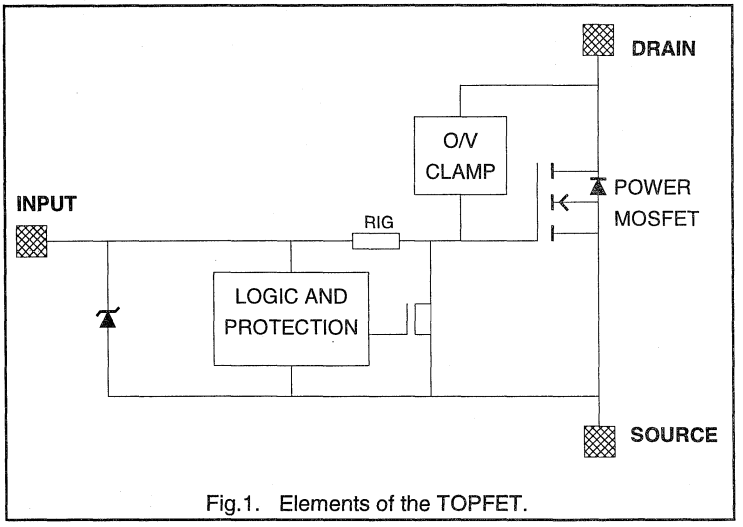
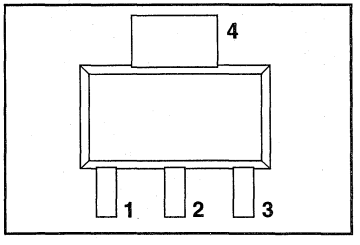


Fig.1. Elements of the TOPFET.

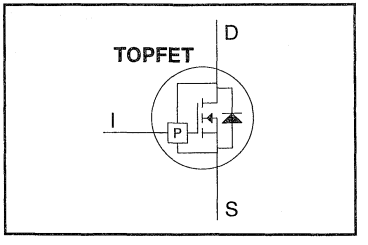
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current[2]	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{amb} = 25$ °C	-	1.8	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature	normal operation[3]	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[4]	for valid protection	6	-	V
V_{DDP}	Protected drain source supply voltage	$I_I = 1.5$ mA	-	35	V

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	$I_I = 1.5$ mA	0.7	1.1	1.5	A
	Overtemperature protection	only in drain current limiting				
$T_{j(TO)}$	Threshold junction temperature	$I_I = 1.5$ mA	100	130	160	°C

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 **Not** in an overload condition with drain current limiting.

4 The input voltage for which the overload protection circuits are functional.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}b}$	Junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	Mounted on PCB of fig. 19	-	-	70	K/W

STATIC CHARACTERISTICS

T_b = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 200 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	V_{DS} = 45 V; V_{IS} = 0 V	-	0.5	2	µA
I_{DSS}	Off-state drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Off-state drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 100 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[2]	I_I = 1.5 mA; I_{DM} = 100 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	125	175	mΩ

INPUT CHARACTERISTICS

T_b = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input. The input clamping is suitable for a drive circuit with a pull-up resistor.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 6 V	-	550	750	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	500	650	µA
			V_{IS} = 3.5 V	-	250	400	µA
V_{ISR}	Protection latch reset voltage[3]			1	2.2	3.5	V
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET		-	33	-	kΩ

SWITCHING CHARACTERISTICS

T_{amb} = 25 °C; resistive load R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	V_{IS} = 0 V to I_I = 1.5 mA	-	4	-	µs
t_r	Rise time		-	16	-	µs
$t_{d\ off}$	Turn-off delay time	I_I = 1.5 mA to V_{IS} = 0 V	-	3	-	µs
t_f	Fall time		-	6	-	µs

1 Temperature measured 1.3 mm from tab.

2 Continuous input voltage. The specified pulse width is for the drain current.

3 The input voltage below which the overload protection circuits will be reset.

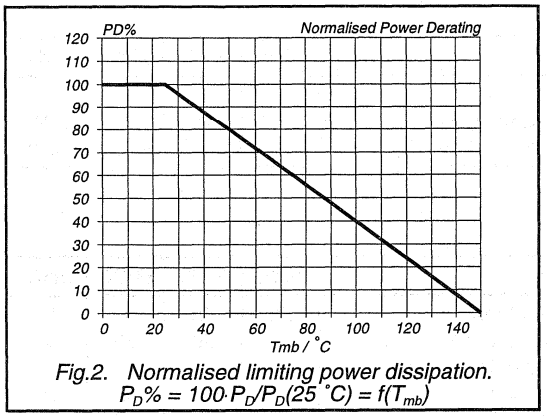


Fig.2. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

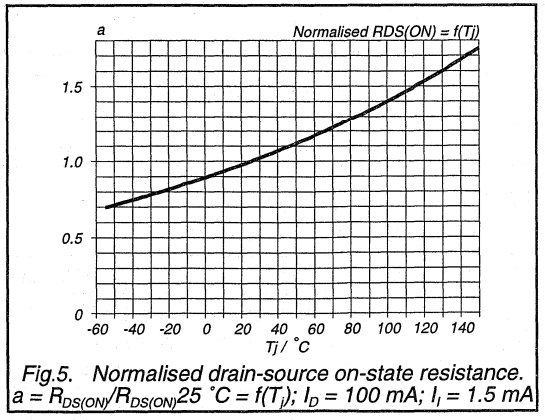


Fig.5. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; I_D = 100 mA; I_l = 1.5 mA

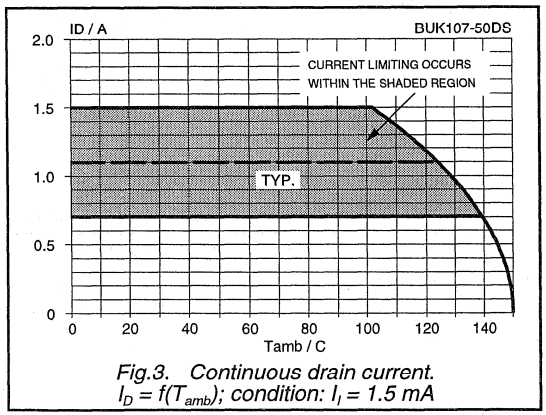


Fig.3. Continuous drain current. $I_D = f(T_{amb})$; condition: I_l = 1.5 mA

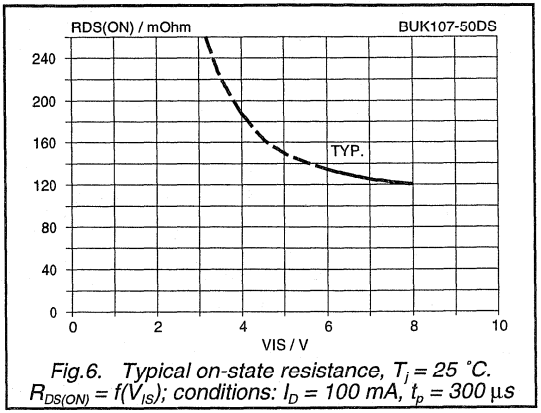


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(V_{IS})$; conditions: I_D = 100 mA, t_p = 300 µs

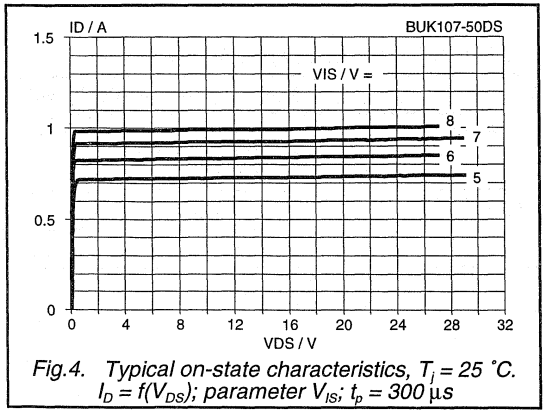


Fig.4. Typical on-state characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{IS}; t_p = 300 µs

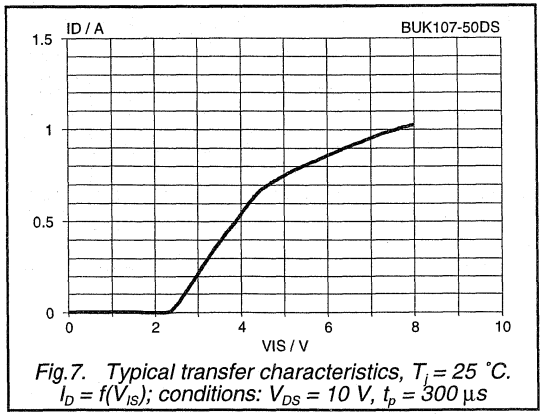


Fig.7. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V, t_p = 300 µs

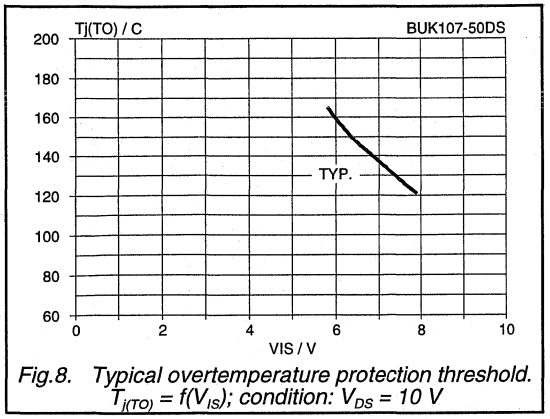


Fig.8. Typical overtemperature protection threshold. $T_{j(TO)} = f(V_{IS})$; condition: V_{DS} = 10 V

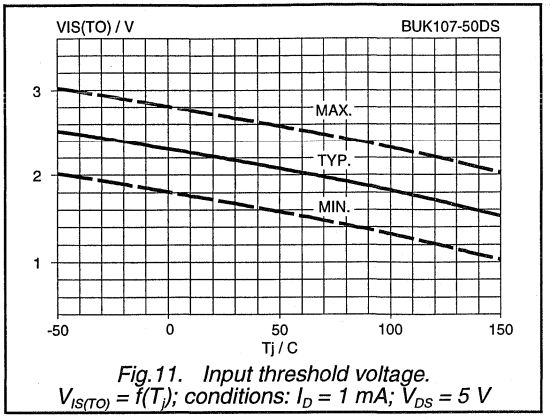


Fig.11. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

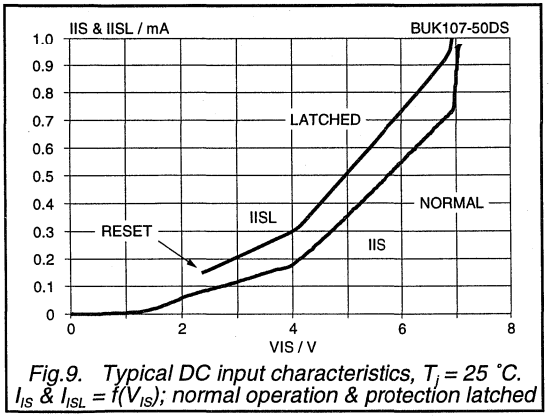


Fig.9. Typical DC input characteristics, T_j = 25 ˚C. I_{IS} & $I_{ISL} = f(V_{IS})$; normal operation & protection latched

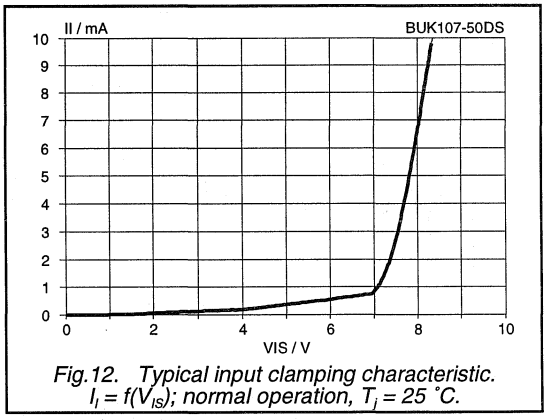


Fig.12. Typical input clamping characteristic. $I_I = f(V_{IS})$; normal operation, T_j = 25 ˚C.

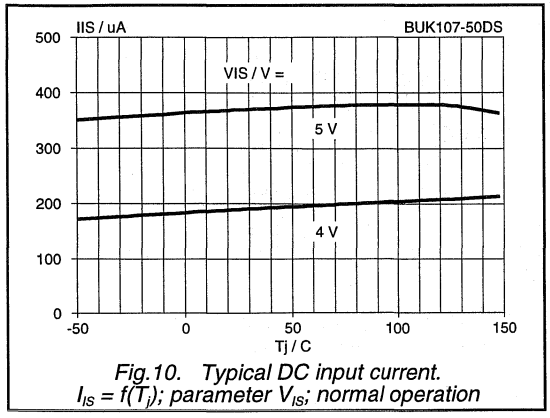


Fig.10. Typical DC input current. $I_{IS} = f(T_j)$; parameter V_{IS}; normal operation

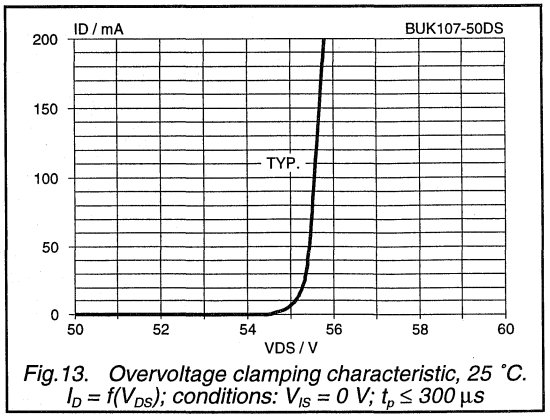


Fig.13. Overvoltage clamping characteristic, 25 ˚C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 300$ µs

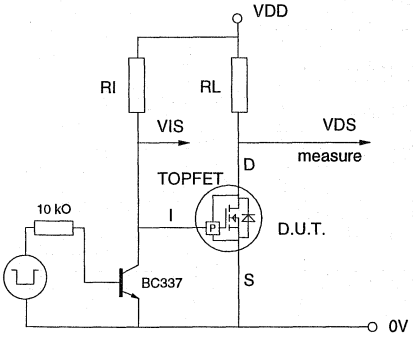


Fig.14. Test circuit for resistive load switching times. Select R_I to give I_I = 1.5 mA, ie 3.3 kΩ approx.

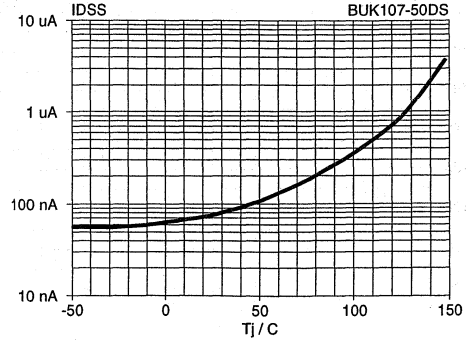


Fig.16. Typical drain source leakage current $I_{DSS} = f(T_j)$; conditions: V_{DS} = 40 V; V_{IS} = 0 V.

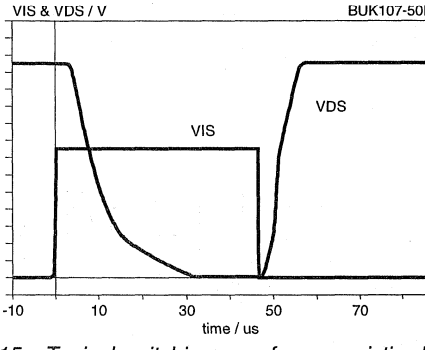


Fig.15. Typical switching waveforms, resistive load. R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; T_j = 25°C

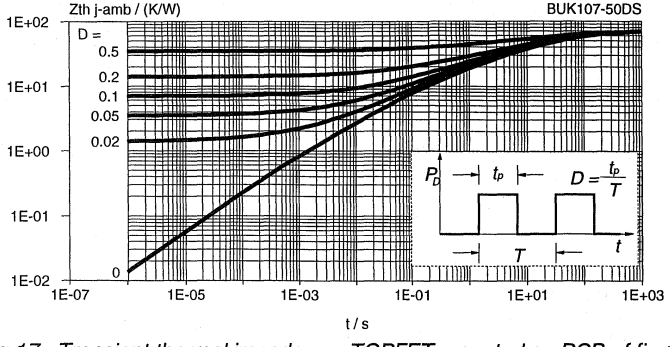


Fig.17. Transient thermal impedance, TOPFET mounted on PCB of fig 19. $Z_{th\ j\text{-}amb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor Logic level TOPFET

BUK107-50GL

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85˚C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	0.7	A
P_D	Total power dissipation	1.8	W
T_j	Continuous junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

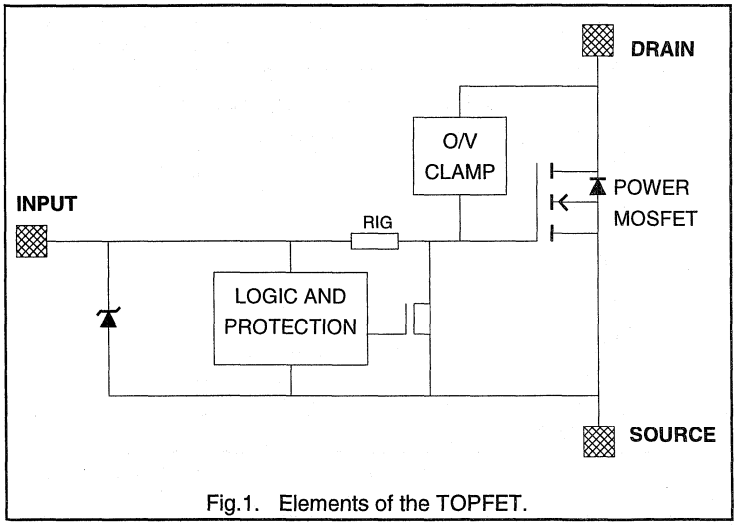
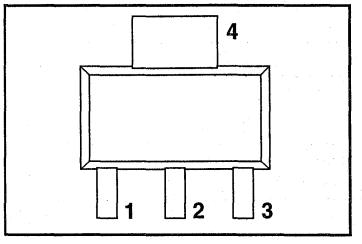


Fig.1. Elements of the TOPFET.

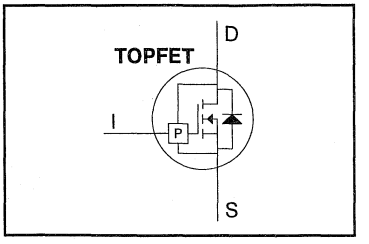
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current[2]	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{amb} = 25$ °C	-	1.8	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature	normal operation[3]	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[4]	for valid protection	4	-	V
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	$V_{IS} = 5$ V	0.7	1.1	1.5	A
	Overtemperature protection	only in drain current limiting				
$T_{j(TO)}$	Threshold junction temperature	$V_{IS} = 5$ V	100	130	160	°C

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 **Not** in an overload condition with drain current limiting.

4 The input voltage for which the overload protection circuits are functional.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}t}$	Junction to tab (pin 4)		-	12	18	K/W
$R_{th\ j\text{-}b}$	Junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	Mounted on PCB of fig. 19	-	-	70	K/W

STATIC CHARACTERISTICS

T_b = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 200 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	V_{DS} = 45 V; V_{IS} = 0 V	-	0.5	2	µA
I_{DSS}	Off-state drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Off-state drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 100 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 100 mA; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	-	150	200	mΩ

INPUT CHARACTERISTICS

T_b = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	-	330	450	µA
			V_{IS} = 4 V	-	170	270	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	1.45	2	mA
			V_{IS} = 3.5 V	-	0.95	1.3	mA
V_{ISR}	Protection latch reset voltage[2]			1	2.7	3.5	V
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET		-	4.5	-	kΩ

1 Temperature measured 1.3 mm from tab.

2 The input voltage below which the overload protection circuits will be reset.

SWITCHING CHARACTERISTICS

T_{amb} = 25 °C; resistive load R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{IS} = 0 V to V_{IS} = 5 V	-	0.9	-	µs
t_r	Rise time		-	3.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS} = 5 V to V_{IS} = 0 V	-	2.8	-	µs
t_f	Fall time		-	9.0	-	µs

T_{amb} = 25 °C; resistive load R_L = 10 kΩ; V_{DD} = 12.5 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{IS} = 0 V to V_{IS} = 5 V	-	0.8	-	µs
t_r	Rise time		-	2.3	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS} = 5 V to V_{IS} = 0 V	-	7.5	-	µs
t_f	Fall time		-	12.5	-	µs

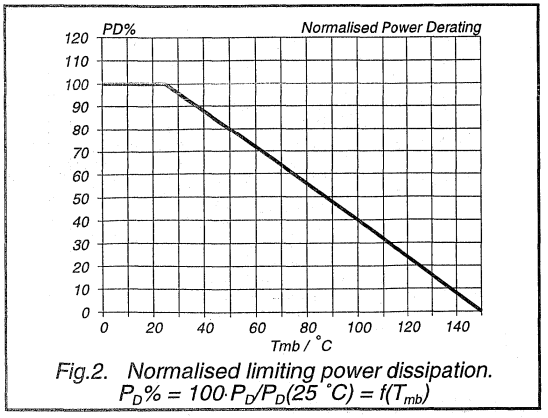


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

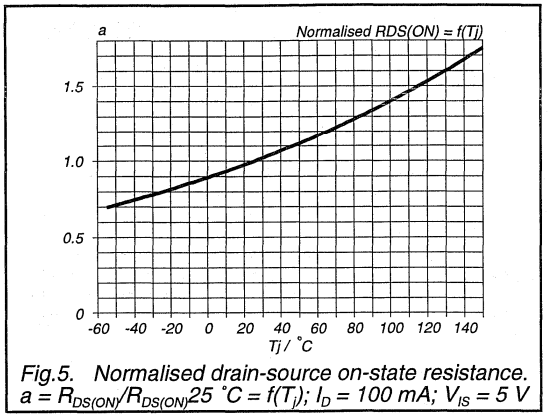


Fig.5. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; I_D = 100 mA; V_{IS} = 5 V

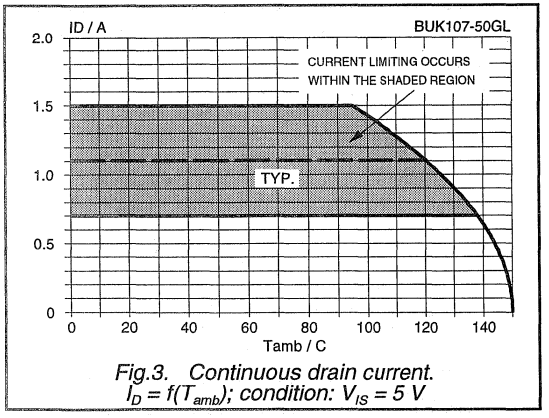


Fig.3. Continuous drain current.
$I_D = f(T_{amb})$; condition: V_{IS} = 5 V

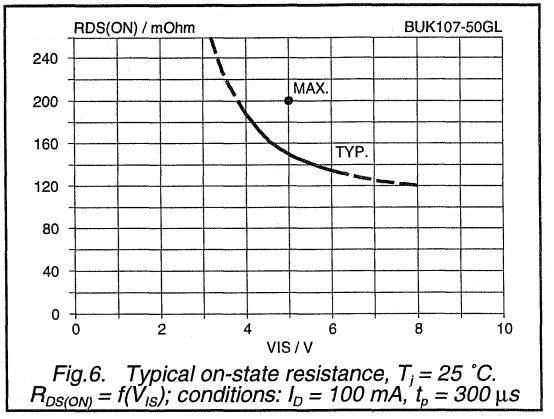


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)} = f(V_{IS})$; conditions: I_D = 100 mA, t_p = 300 µs

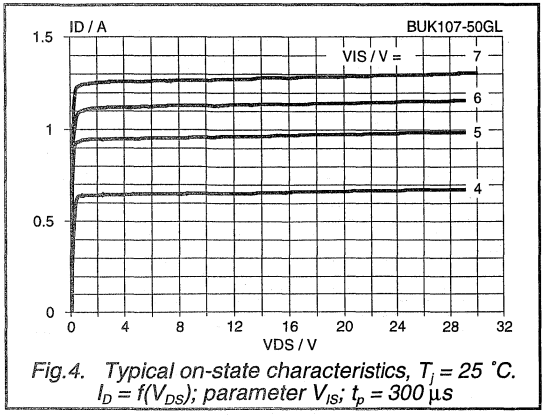


Fig.4. Typical on-state characteristics, T_j = 25 °C.
$I_D = f(V_{DS})$; parameter V_{IS}; t_p = 300 µs

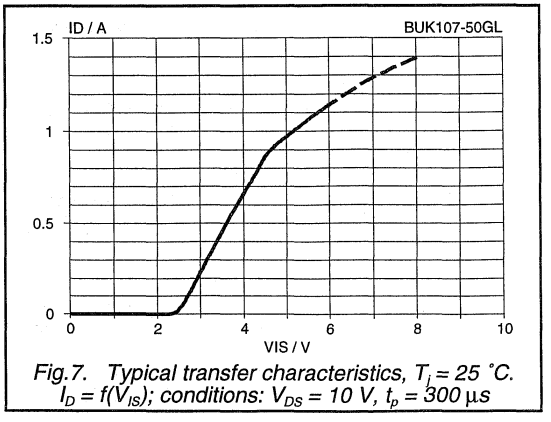


Fig.7. Typical transfer characteristics, T_j = 25 °C.
$I_D = f(V_{IS})$; conditions: V_{DS} = 10 V, t_p = 300 µs

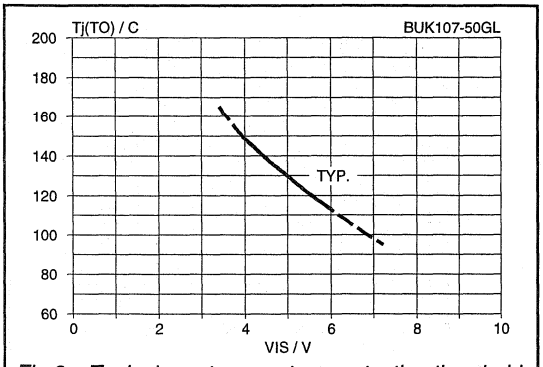


Fig.8. Typical overtemperature protection threshold. $T_{j(TO)} = f(V_{IS})$; condition: V_{DS} = 10 V

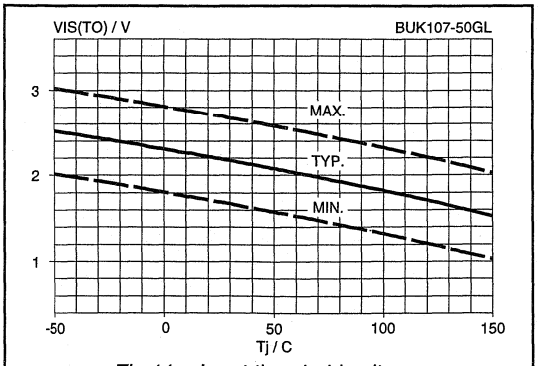


Fig.11. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

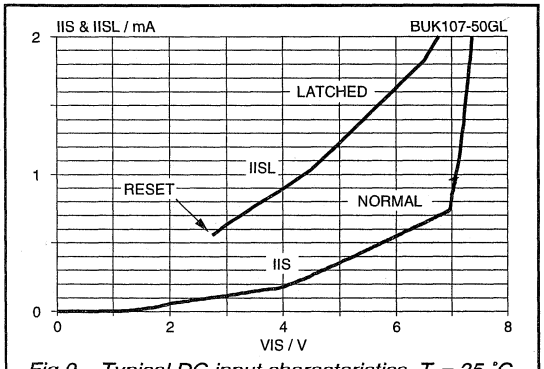


Fig.9. Typical DC input characteristics, T_j = 25 °C. I_{IS} & $I_{ISL} = f(V_{IS})$; normal operation & protection latched

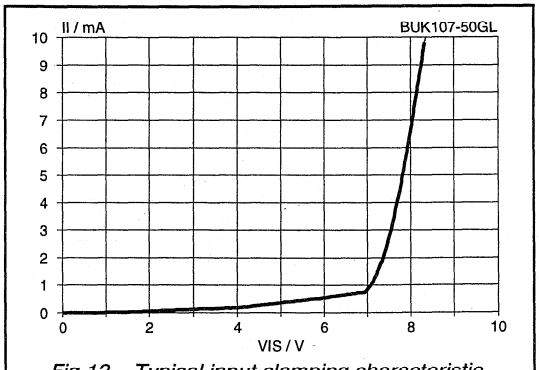


Fig.12. Typical input clamping characteristic. $I_I = f(V_{IS})$; normal operation, T_j = 25 °C.

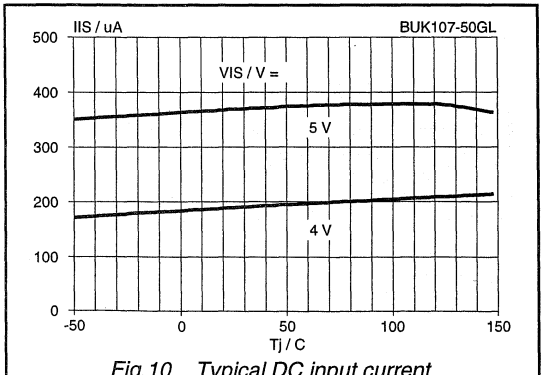


Fig.10. Typical DC input current. $I_{IS} = f(T_j)$; parameter V_{IS}; normal operation

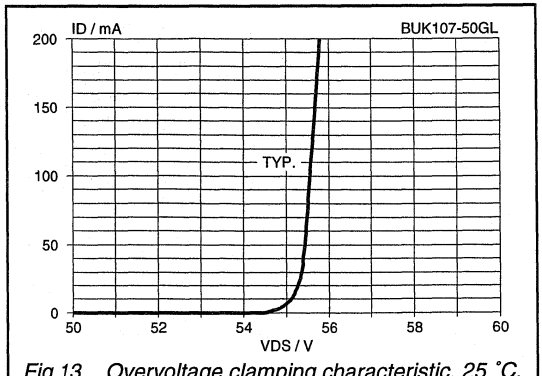


Fig.13. Overvoltage clamping characteristic, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 300$ µs

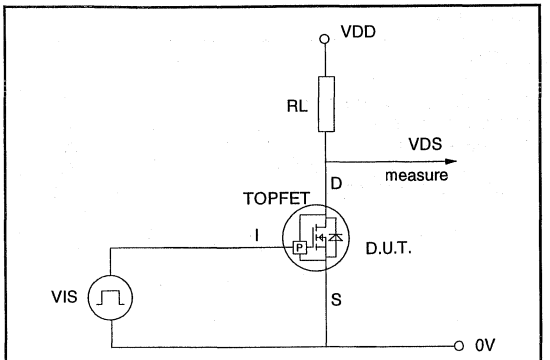


Fig.14. Test circuit for resistive load switching times. V_{IS} = 5 V

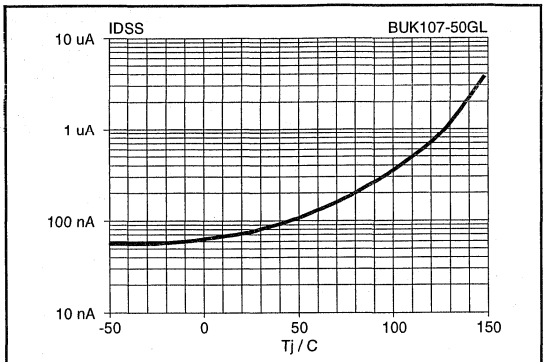


Fig.16. Typical drain source leakage current $I_{DSS} = f(T_j)$; conditions: V_{DS} = 40 V; V_{IS} = 0 V.

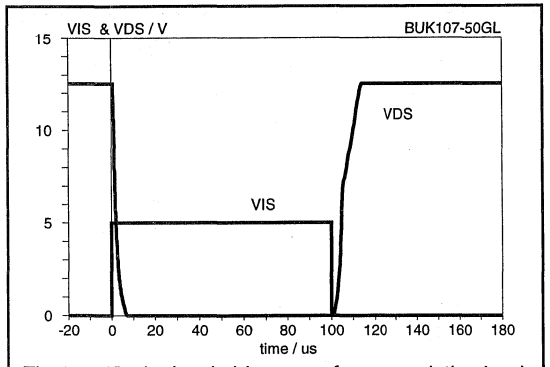


Fig.15. Typical switching waveforms, resistive load . R_L = 50 Ω; adjust V_{DD} to obtain I_D = 250 mA; T_j = 25˚C

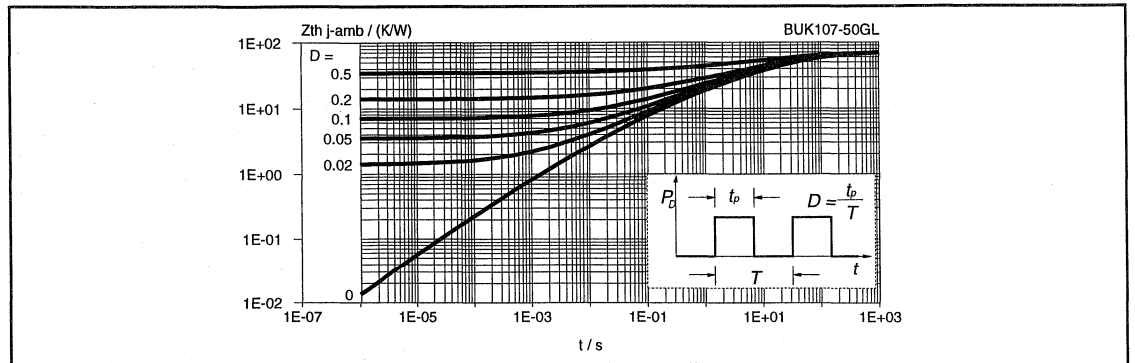


Fig.17. Transient thermal impedance, TOPFET mounted on PCB of fig 19. $Z_{th\ j\text{-}amb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor Logic level TOPFET

BUK108-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		13.5	A
P_D	Total power dissipation		40	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		125	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	µA

FUNCTIONAL BLOCK DIAGRAM

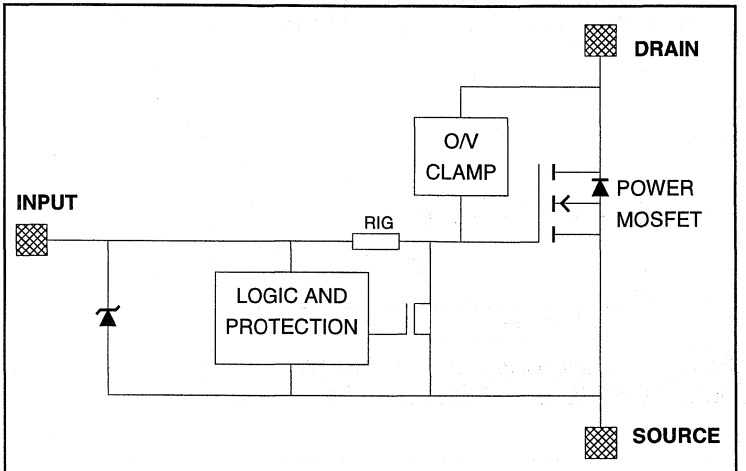
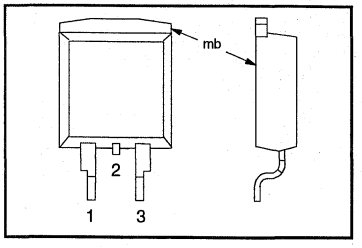


Fig.1. Elements of the TOPFET.

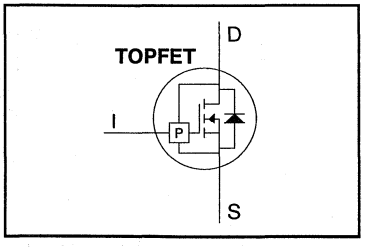
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	24	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 15$ A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 23)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	25	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	60	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 0.5$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	8	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	40	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	40	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	35	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	15	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

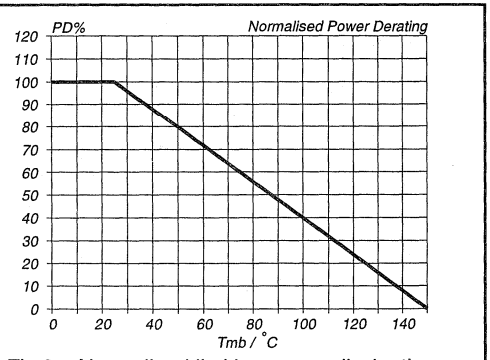


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

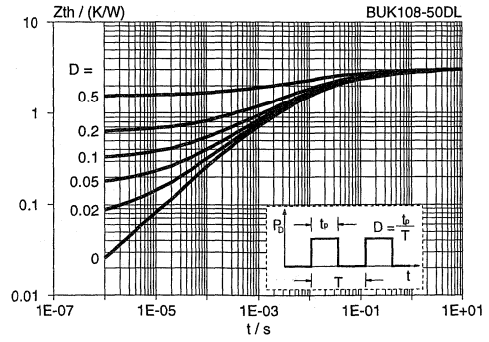


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

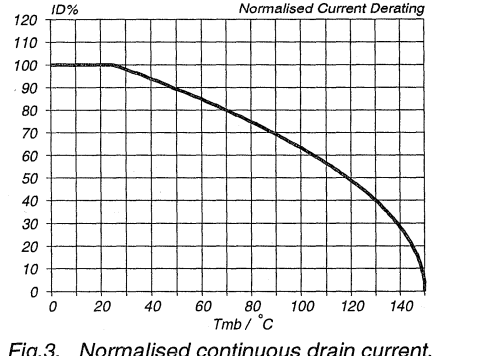


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

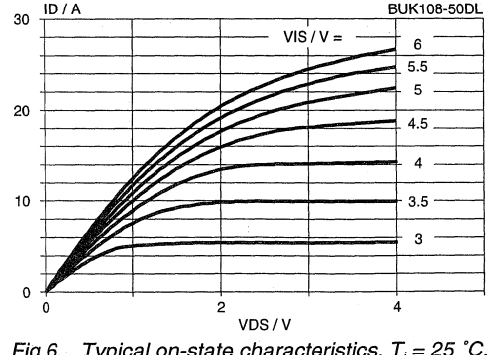


Fig.6. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 2$ ms

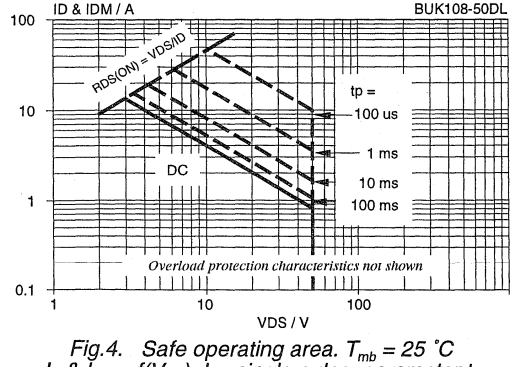


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

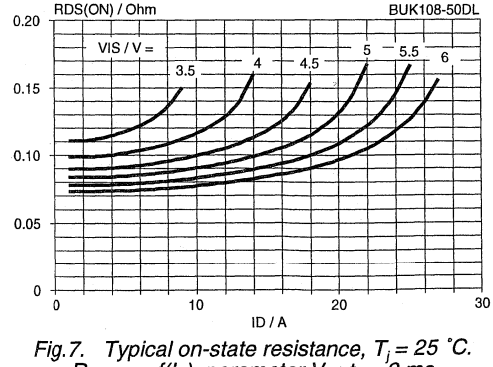


Fig.7. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{IS}; $t_p = 2$ ms

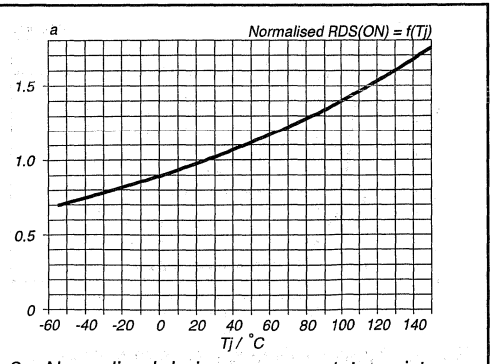


Fig.8. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^{\circ}C = f(T_j)$; $I_D = 7.5$ A; $V_{IS} = 5$ V

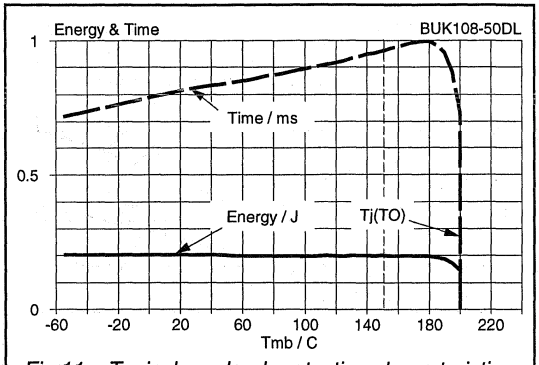


Fig.11. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{IS} = 5$ V; SC load = 30 mΩ

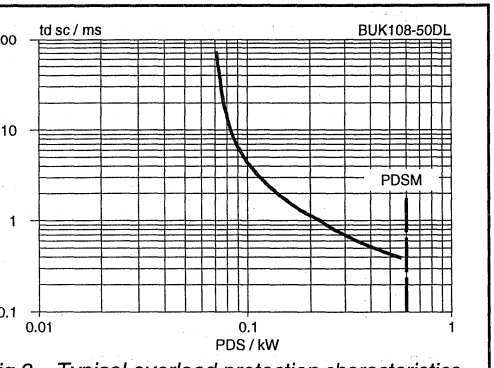


Fig.9. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; $T_j = 25\ ^{\circ}C$.

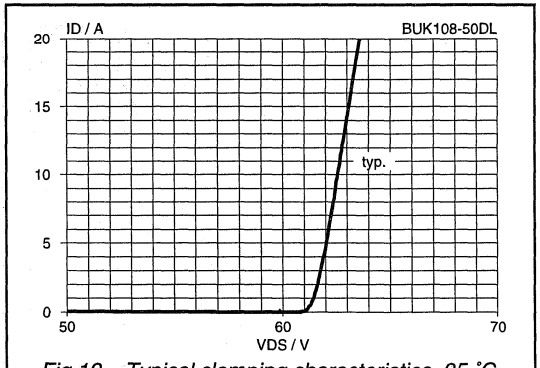


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

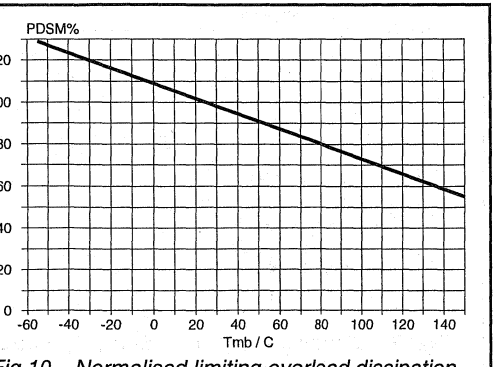


Fig.10. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^{\circ}C) = f(T_{mb})$

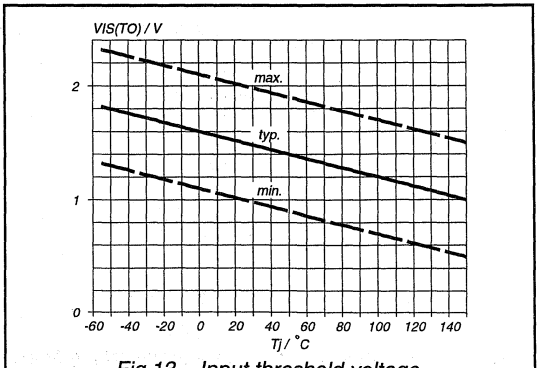


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

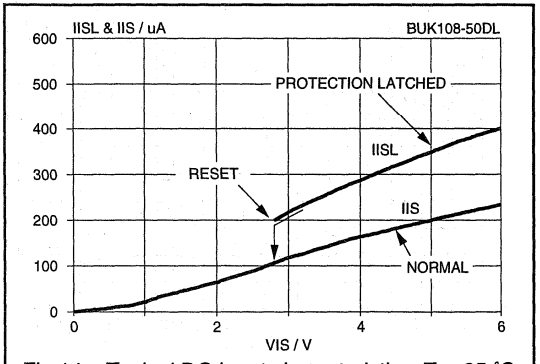


Fig.14. Typical DC input characteristics, T_j = 25 °C. I_{ISL} & I_{IS} = f(V_{IS}); protection latched & normal operation

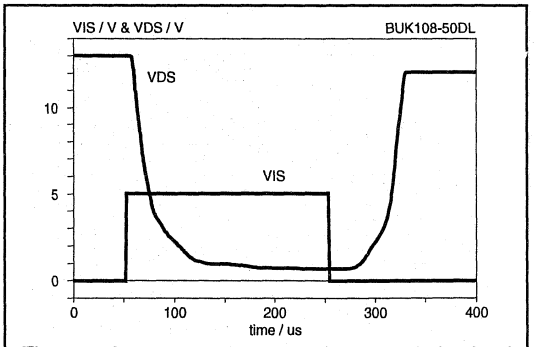


Fig.17. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

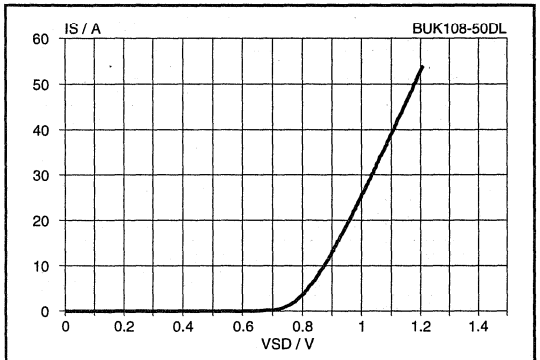


Fig.15. Typical reverse diode current, T_j = 25 °C. I_S = f(V_{SDS}); conditions: V_{IS} = 0 V; t_p = 250 µs

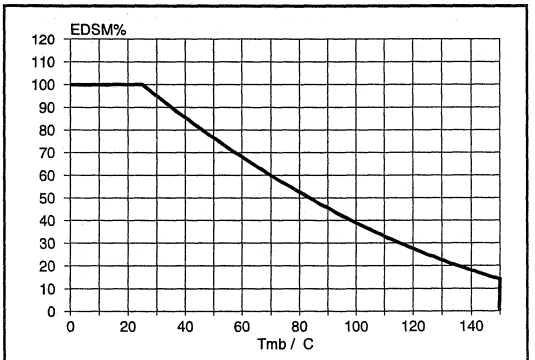


Fig.18. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 15 A; V_{IS} = 5 V

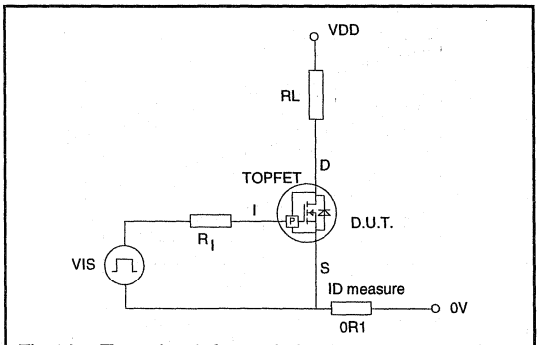


Fig.16. Test circuit for resistive load switching times.

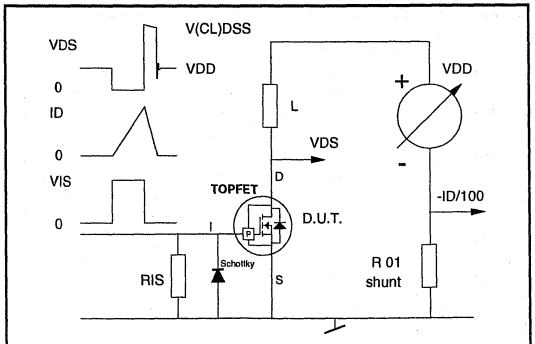


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

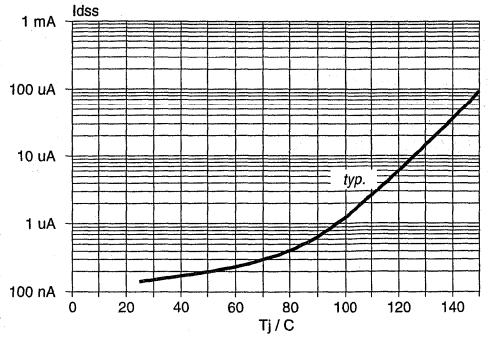


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

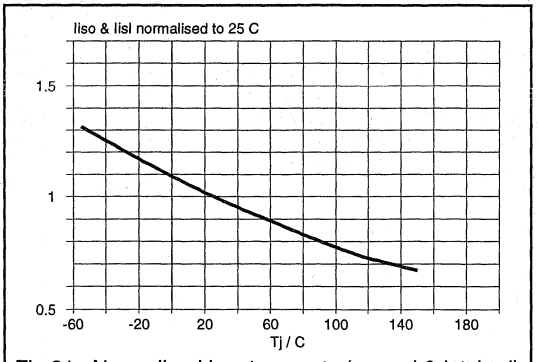


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25°C$ & $I_{ISL}/I_{ISL}25°C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK108-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	13.5	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	125	mΩ

FUNCTIONAL BLOCK DIAGRAM

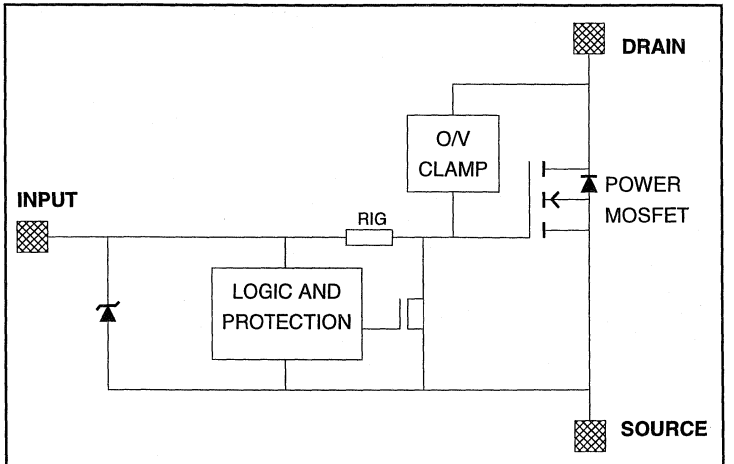
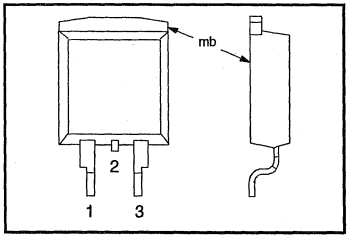


Fig.1. Elements of the TOPFET.

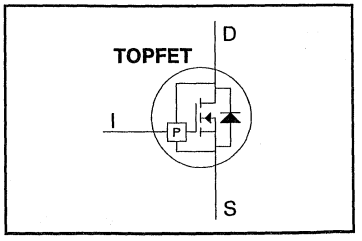
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	13.5	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	54	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 32)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 7.5 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.2	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 0.5$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq$ 300 µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	25	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	6	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	4.5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	13.5	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

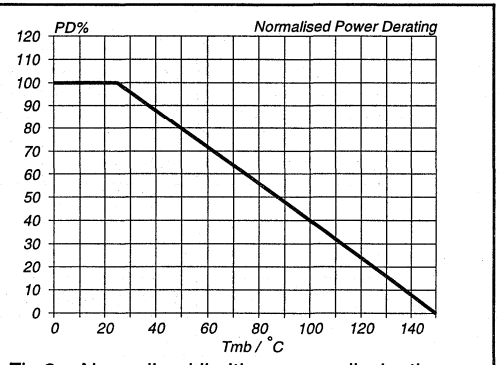


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

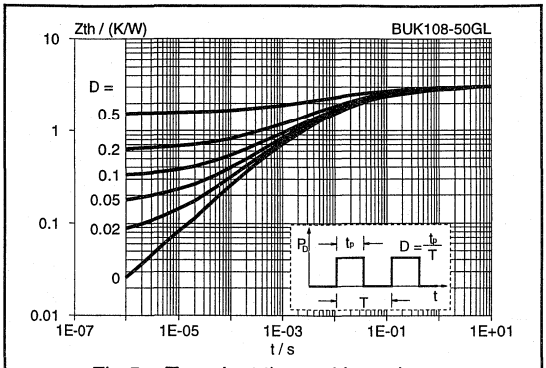


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

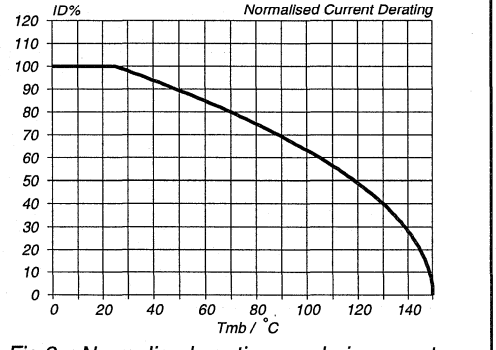


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

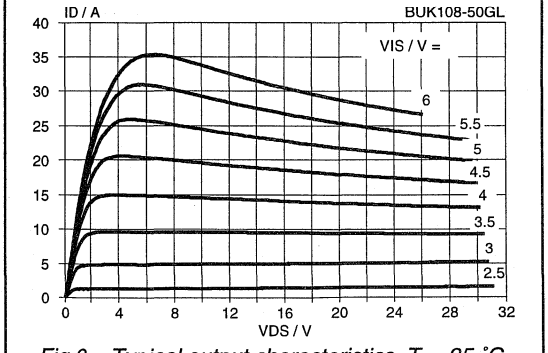


Fig.6. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

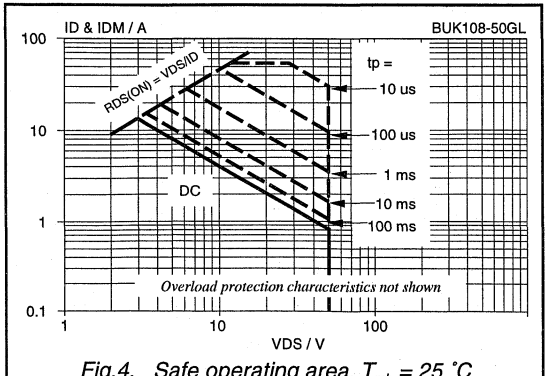


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

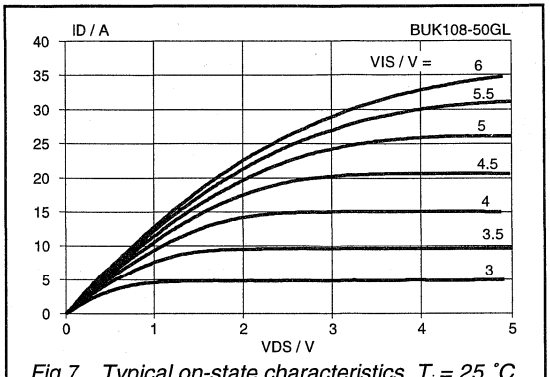


Fig.7. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

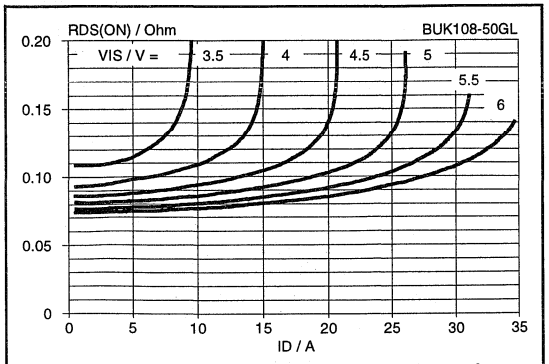


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

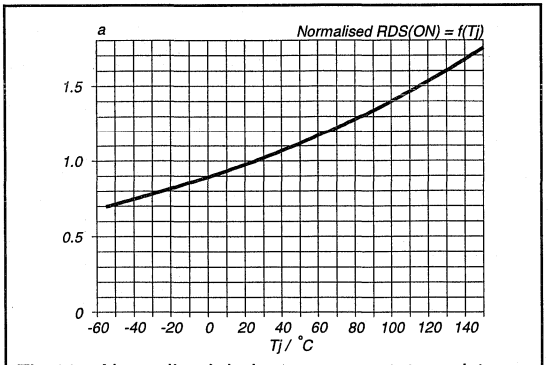


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C = $f(T_j)$; I_D = 7.5 A; V_{IS} = 5 V

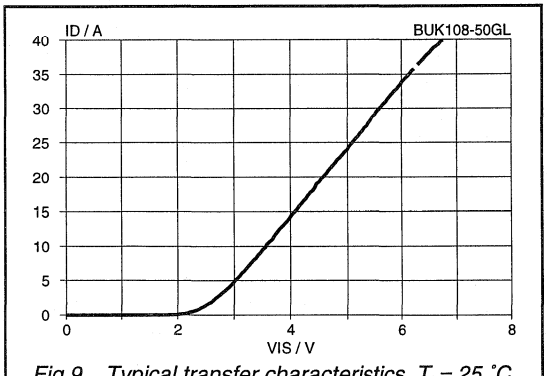


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

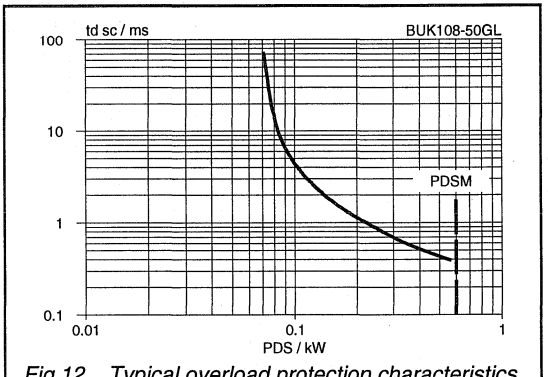


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

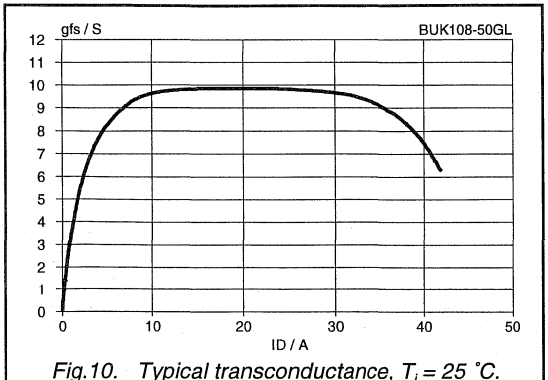


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

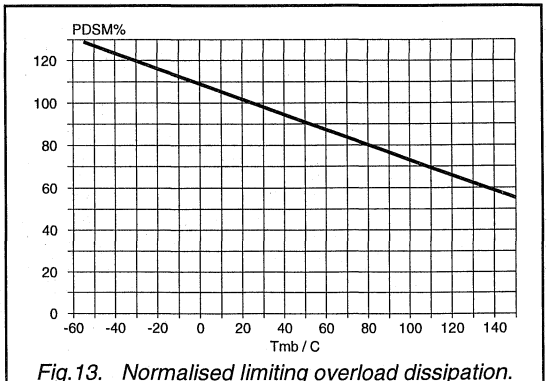


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ˚C) = f(T_{mb})$

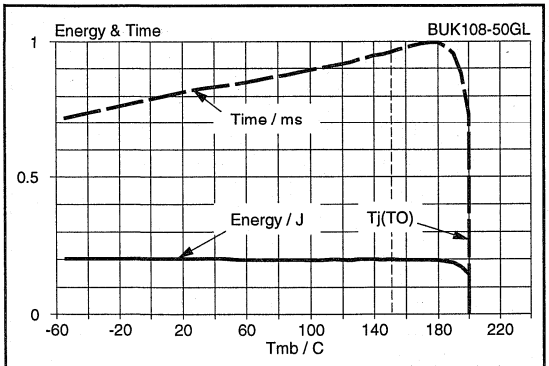


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

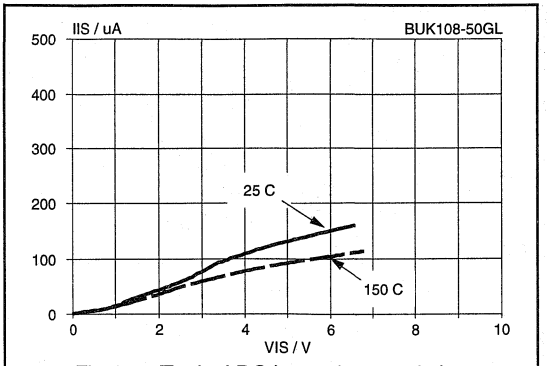


Fig.17. Typical DC input characteristics. $I_{IS} = f(V_{IS})$; normal operation, parameter: T_j

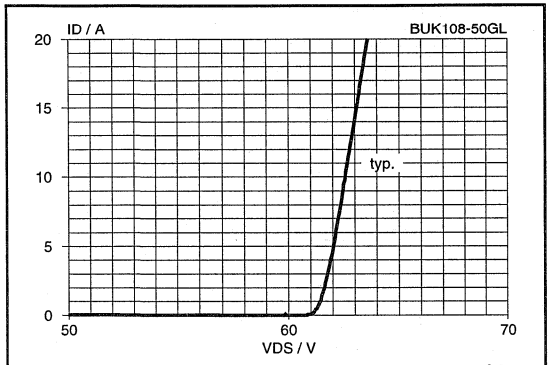


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

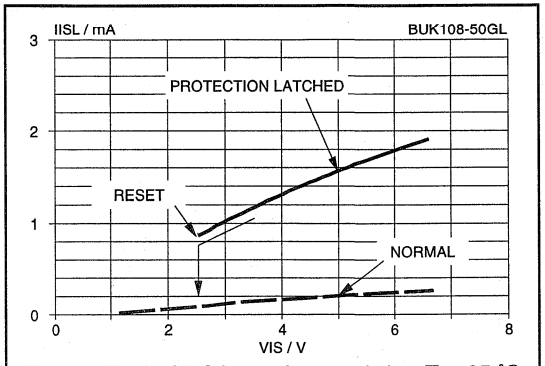


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

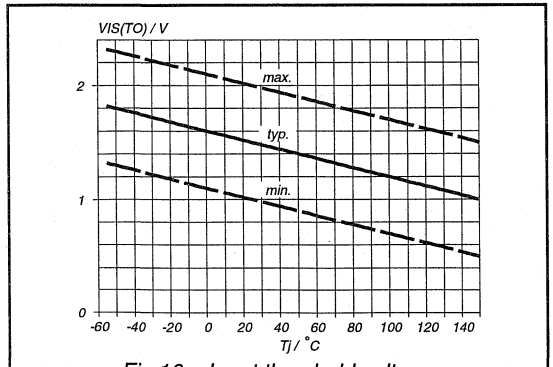


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

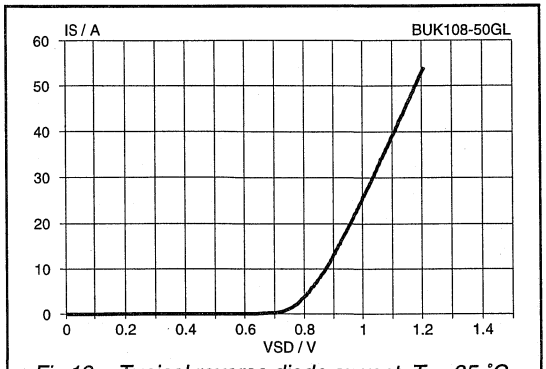


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

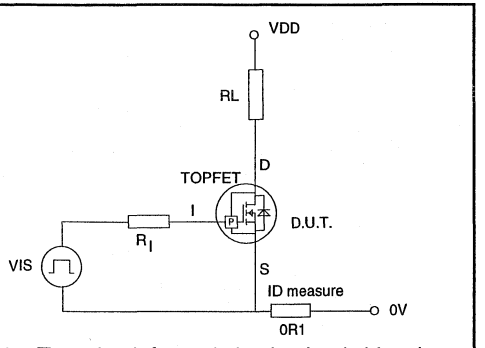


Fig.20. Test circuit for resistive load switching times.

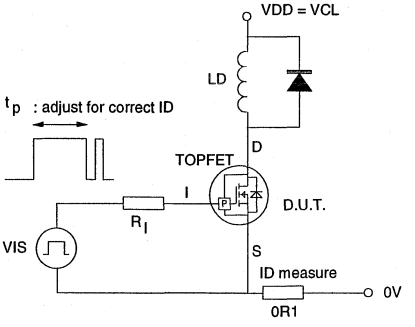


Fig.23. Test circuit for inductive load switching times.

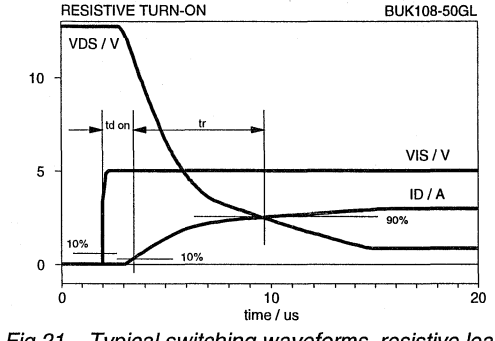


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

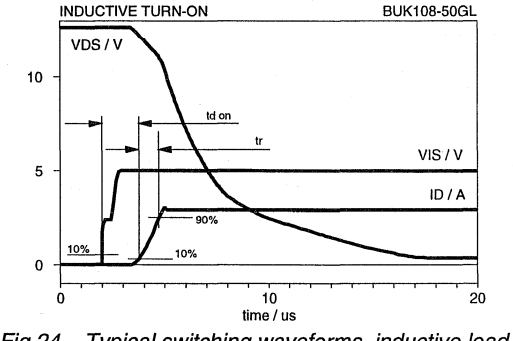


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

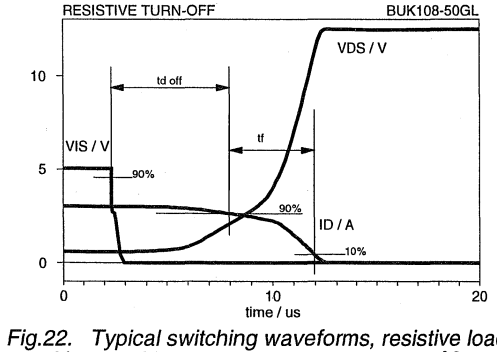


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 °C.

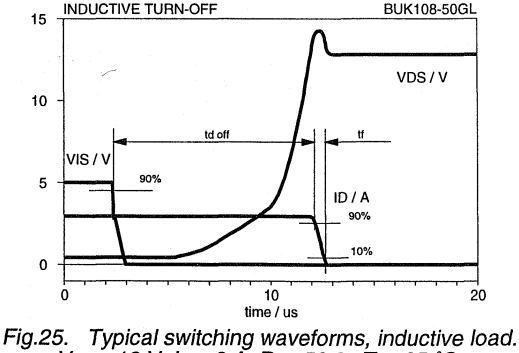


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

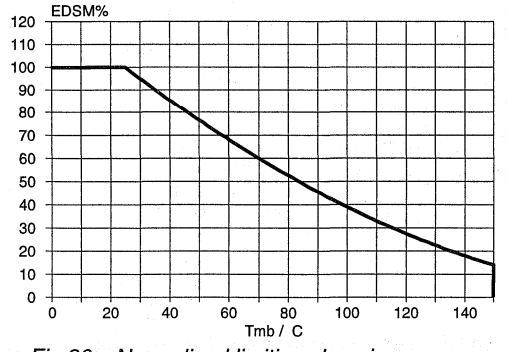


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A; V_{IS} = 5 V

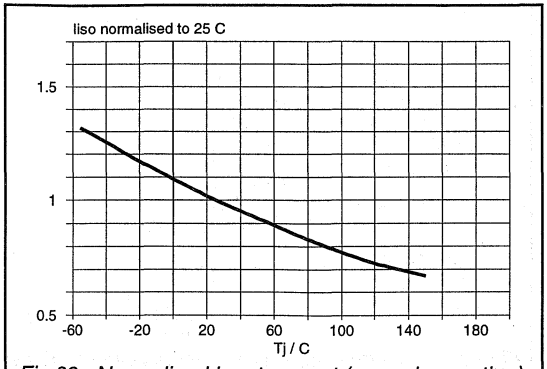


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

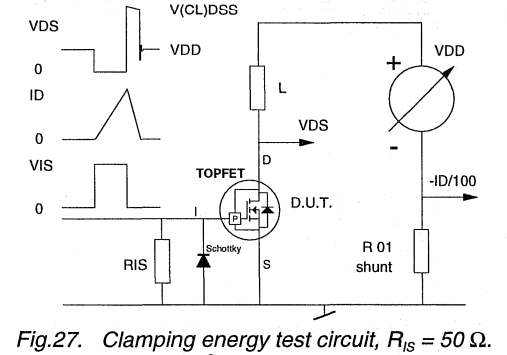


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

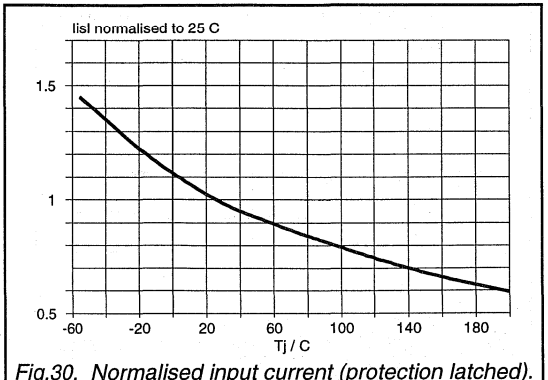


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

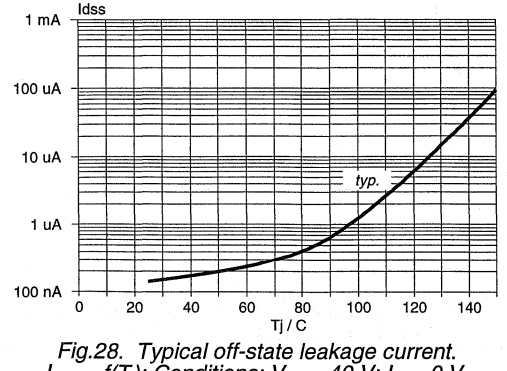


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK108-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_D	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	100	mΩ

FUNCTIONAL BLOCK DIAGRAM

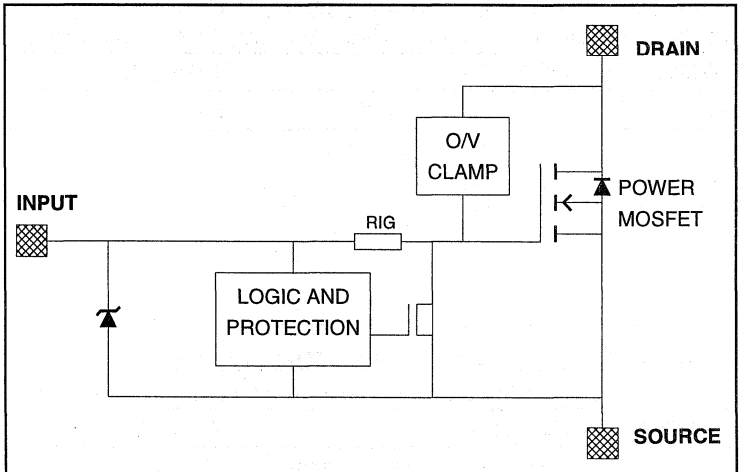
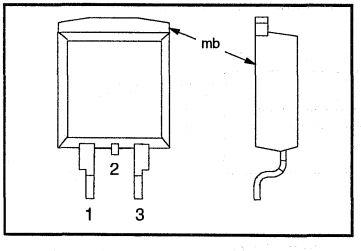


Fig.1. Elements of the TOPFET.

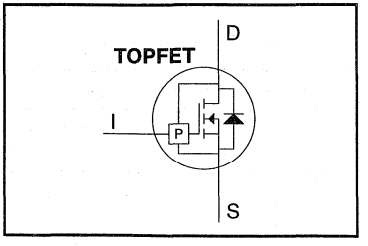
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	15	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	9.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	60	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	20	V
		V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	0.6	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	15	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 15 A; $V_{DD} \leq 20$ V; inductive load	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 33)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 1 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 7.5 A; $t_p \leq 300\ \mu s$; $\delta \leq 0.01$	V_{IS} = 10 V	-	65	100	mΩ
			V_{IS} = 5 V	-	85	125	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	0.2	-	J
$t_{d\,sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \geq 0.5$ A[2]	150	-	-	°C

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[1]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	1.0	2.5	5.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
$I_{D(SC)}$	Drain current[2]	V_{DS} = 13 V; V_{IS} = 10 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	resistive load R_L = 4 Ω	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 4 Ω	-	5	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1	-	µs
t_r	Rise time	inductive load I_{DM} = 3 A	-	0.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 3 A	-	0.5	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	15	A

1 The input voltage below which the overload protection circuits will be reset.

2 During overload before short circuit load protection operates.

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[1]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead solering point to source bond pad	-	7.5	-	nH

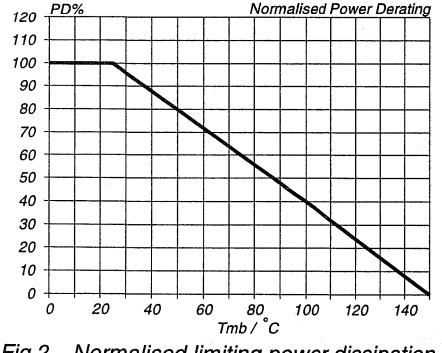


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

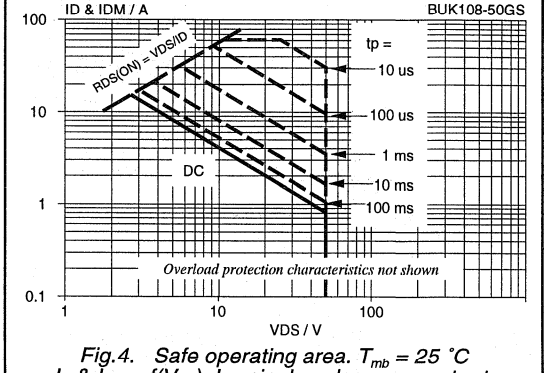


Fig.4. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

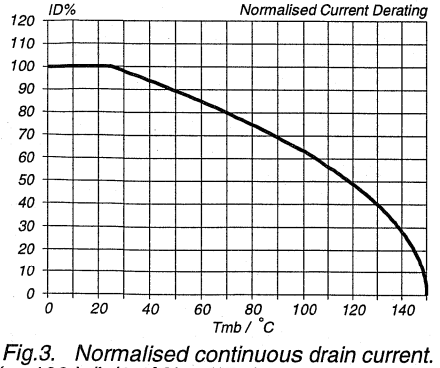


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ °C) = f(T_{mb})$; *conditions:* V_{IS} = 5 V

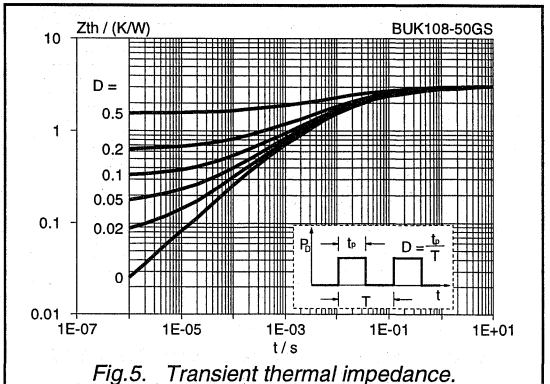


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

1 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

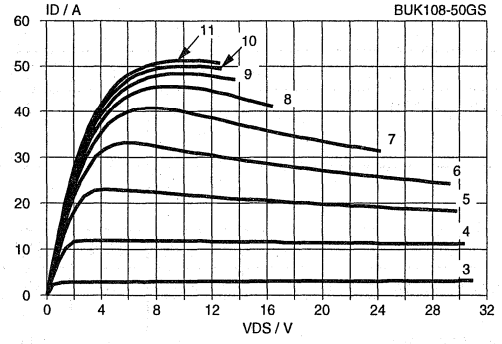


Fig.6. Typical output characteristics, T_j = 25 ˚C. ID = f(V_{DS}); parameter V_{IS}; t_p = 250 µs & $t_p < t_{d\,sc}$

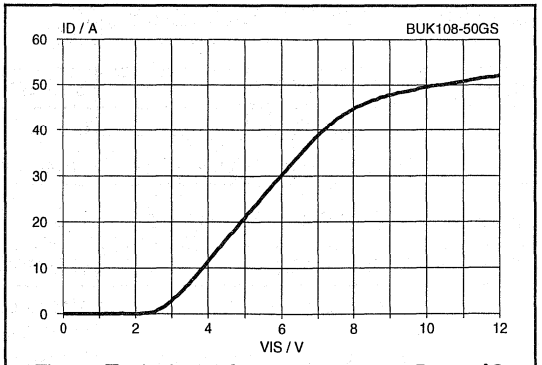


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. I_D = f(V_{IS}) ; conditions: V_{DS} = 10 V; t_p = 250 µs

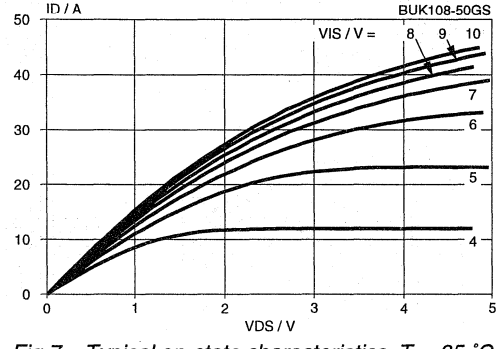


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. ID = f(V_{DS}); parameter V_{IS}; t_p = 250 µs

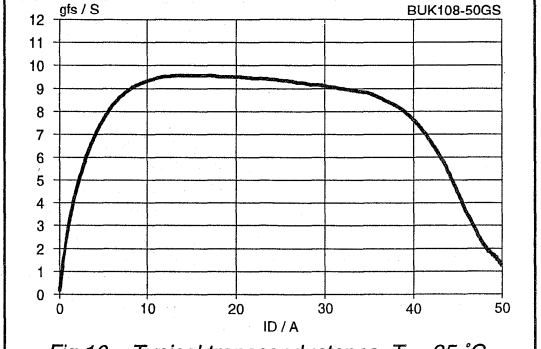


Fig.10. Typical transconductance, T_j = 25 ˚C. g_{fs} = f(I_D); conditions: V_{DS} = 10 V; t_p = 250 µs

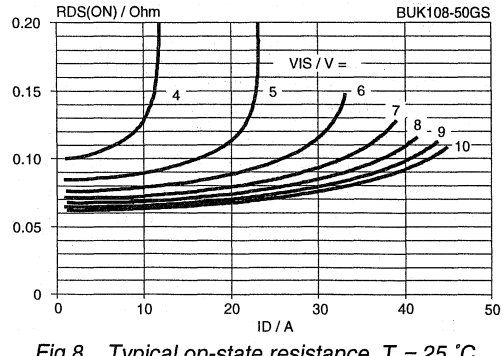


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 250 µs

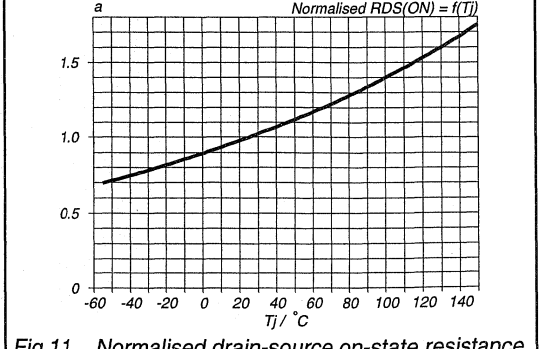


Fig.11. Normalised drain-source on-state resistance. a = $R_{DS(ON)}/R_{DS(ON)}$25 ˚C = f(T_j); I_D = 7.5 A; V_{IS} = 5 V

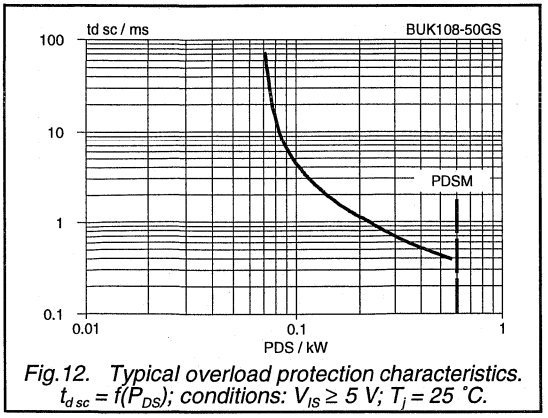


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 5$ V; $T_j = 25$ °C.

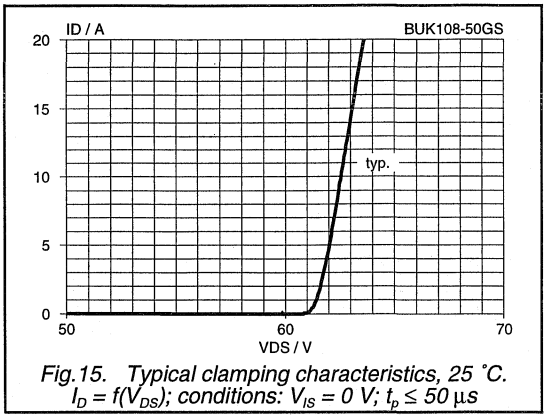


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

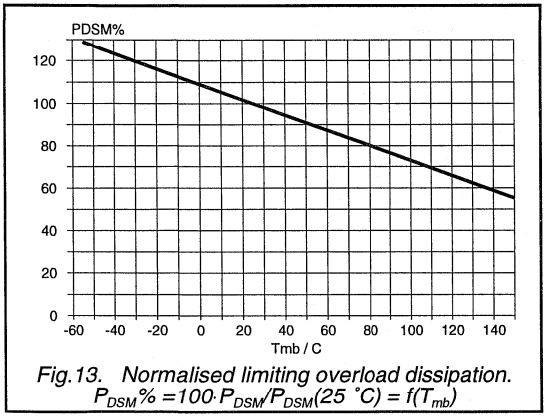


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

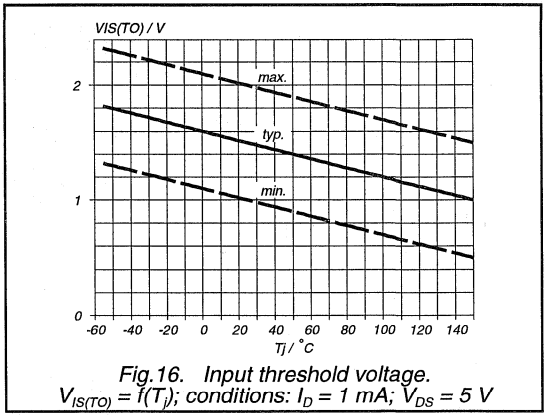


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

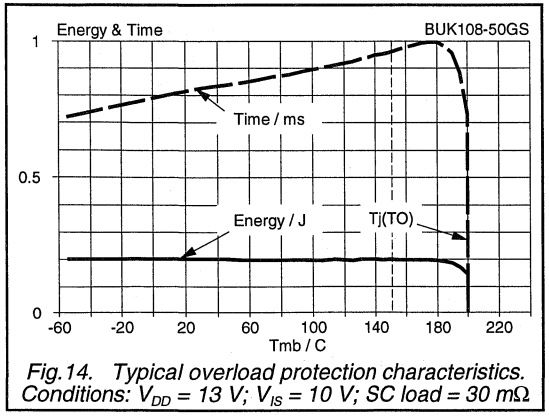


Fig.14. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{IS} = 10$ V; SC load = 30 mΩ

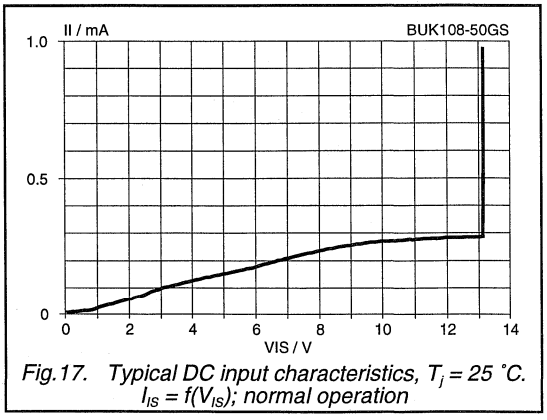


Fig.17. Typical DC input characteristics, $T_j = 25$ °C. $I_{IS} = f(V_{IS})$; normal operation

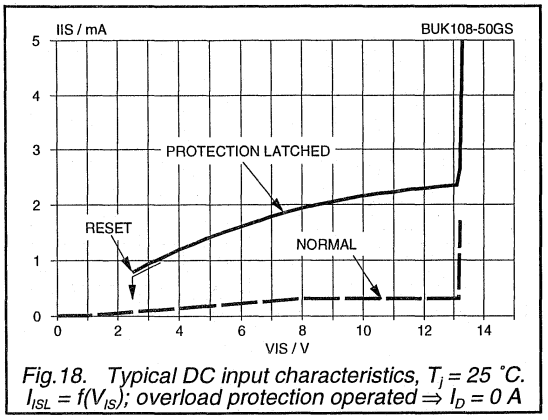


Fig.18. Typical DC input characteristics, T_j = 25 ˚C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

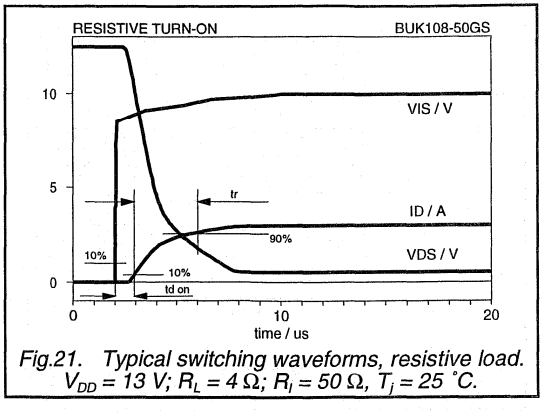


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 ˚C.

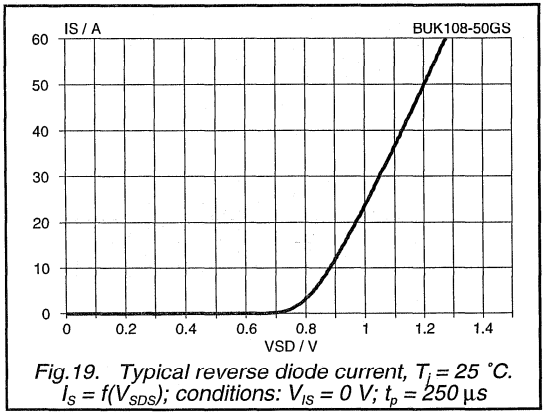


Fig.19. Typical reverse diode current, T_j = 25 ˚C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

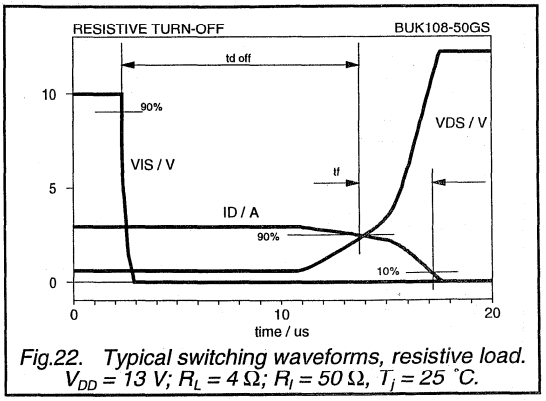


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 4 Ω; R_I = 50 Ω, T_j = 25 ˚C.

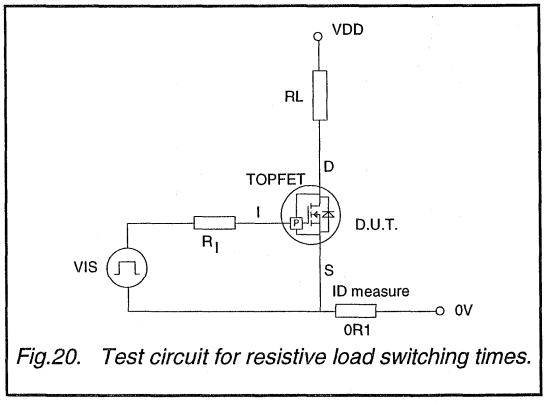


Fig.20. Test circuit for resistive load switching times.

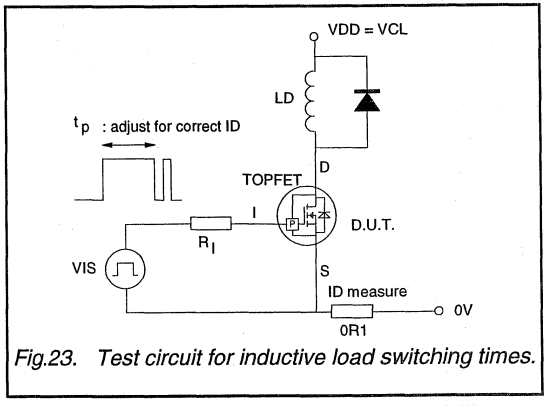


Fig.23. Test circuit for inductive load switching times.

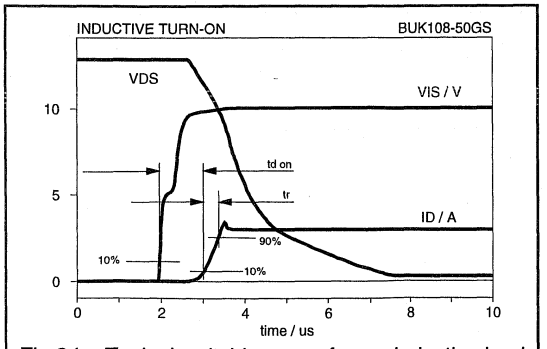


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

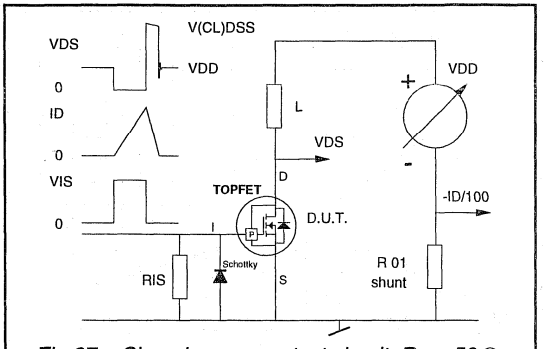


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

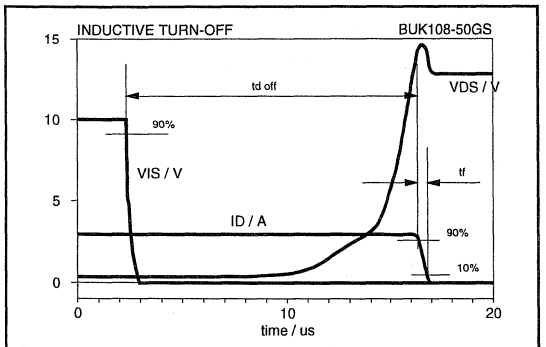


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 3 A; R_I = 50 Ω, T_j = 25 °C.

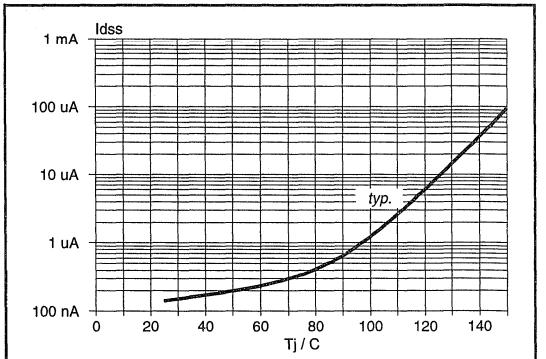


Fig.28. Typical off-state leakage current. I_{DSS} = f(T_j); Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

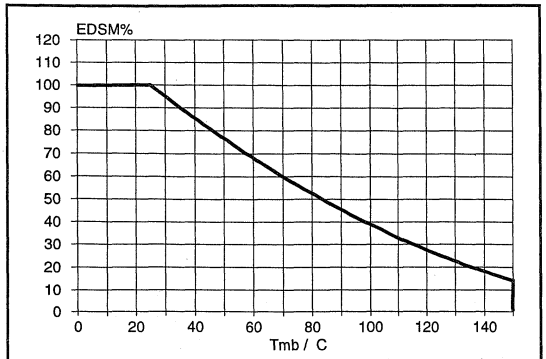


Fig.26. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 15 A; V_{IS} = 10 V

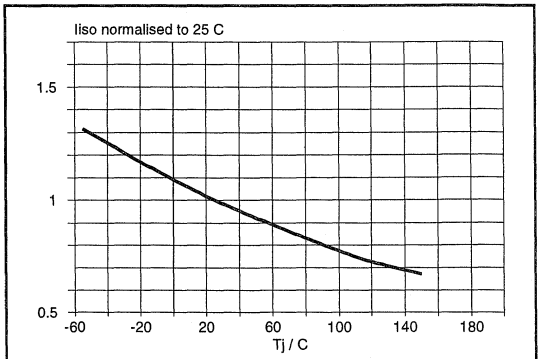


Fig.29. Normalised input current (normal operation). I_{IS}/I_{IS}25 °C = f(T_j); V_{IS} = 10 V

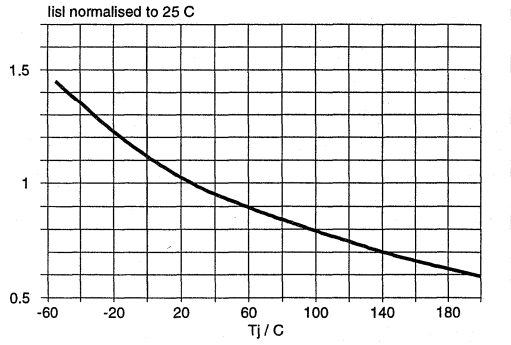


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

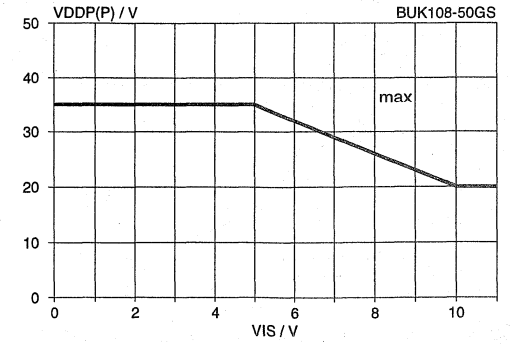


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^{\circ}C$

PowerMOS transistor
Logic level TOPFET

BUK109-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		26	A
P_D	Total power dissipation		75	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		60	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	μA

FUNCTIONAL BLOCK DIAGRAM

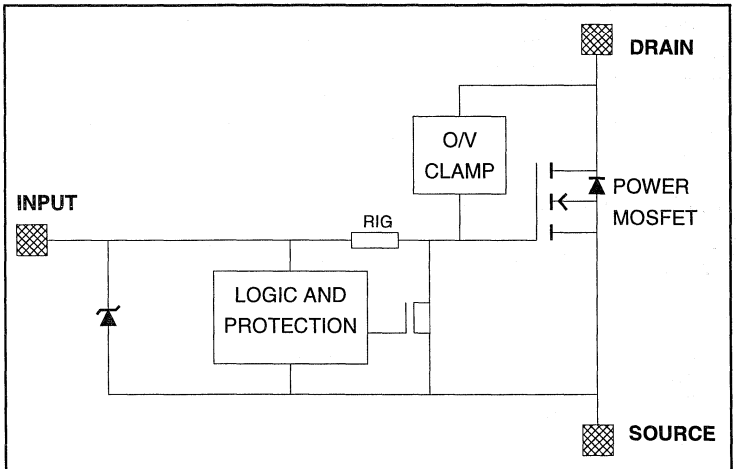
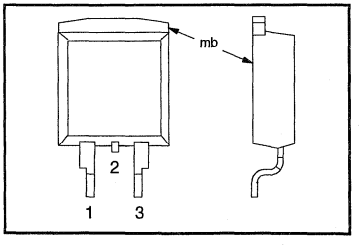


Fig.1. Elements of the TOPFET.

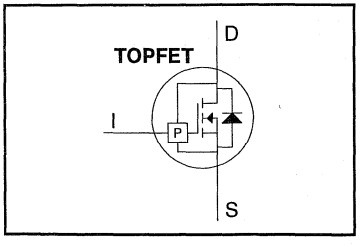
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	20	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 26$ A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; $I_{DM} = 8$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 23)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	45	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	105	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq 300$ µs; $\delta \leq 0.01$	10	16	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	17	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	75	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	60	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	70	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

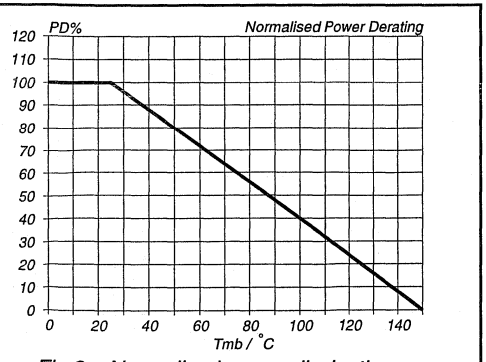


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

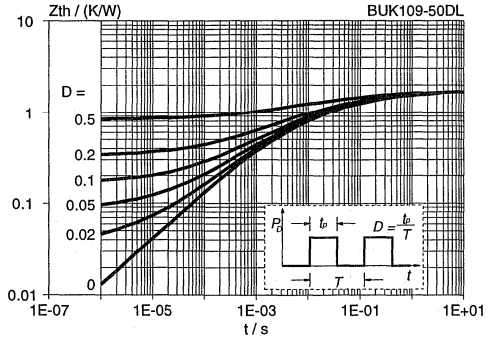


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

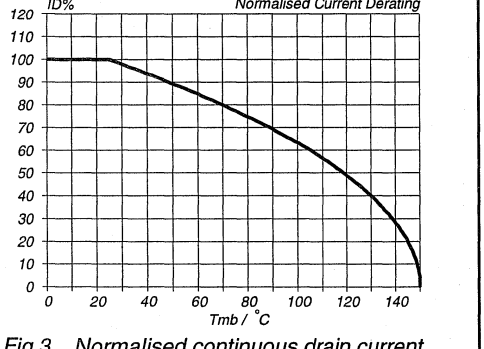


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; *conditions:* $V_{IS} = 5$ V

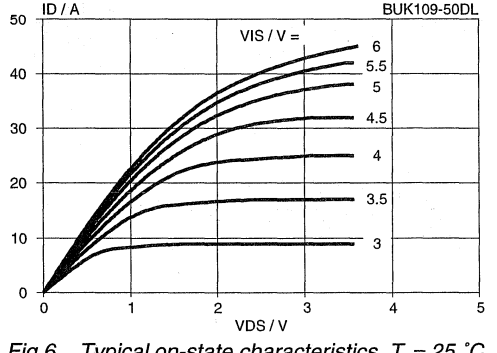


Fig.6. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 2$ *ms*

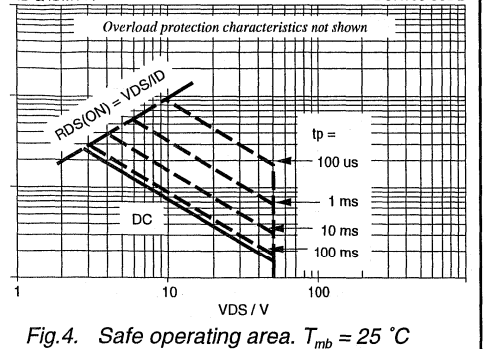


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

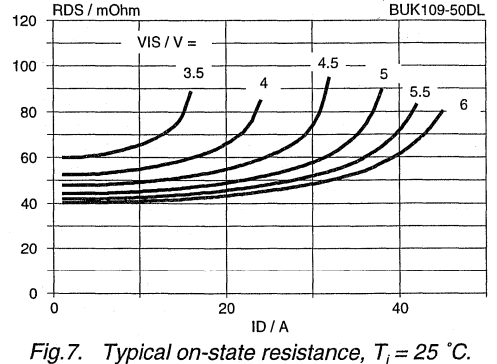


Fig.7. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; *parameter* V_{IS}; $t_p = 2$ *ms*

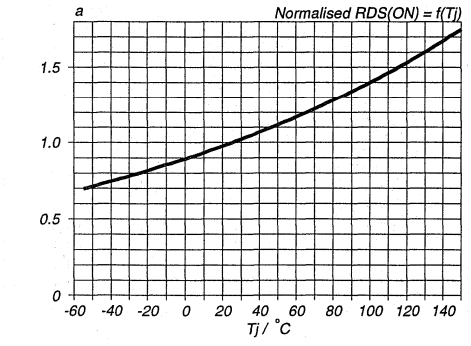


Fig.8. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; $I_D = 13$ A; $V_{IS} = 5$ V

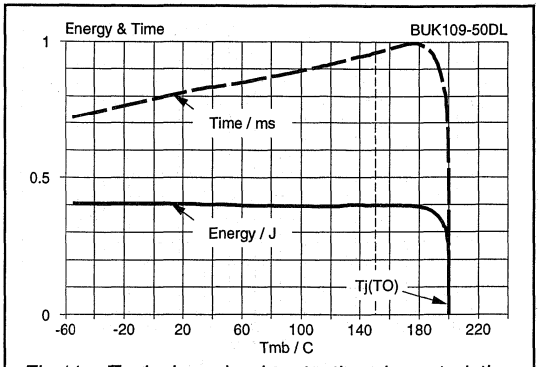


Fig.11. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{IS} = 5$ V; SC load = 30 mΩ

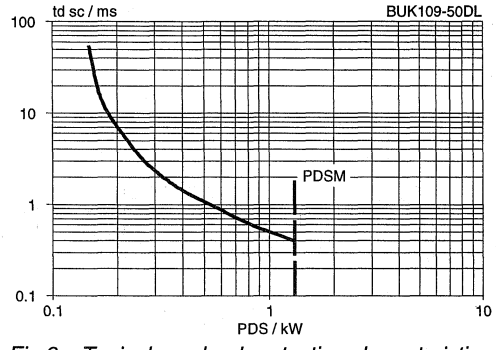


Fig.9. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; $T_j = 25\ ^\circ C$.

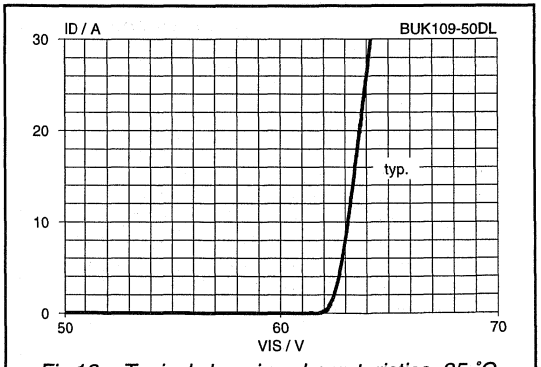


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

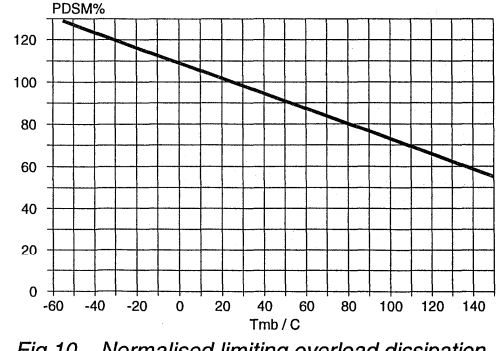


Fig.10. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

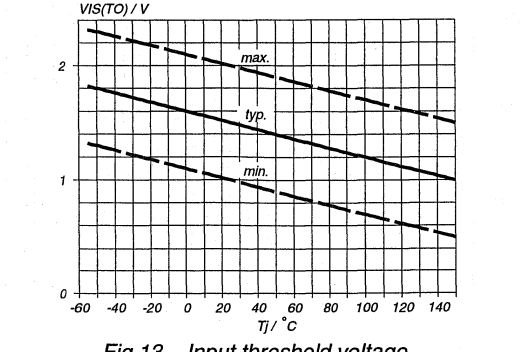


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

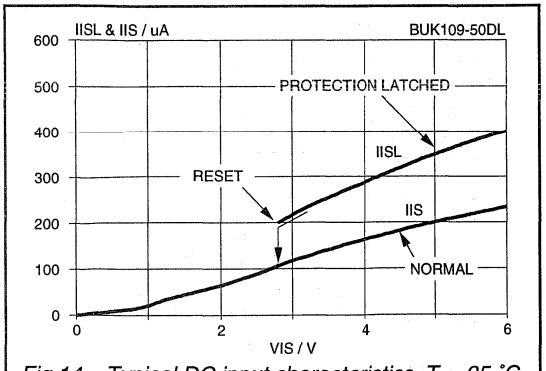


Fig.14. Typical DC input characteristics, T_j = 25 °C. I_{ISL} & I_{IS} = f(V_{IS}); protection latched & normal operation

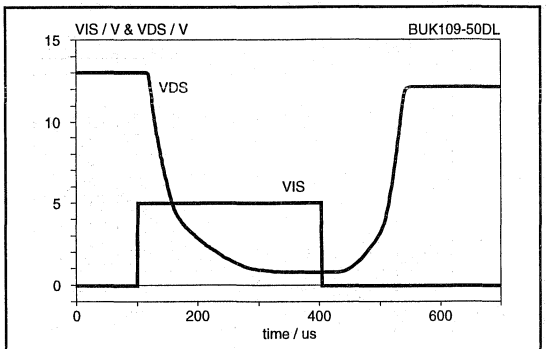


Fig.17. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

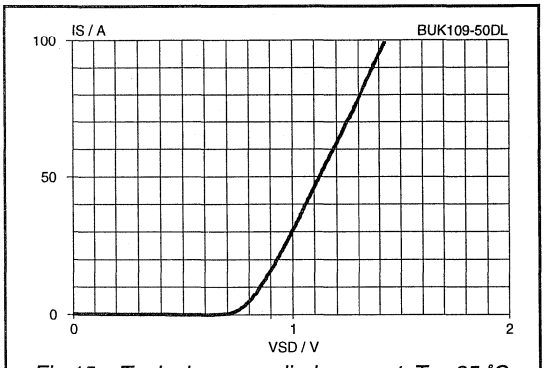


Fig.15. Typical reverse diode current, T_j = 25 °C. I_S = f(V_{SDS}); conditions: V_{IS} = 0 V

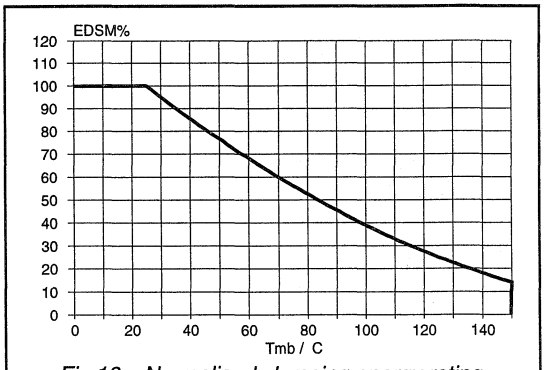


Fig.18. Normalised clamping energy rating. E_{DSM}% = f(T_{mb}); conditions: I_D = 26 A; V_{IS} = 5 V

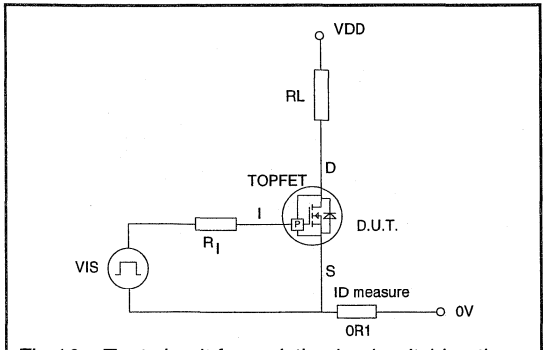


Fig.16. Test circuit for resistive load switching times.

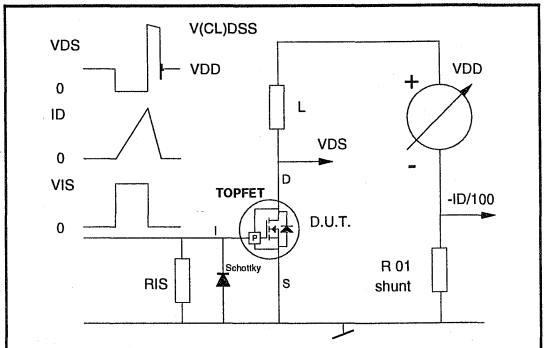


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

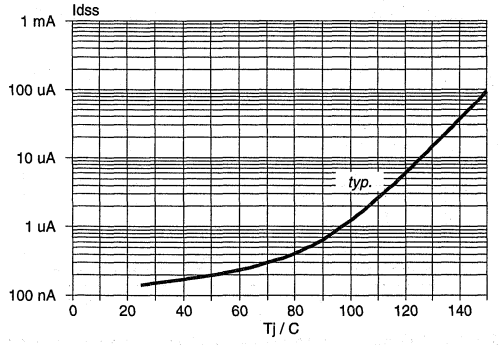


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

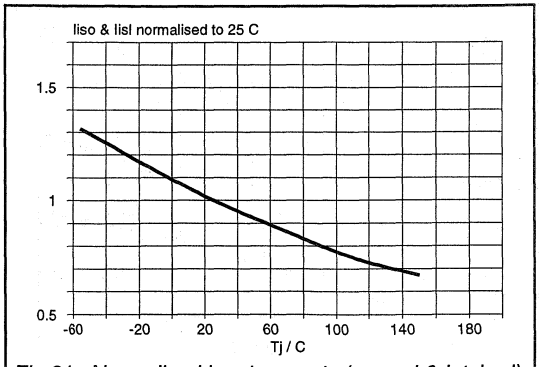


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor
Logic level TOPFET

BUK109-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	26	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	60	mΩ

FUNCTIONAL BLOCK DIAGRAM

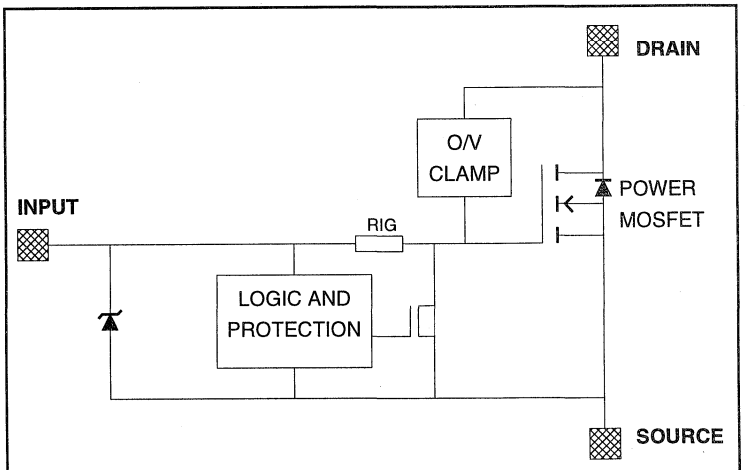
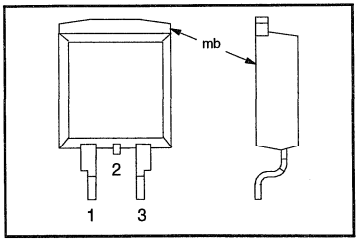


Fig.1. Elements of the TOPFET.

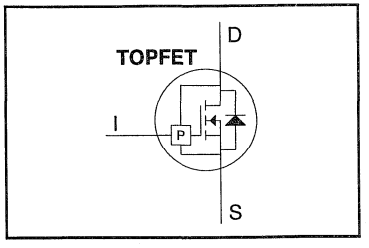
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[1]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[2]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[3]	V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 26 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

2 The input voltage for which the overload protection circuits are functional.

3 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 32)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{IS} = 5 V; I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	0.4	-	J
$t_{d\,sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 1$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	0.5	1.2	2.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	7	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq$ 300 µs; $\delta \leq$ 0.01	10	16	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	40	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	15	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	10	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	7	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	4	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	15	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C	-	26	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 26 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

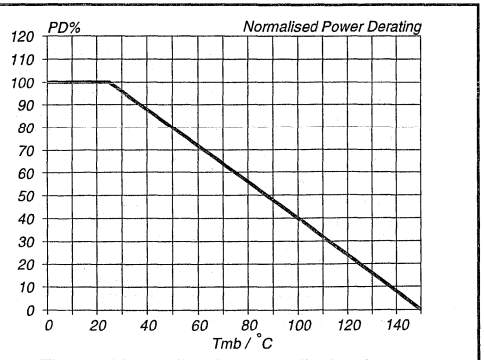


Fig.2. Normalised power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

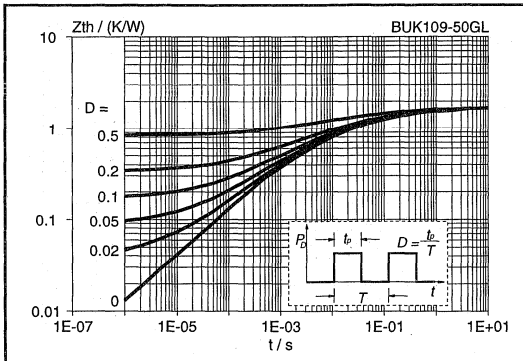


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

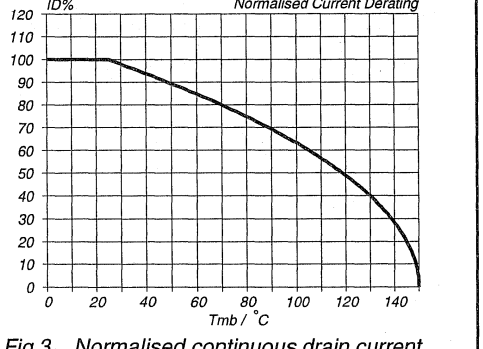


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

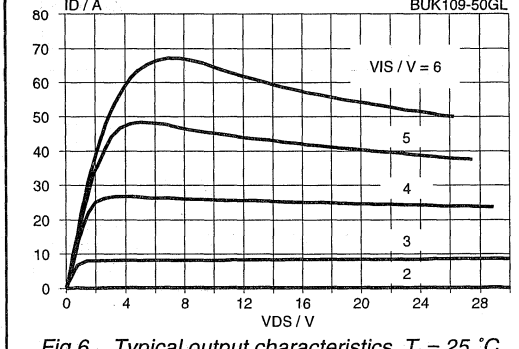


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

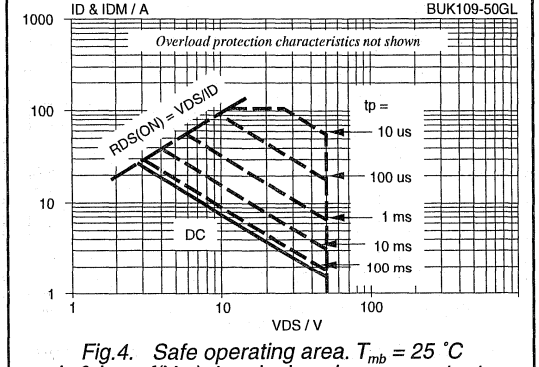


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

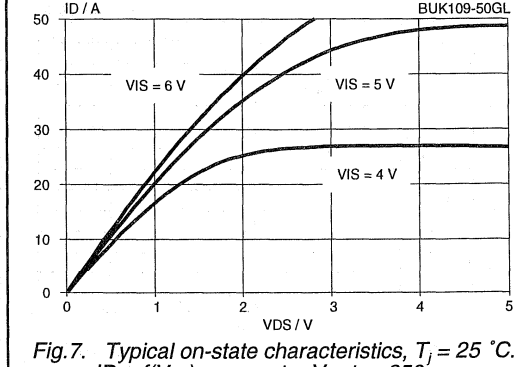


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

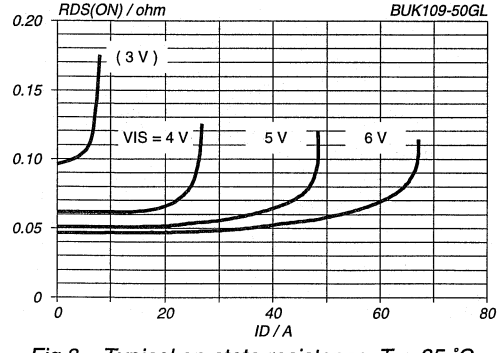


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

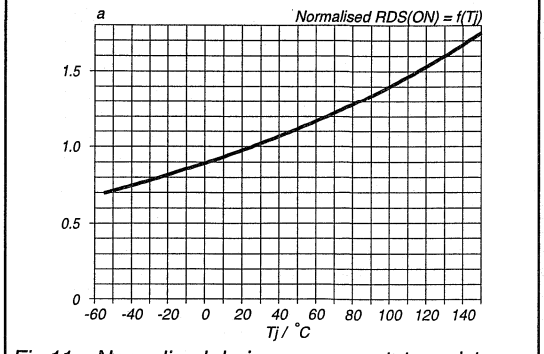


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C $= f(T_j)$; I_D = 13 A; V_{IS} = 5 V

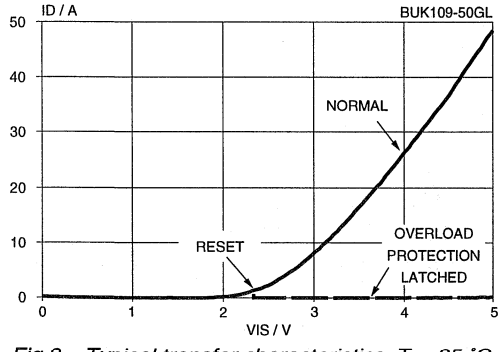


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

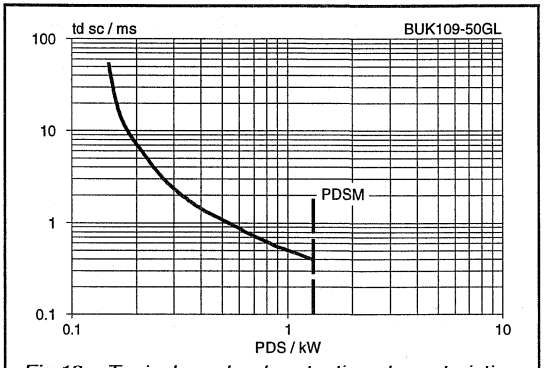


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

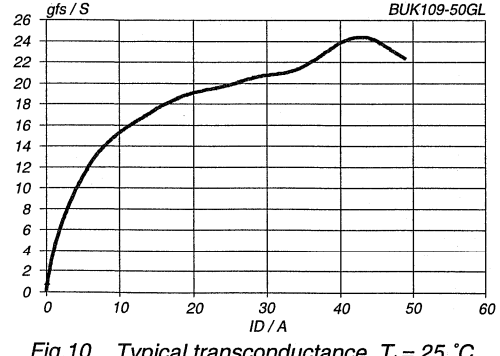


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

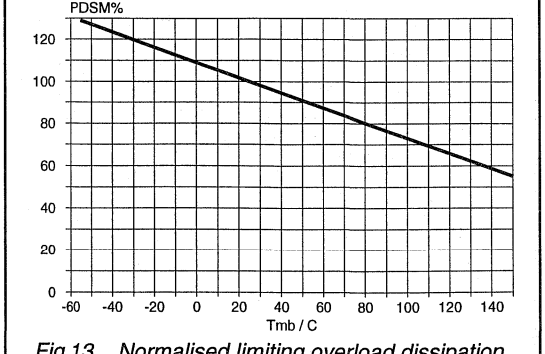


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

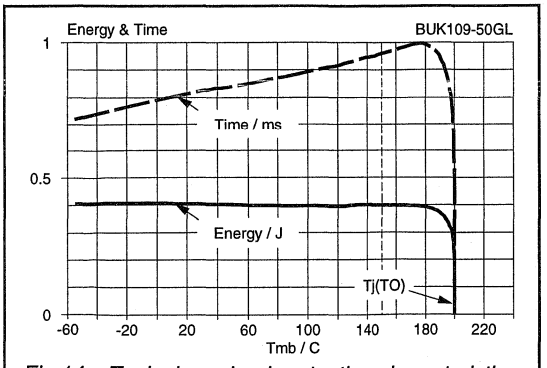


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

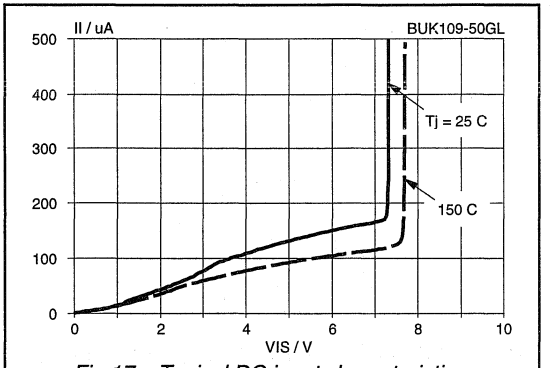


Fig.17. Typical DC input characteristics. $I_I = f(V_{IS})$; normal operation; parameter: T_j

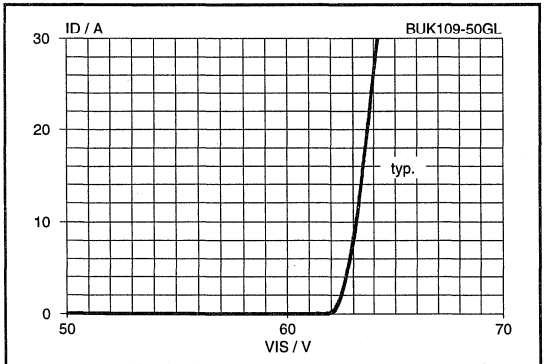


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

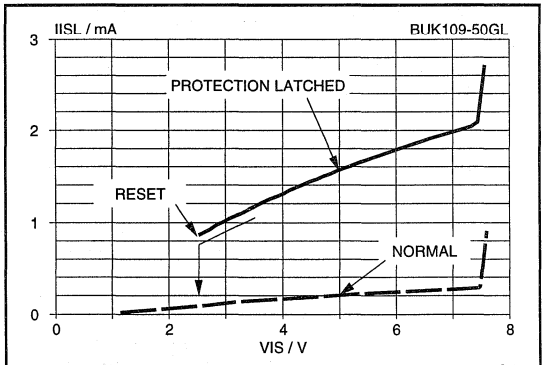


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

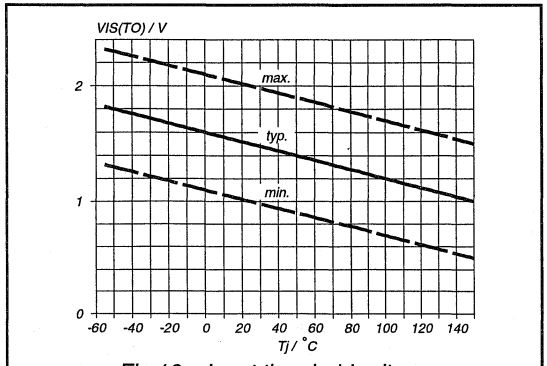


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

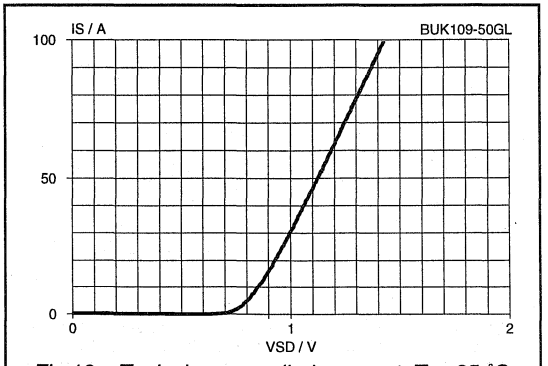


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V

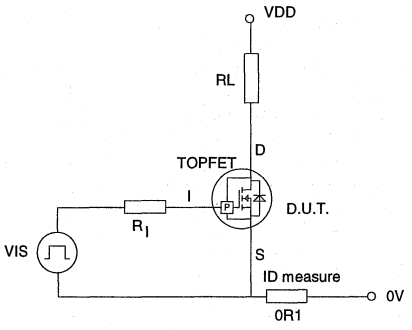


Fig.20. Test circuit for resistive load switching times.

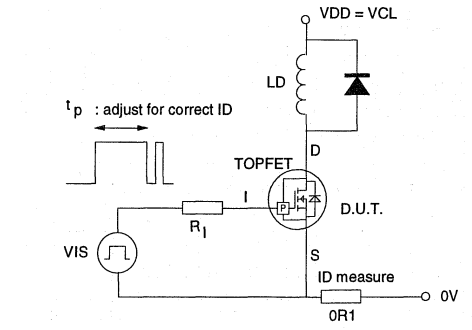


Fig.23. Test circuit for inductive load switching times.

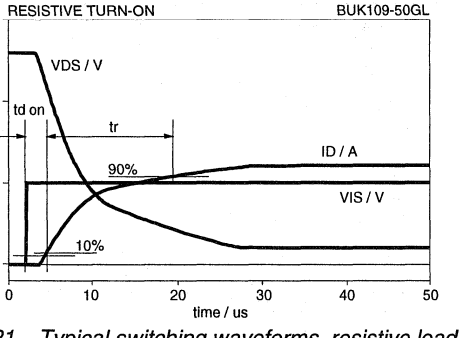


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

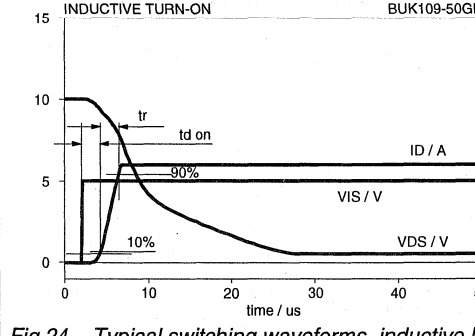


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 ˚C.

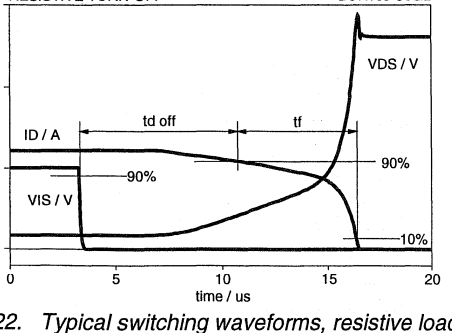


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

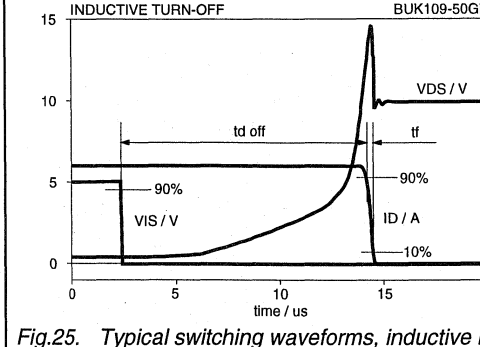


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_I = 50 Ω, T_j = 25 ˚C.

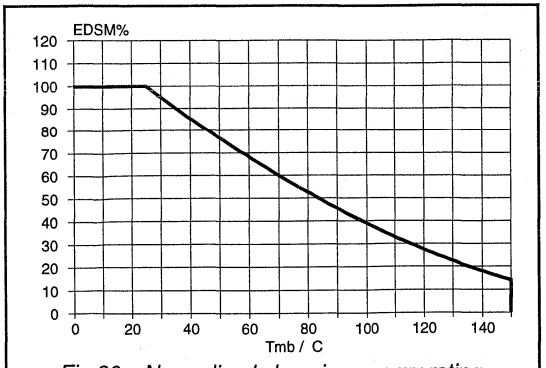


Fig.26. Normalised clamping energy rating. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 26 A; V_{IS} = 5 V

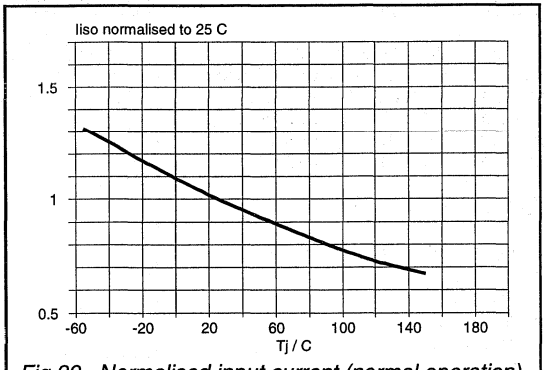


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

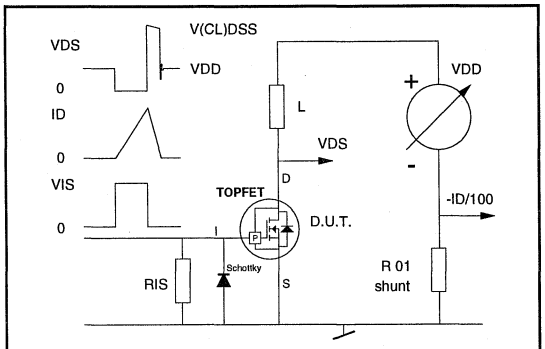


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

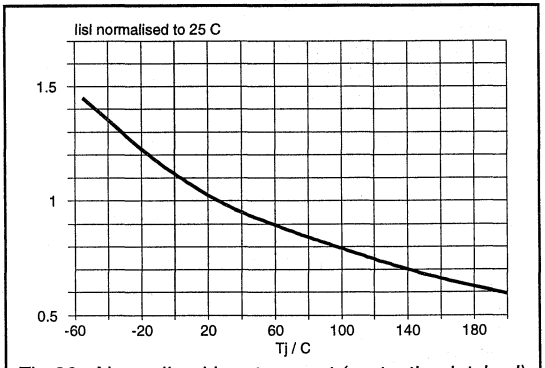


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 5 V

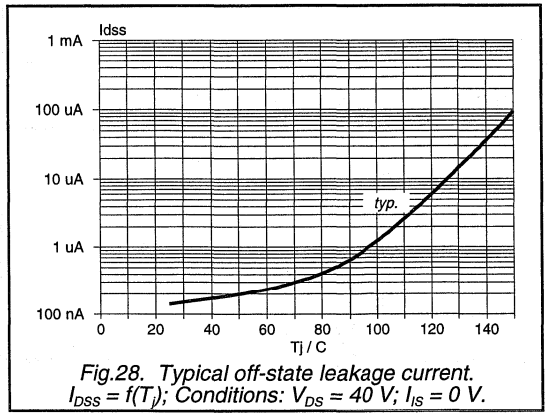


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK109-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	29	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	50	mΩ

FUNCTIONAL BLOCK DIAGRAM

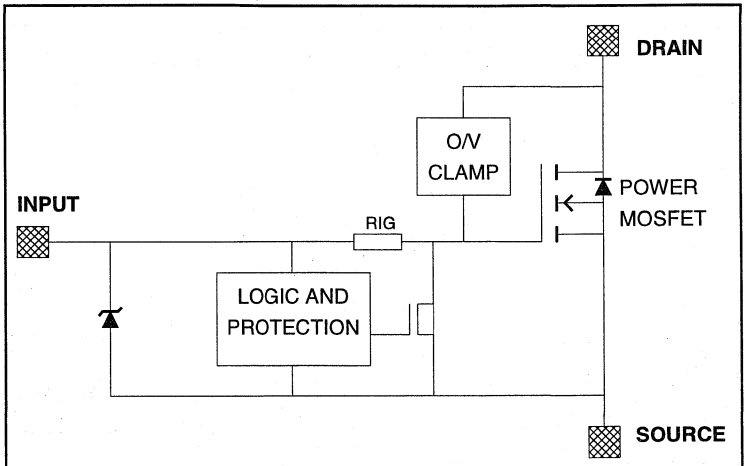
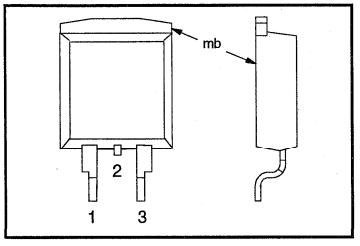


Fig.1. Elements of the TOPFET.

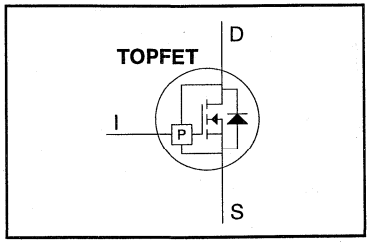
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	29	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	18	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	120	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	75	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	20	V
		V_{IS} = 5 V	-	35	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	29	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 27 A; $V_{DD} \leq 20$ V; inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95$ °C; I_{DM} = 8 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB (see fig. 33)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 2 A; $t_p \leq 300$ µs; $\delta \leq 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 13 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	V_{IS} = 10 V	-	35	50	mΩ
			V_{IS} = 5 V	-	45	60	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	0.4	-	J
$t_{d\,sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \geq 1$ A[2]	150	-	-	°C

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[1]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	1.0	2.5	4.0	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	4	-	kΩ

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 13 A $t_p \leq$ 300 µs; $\delta \leq$ 0.01	10	16	-	S
$I_{D(SC)}$	Drain current[2]	V_{DS} = 13 V; V_{IS} = 10 V	-	80	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	6	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	18	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	9	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 10 V; V_{IS} = 10 V	-	2	-	µs
t_r	Rise time	inductive load I_{DM} = 6 A	-	1	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 10 V; V_{IS} = 0 V	-	22	-	µs
t_f	Fall time	inductive load I_{DM} = 6 A	-	1	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	29	A

1 The input voltage below which the overload protection circuits will be reset.

2 During overload before short circuit load protection operates.

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 29 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[1]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

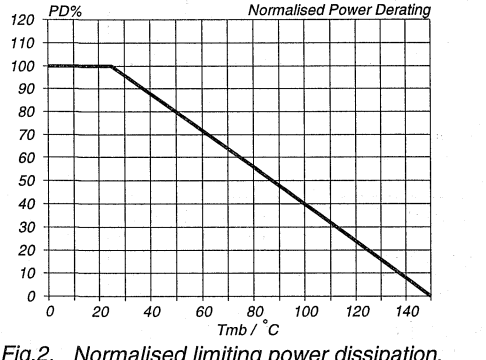


Fig.2. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

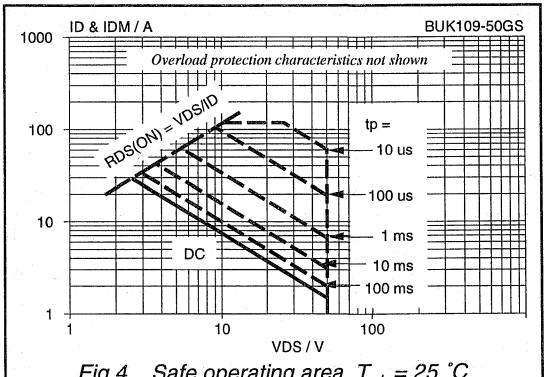


Fig.4. Safe operating area. T_{mb} = 25 °C I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

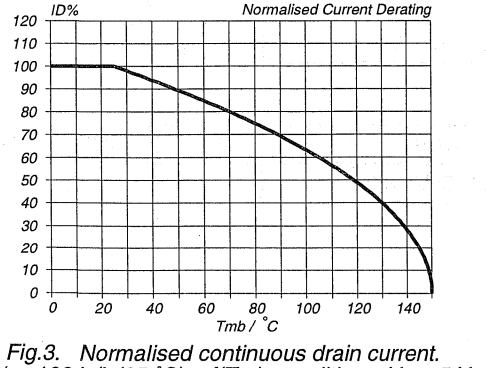


Fig.3. Normalised continuous drain current. $I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: V_{IS} = 5 V

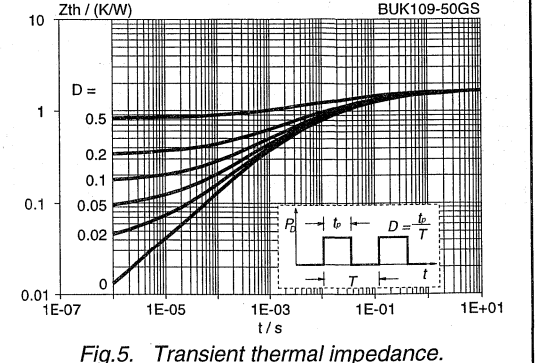


Fig.5. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

1 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

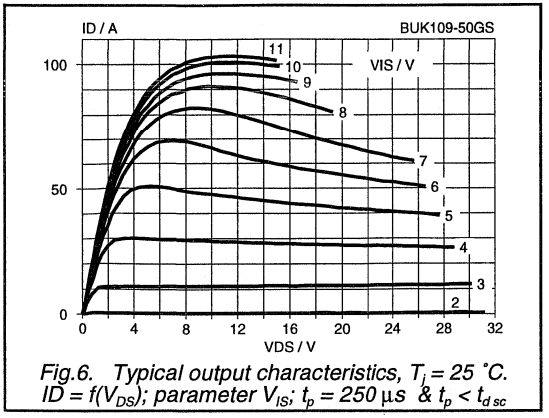


Fig.6. Typical output characteristics, T_j = 25 °C. ID = f(V_{DS}); parameter V_{IS}; t_p = 250 µs & $t_p < t_{d\,sc}$

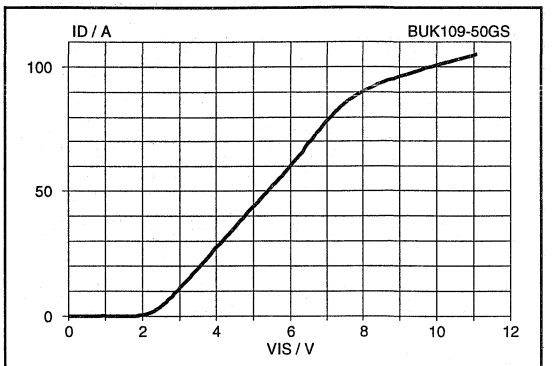


Fig.9. Typical transfer characteristics, T_j = 25 °C. I_D = f(V_{IS}) ; conditions: V_{DS} = 10 V; t_p = 250 µs

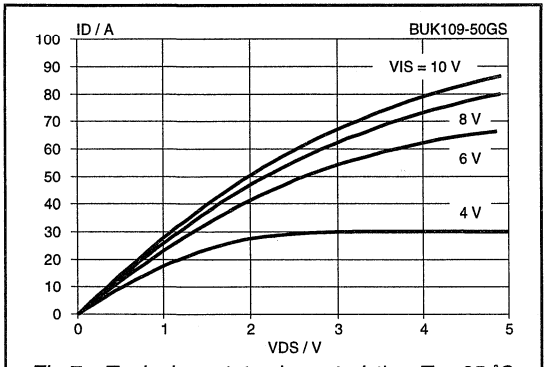


Fig.7. Typical on-state characteristics, T_j = 25 °C. ID = f(V_{DS}); parameter V_{IS}; t_p = 250 µs

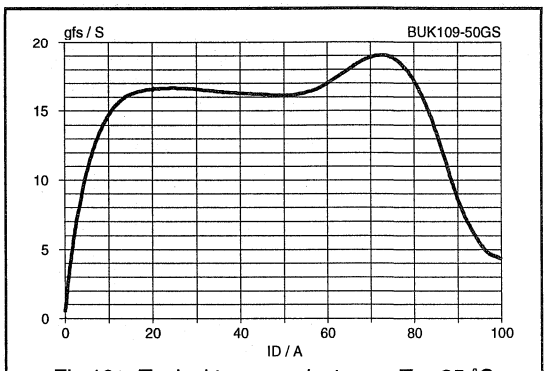


Fig.10. Typical transconductance, T_j = 25 °C. g_{fs} = f(I_D); conditions: V_{DS} = 10 V; t_p = 250 µs

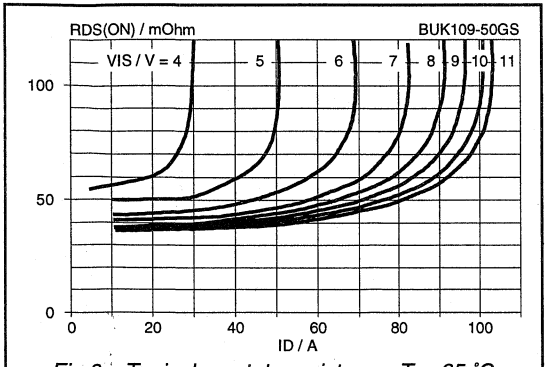


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)}$ = f(I_D); parameter V_{IS}; t_p = 250 µs

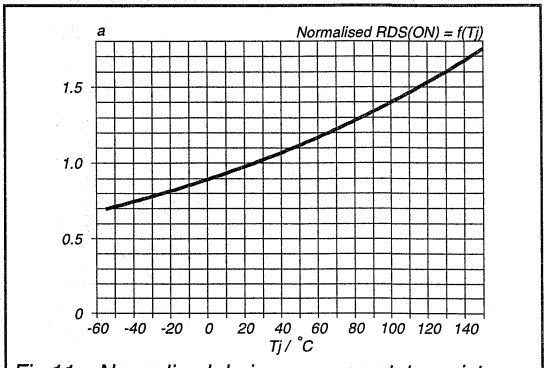


Fig.11. Normalised drain-source on-state resistance. a = $R_{DS(ON)}$/$R_{DS(ON)}$25 °C = f(T_j); I_D = 13 A; V_{IS} = 10 V

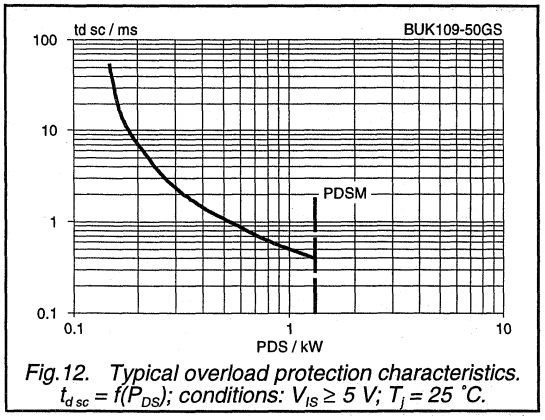


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 5$ V; $T_j = 25$ ˚C.

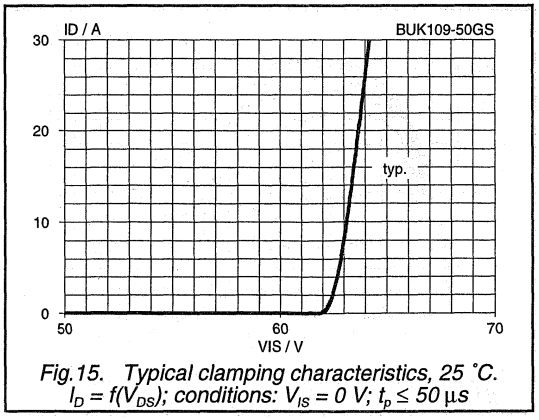


Fig.15. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

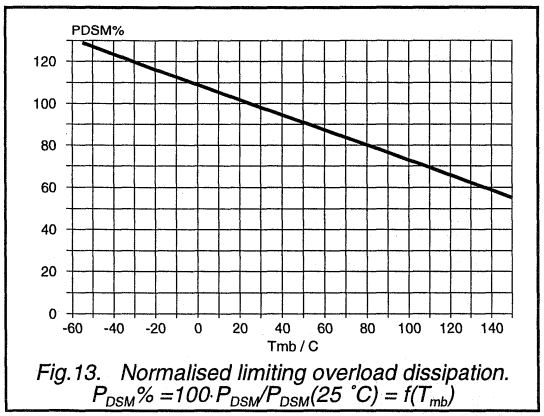


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

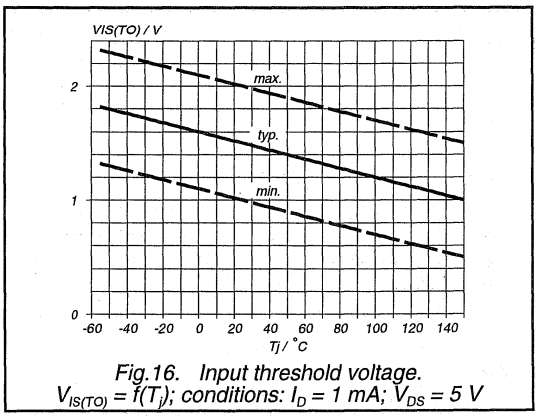


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

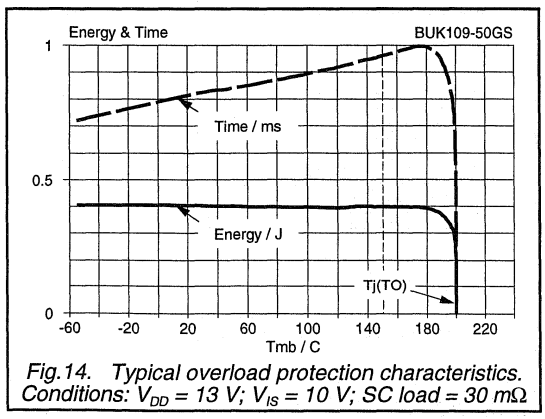


Fig.14. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{IS} = 10$ V; SC load = 30 mΩ

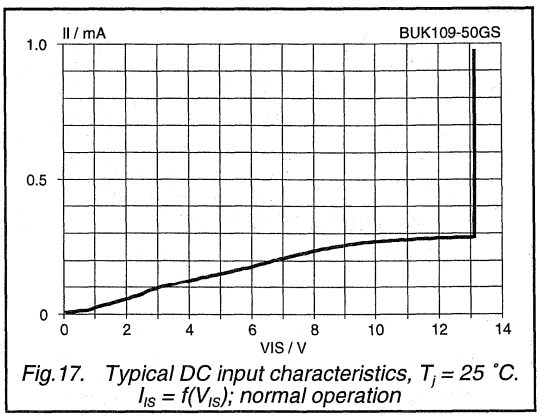


Fig.17. Typical DC input characteristics, $T_j = 25$ ˚C. $I_{IS} = f(V_{IS})$; normal operation

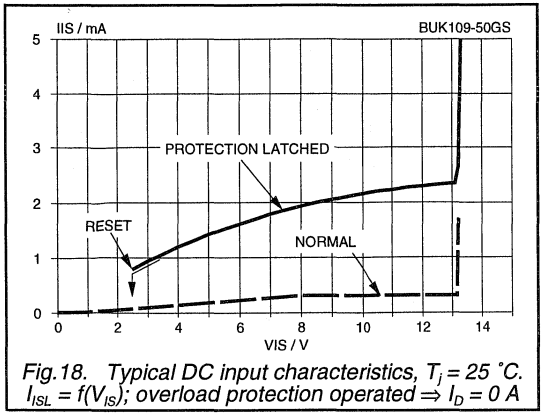


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

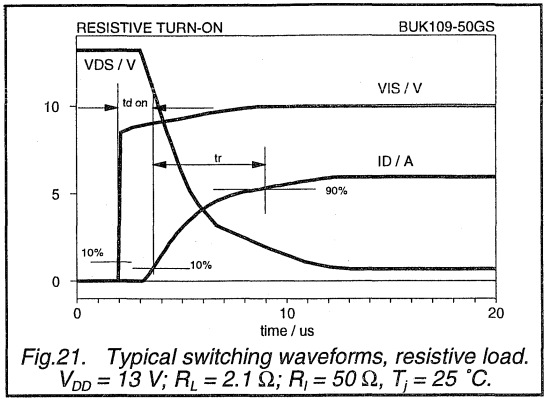


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

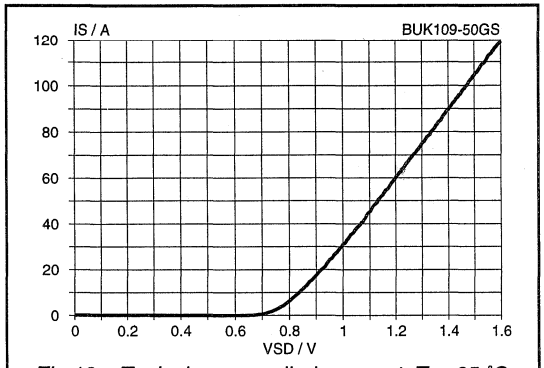


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

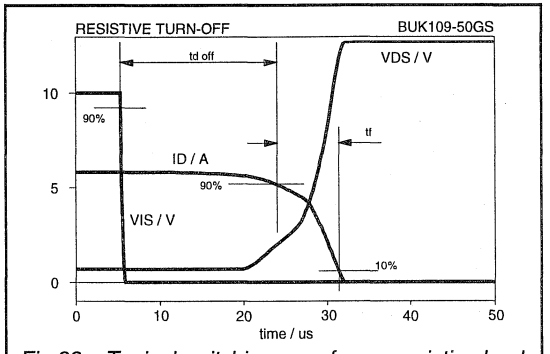


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 2.1 Ω; R_I = 50 Ω, T_j = 25 °C.

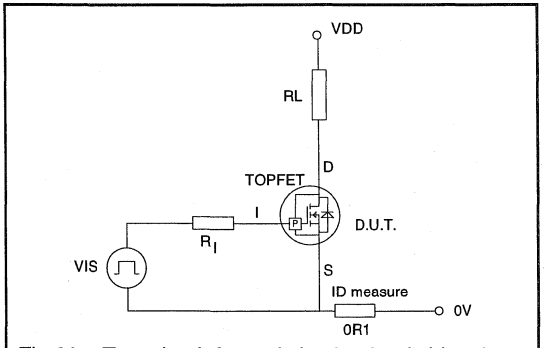


Fig.20. Test circuit for resistive load switching times.

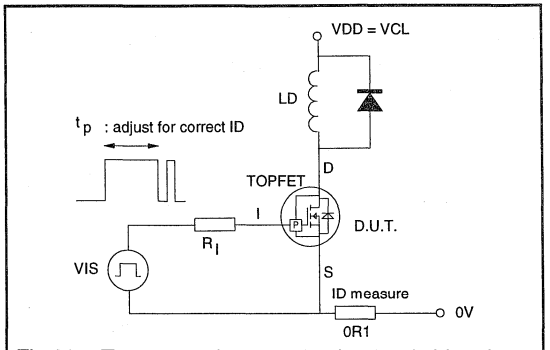


Fig.23. Test circuit for inductive load switching times.

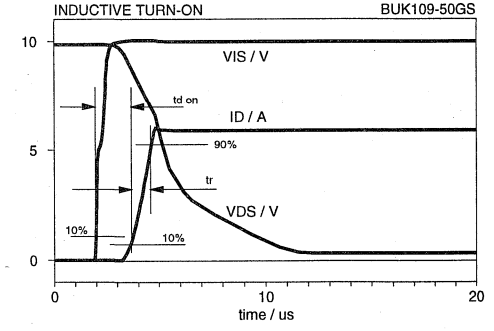


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_l = 50 Ω, T_j = 25 °C.

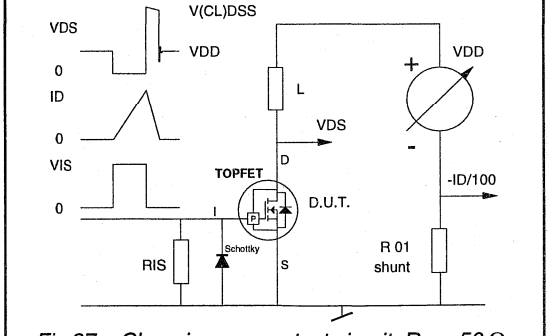


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

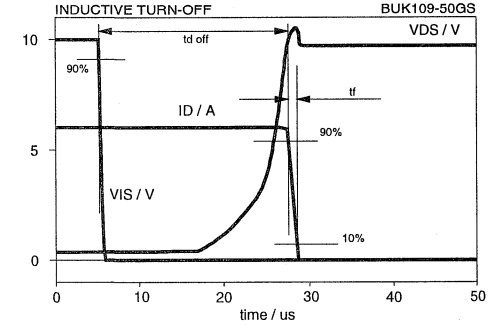


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 10 V; I_D = 6 A; R_l = 50 Ω, T_j = 25 °C.

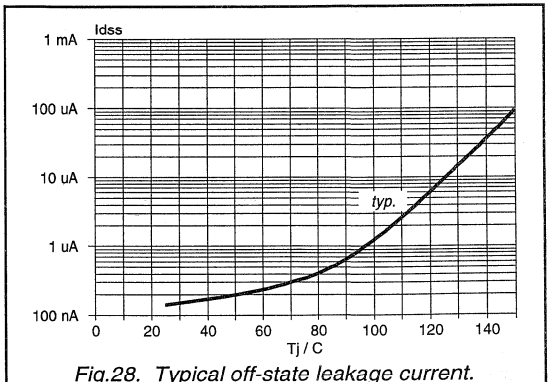


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

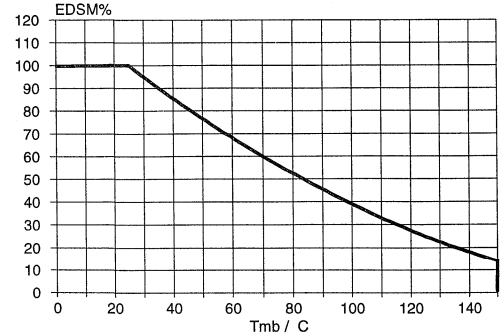


Fig.26. Normalised limiting clamping energy. E_{DSM}% = $f(T_{mb})$; conditions: I_D = 27 A; V_{IS} = 10 V

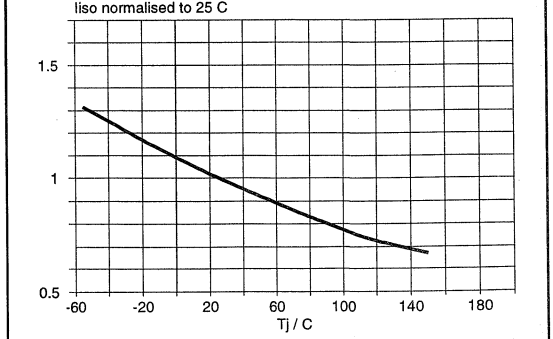


Fig.29. Normalised input current (normal operation). I_{IS}/I_{IS}25 °C = $f(T_j)$; V_{IS} = 10 V

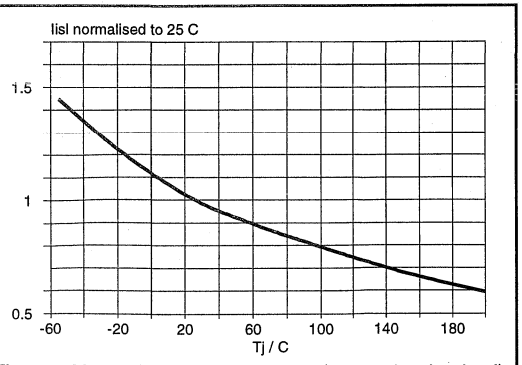


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^{\circ}C = f(T_j)$; V_{IS} = 10 V

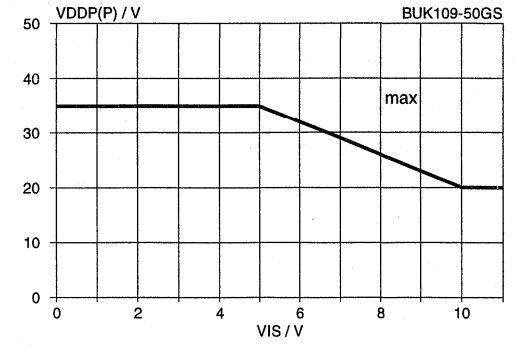


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^{\circ}C$

PowerMOS transistor
Logic level TOPFET

BUK110-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER		MAX.	UNIT
V_{DS}	Continuous drain source voltage		50	V
I_D	Continuous drain current		45	A
P_D	Total power dissipation		125	W
T_j	Continuous junction temperature		150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		35	mΩ
I_{ISL}	Input supply current	V_{IS} = 5 V	650	μA

FUNCTIONAL BLOCK DIAGRAM

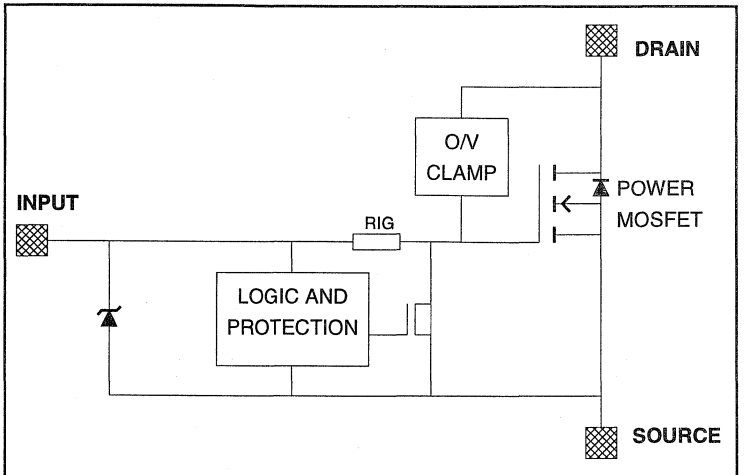
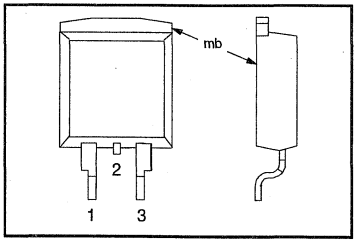


Fig.1. Elements of the TOPFET.

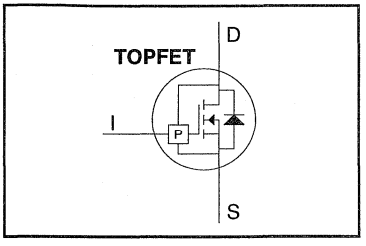
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; $V_{IS} = 5$ V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; $V_{IS} = 5$ V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5$ V	-	50	V
	Short circuit load protection[4]				
$V_{DDP(P)}$	Protected drain source supply voltage[5]	$V_{IS} = 5$ V	-	16	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25$ °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0$ V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; $I_{DM} = 25$ A; $V_{DD} \leq 20$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

5 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 25 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[2]	T_{mb} = 25 °C; L ≤ 10 µH; R_L = 10 mΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
$I_{D(SC)}$	Drain current[3]	V_{DD} = 13 V; V_{IS} = 5 V	-	75	-	A
$I_{DM(SC)}$	Peak drain current[4]	V_{IS} = 5 V; V_{DD} = 13 V	-	200	-	A
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \geq 2$ A[5]	150	-	-	°C

TRANSFER CHARACTERISTIC

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S

1 Continuous input voltage. The specified pulse width is for the drain current.

2 Refer to OVERLOAD PROTECTION LIMITING VALUES.

3 Continuous drain-source supply voltage. Pulsed input voltage.

4 Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

5 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	100	200	350	µA
			V_{IS} = 4 V	-	160	270	µA
V_{ISR}	Protection reset voltage[1]		T_j = 25 °C	2.0	2.6	3.5	V
			T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	330	650	µA
			V_{IS} = 3.5 V	-	240	430	µA
$V_{(BR)IS}$	Input breakdown voltage	I_I = 10 mA		6	-	-	V
R_{IG}	Input series resistance		T_j = 25 °C	-	33	-	kΩ
	to gate of power MOSFET		T_j = 150 °C	-	50	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	30	-	µs
t_r	Rise time	resistive load R_L = 2.1 Ω	-	150	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	120	-	µs
t_f	Fall time	resistive load R_L = 2.1 Ω	-	120	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25$ °C; V_{IS} = 0 V	-	45	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	I_S = 45 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 The input voltage below which the overload protection circuits will be reset.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

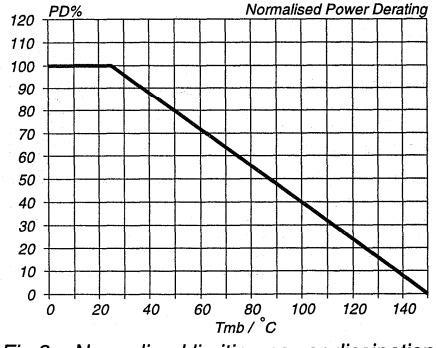


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

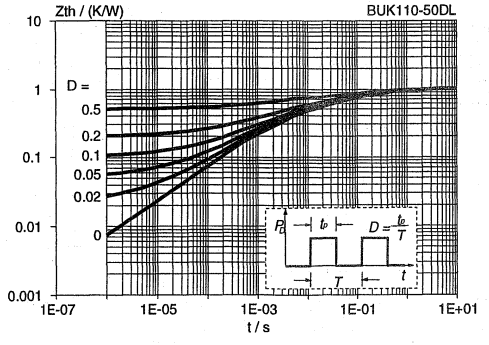


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

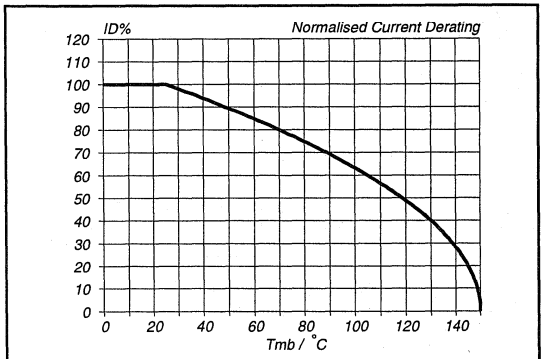


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; *conditions:* $V_{IS} = 5$ V

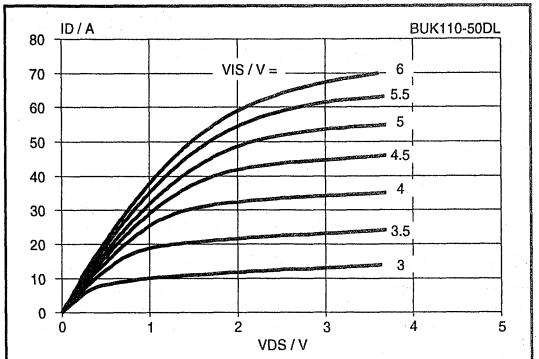


Fig.6. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; *parameter* V_{IS}; $t_p = 2$ *ms*

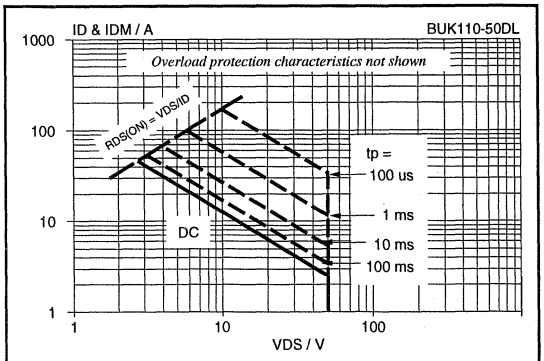


Fig.4. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

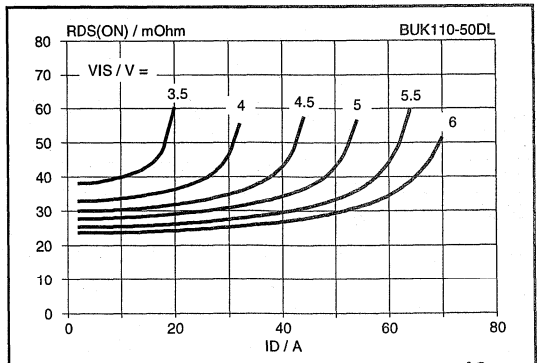


Fig.7. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; *parameter* V_{IS}; $t_p = 2$ *ms*

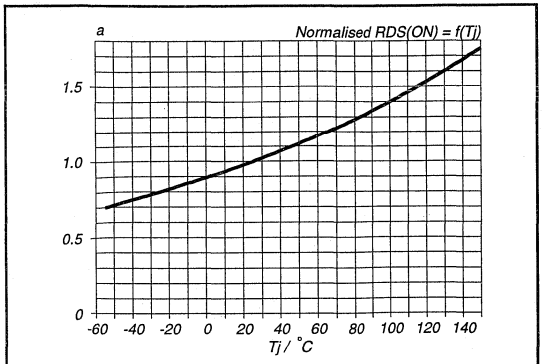


Fig.8. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; $I_D = 25$ A; $V_{IS} = 5$ V

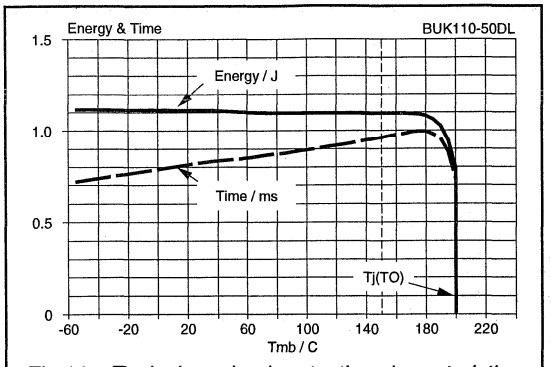


Fig.11. Typical overload protection characteristics. Conditions: $V_{DD} = 13$ V; $V_{IS} = 5$ V; SC load = 30 mΩ

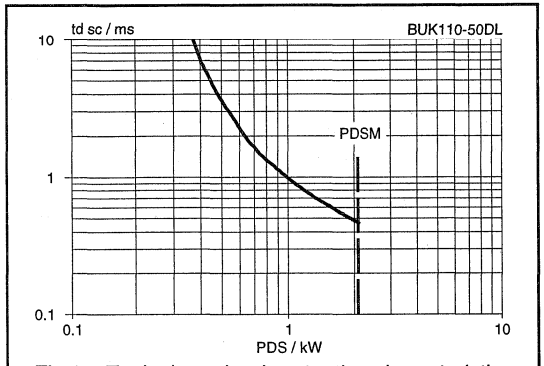


Fig.9. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; $T_j = 25\ ^\circ C$.

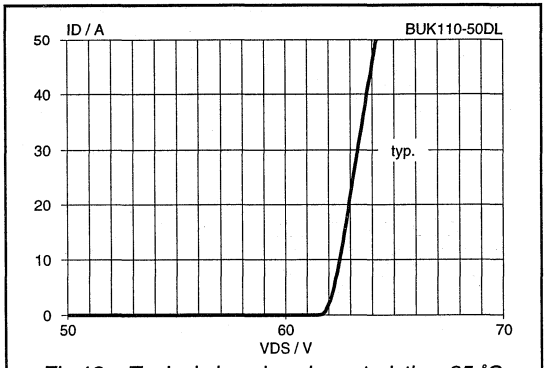


Fig.12. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50\ \mu s$

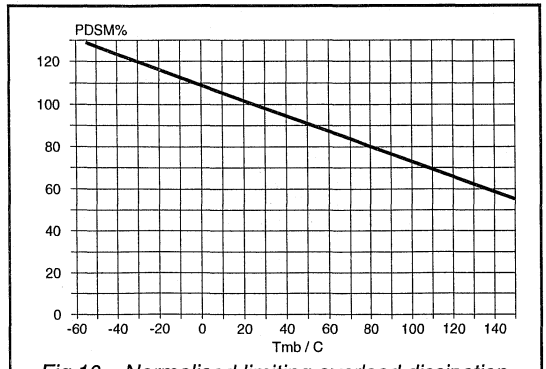


Fig.10. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

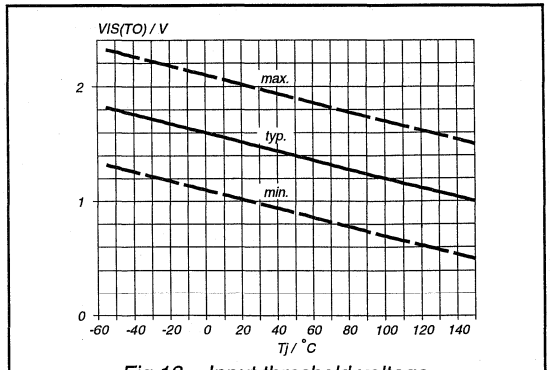


Fig.13. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

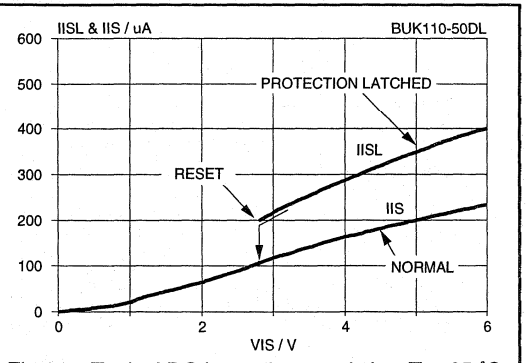


Fig.14. Typical DC input characteristics, T_j = 25 °C. I_{ISL} & I_{IS} = f(V_{IS}); protection latched & normal operation

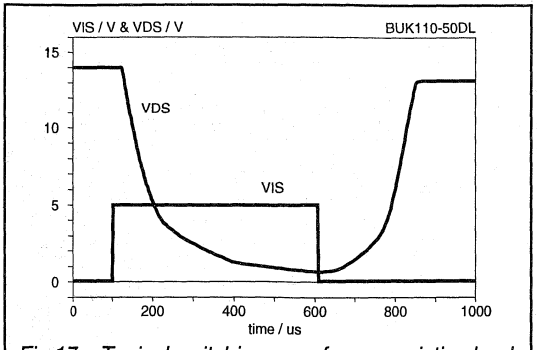


Fig.17. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 °C.

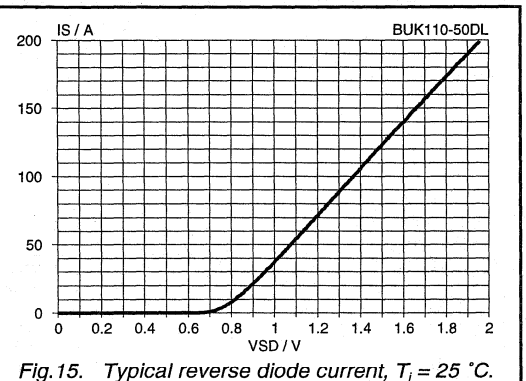


Fig.15. Typical reverse diode current, T_j = 25 °C. I_S = f(V_{SDS}); conditions: V_{IS} = 0 V; t_p = 250 µs

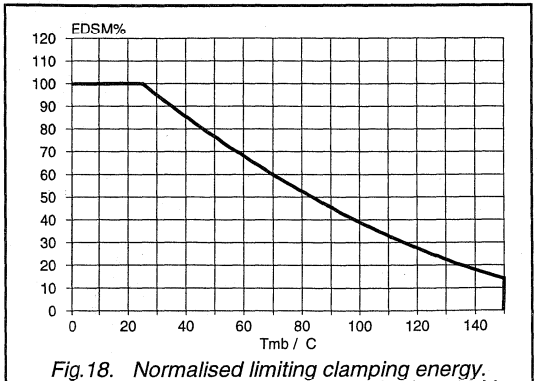


Fig.18. Normalised limiting clamping energy. E_{DSM}% = f(T_{mb}); conditions: I_D = 25 A; V_{IS} = 10 V

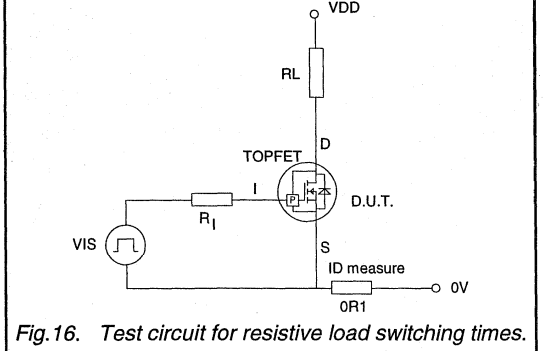


Fig.16. Test circuit for resistive load switching times.

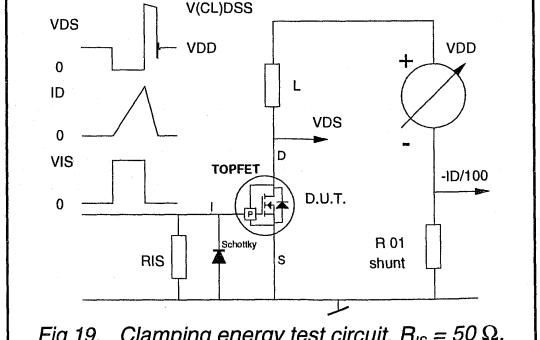


Fig.19. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

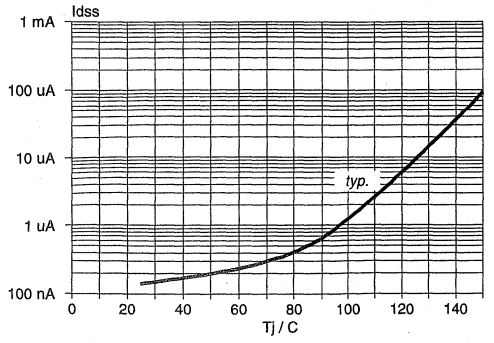


Fig.20. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

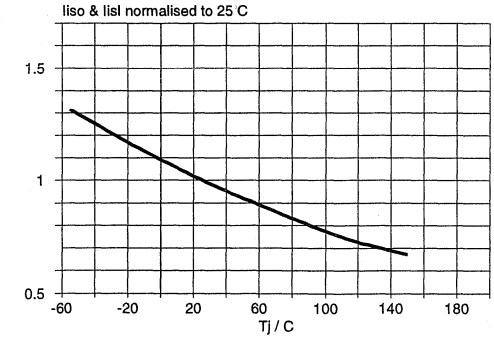


Fig.21. Normalised input currents (normal & latched). $I_{ISO}/I_{ISO}25^{\circ}C$ & $I_{ISL}/I_{ISL}25^{\circ}C = f(T_j)$; V_{IS} = 5 V

PowerMOS transistor Logic level TOPFET

BUK110-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	45	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 5 V	35	mΩ

FUNCTIONAL BLOCK DIAGRAM

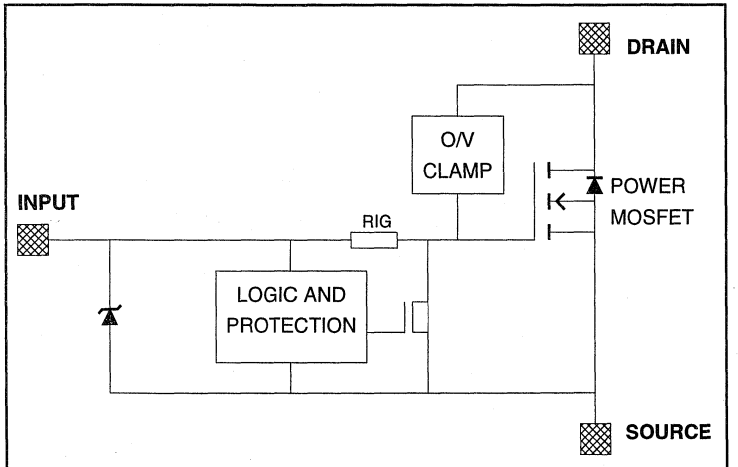
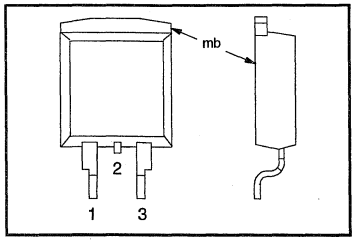


Fig.1. Elements of the TOPFET.

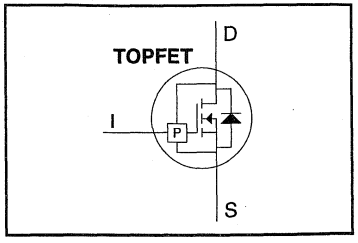
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 5 V	-	28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 5 V	-	180	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 5 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	45	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \le 300\ \mu s$; $\delta \le 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V	-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; V_{IS} = 5 V; $t_p \le 300\ \mu s$; $\delta \le 0.01$	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 5 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V; from $I_D \ge 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 5 V; normal operation	-	0.2	0.35	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 5 V; protection latched	2	3.8	10	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	6	-	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq$ 300 µs; $\delta \leq$ 0.01	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 5 V	-	60	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_I = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	2	-	µs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	8	-	µs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	8	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 5 V	-	3.7	-	µs
t_r	Rise time	inductive load I_{DM} = 11 A	-	3.7	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	µs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

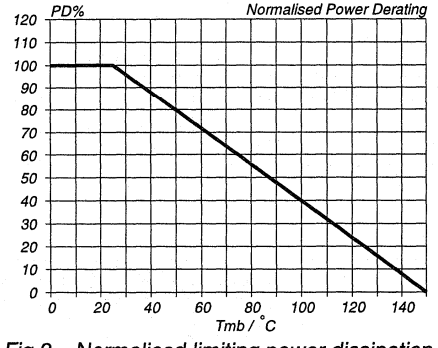


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

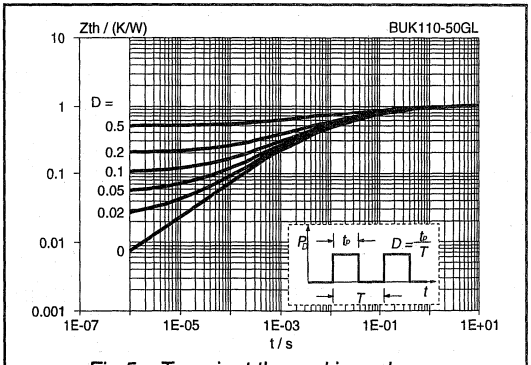


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

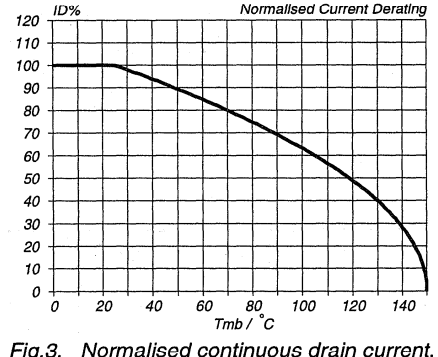


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

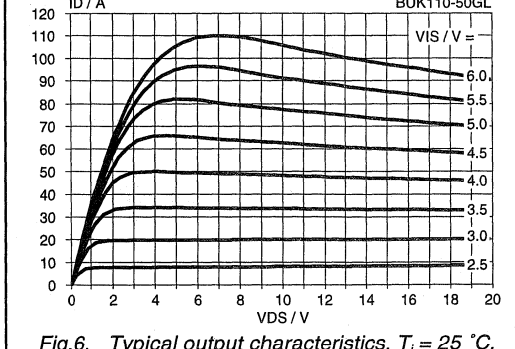


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

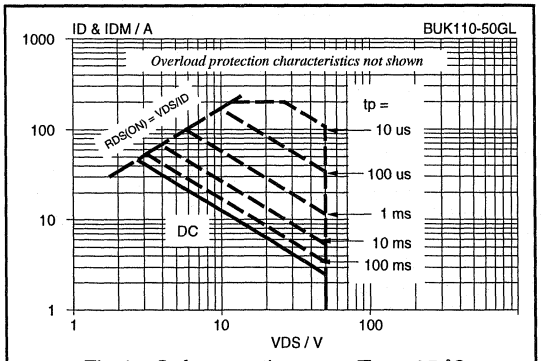


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

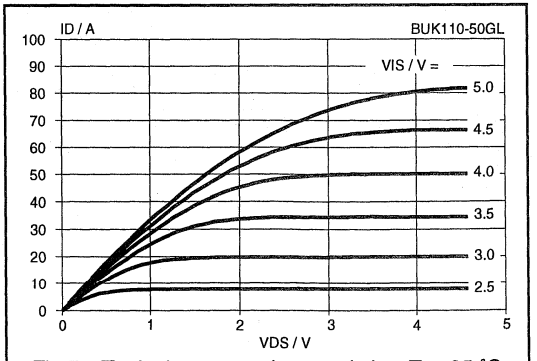


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

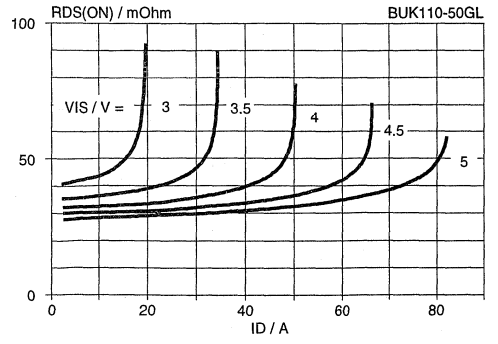


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

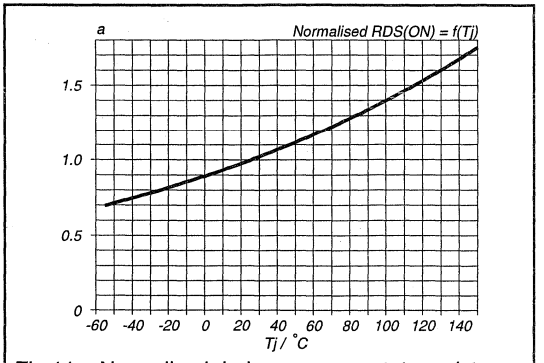


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; I_D = 25 A; V_{IS} = 5 V

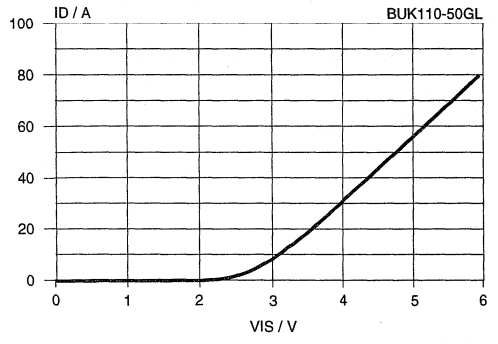


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

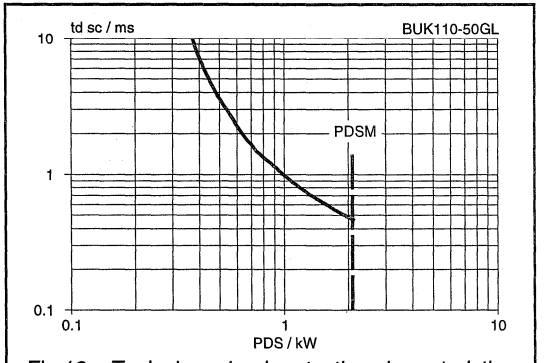


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq 4$ V; T_j = 25 ˚C.

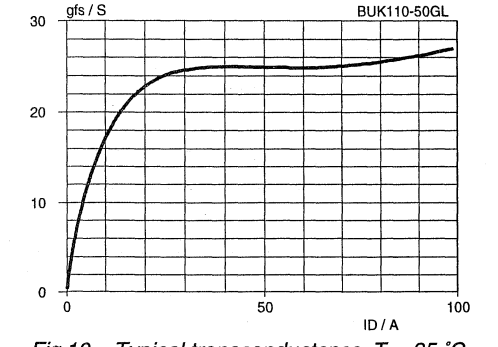


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

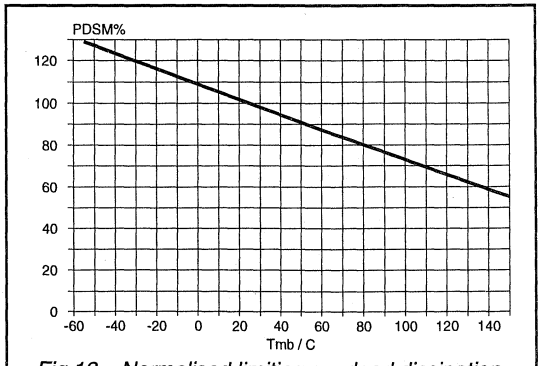


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

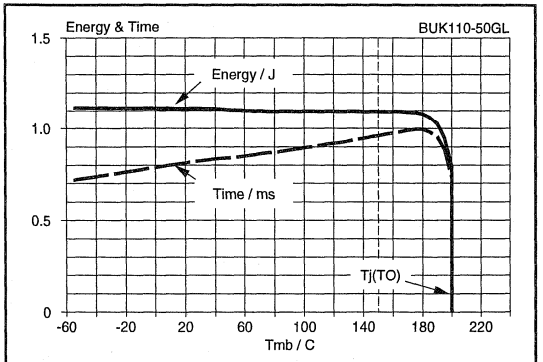


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 5 V; SC load = 30 mΩ

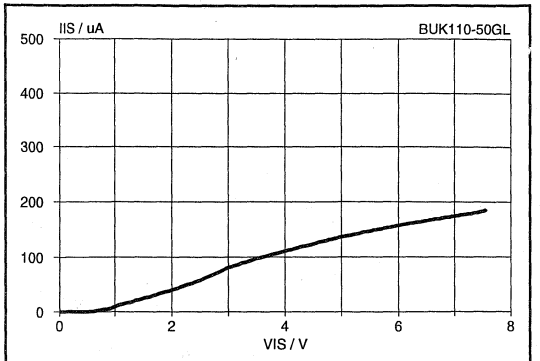


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

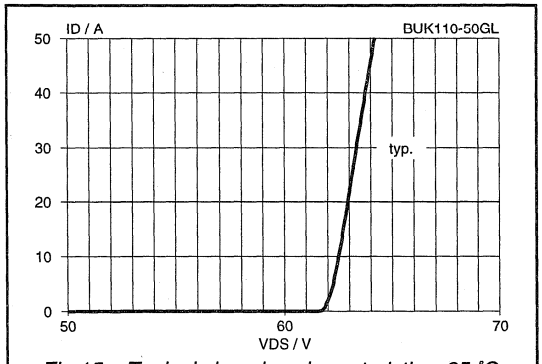


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

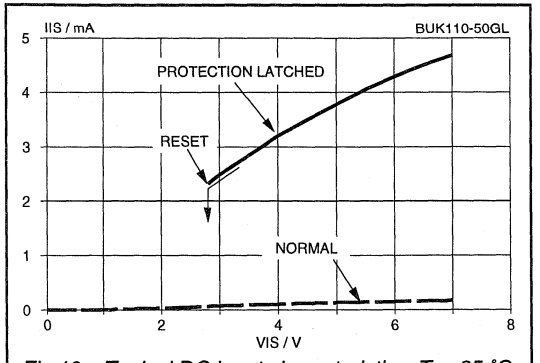


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

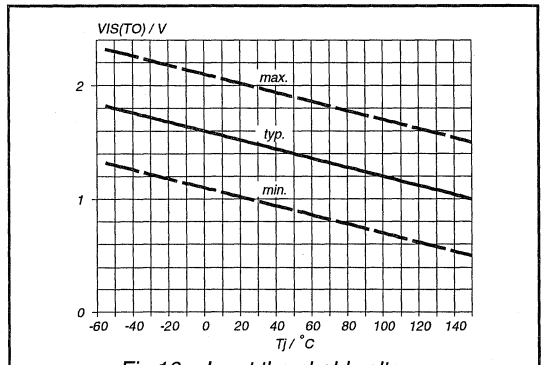


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

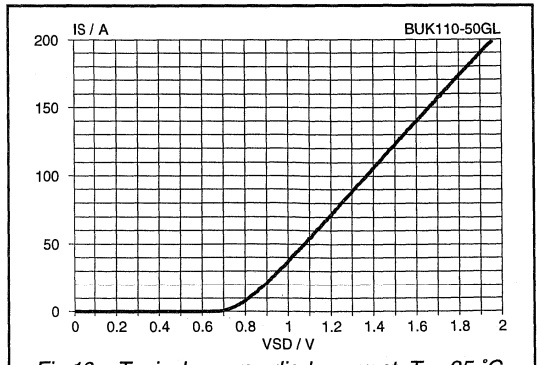


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

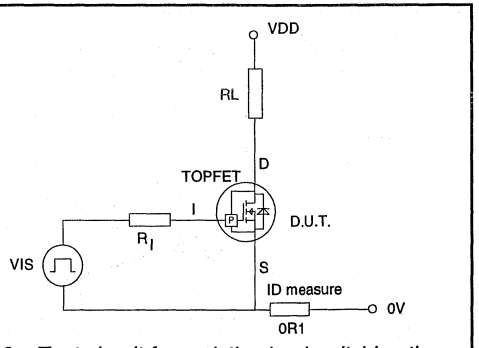


Fig.20. Test circuit for resistive load switching times.

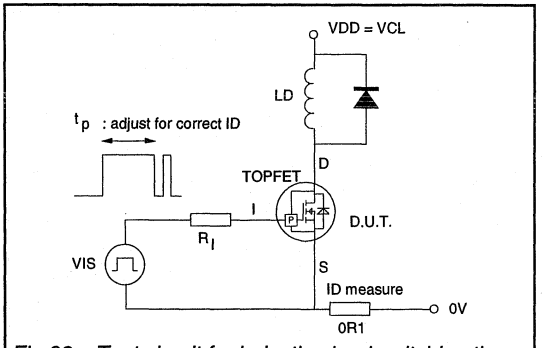


Fig.23. Test circuit for inductive load switching times.

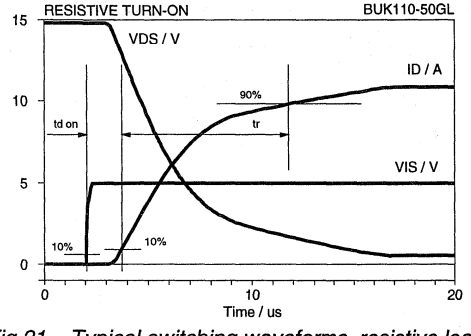


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

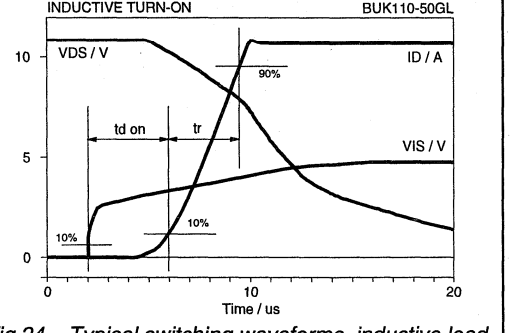


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 ˚C.

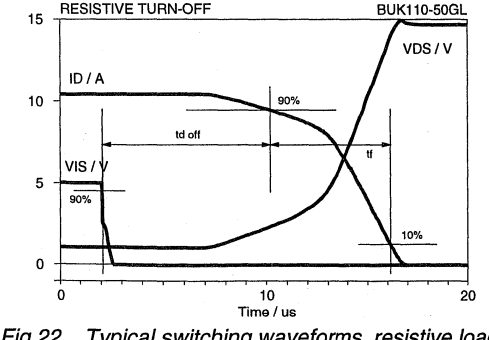


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

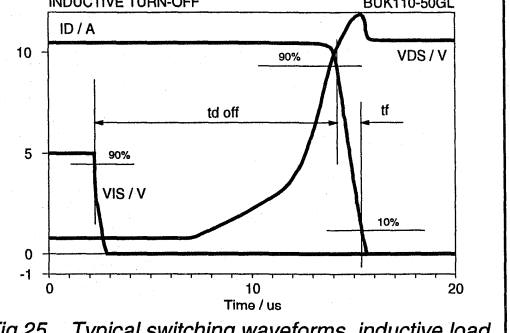


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 ˚C.

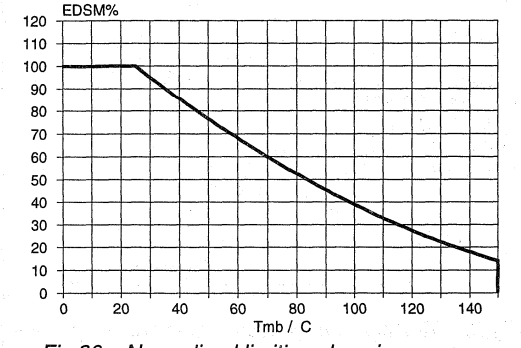


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: I_D = 25 A; V_{IS} = 10 V

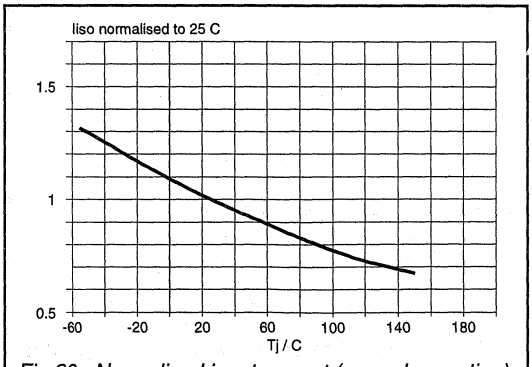


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

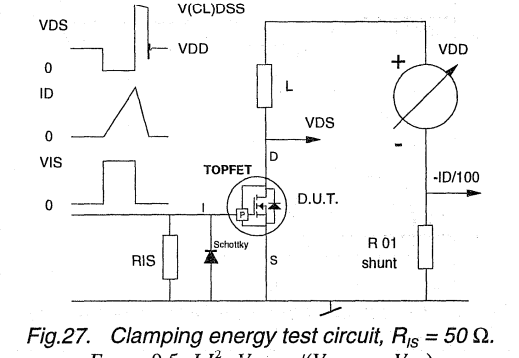


Fig.27. Clamping energy test circuit, R_{IS} = 50 Ω.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

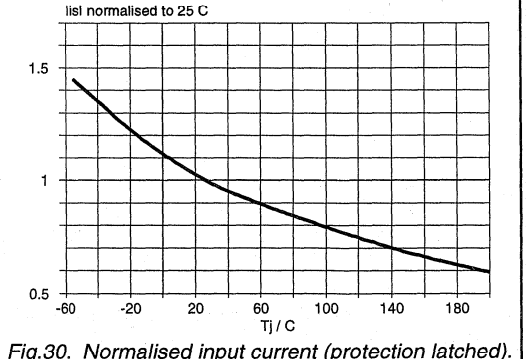


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^\circ C = f(T_j)$; V_{IS} = 5 V

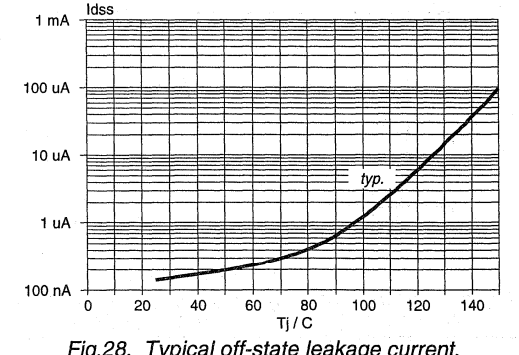


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; I_{IS} = 0 V.

PowerMOS transistor TOPFET

BUK110-50GS

DESCRIPTION

Monolithic temperature and overload protected power MOSFET in a 3 pin plastic surface mount envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 10 V input level
- Low threshold voltage also allows 5 V control
- Control of power MOSFET and supply of overload protection circuits derived from input
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_D	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{IS} = 10 V	28	mΩ

FUNCTIONAL BLOCK DIAGRAM

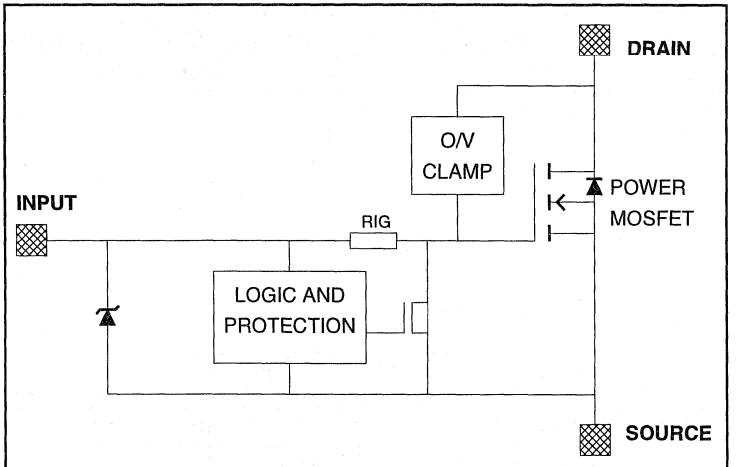
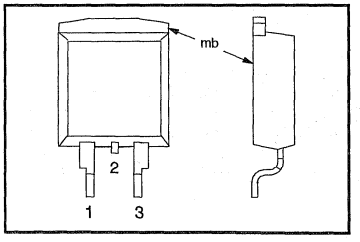


Fig.1. Elements of the TOPFET.

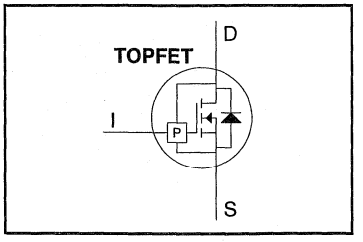
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	50	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C; V_{IS} = 10 V	-	31	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C; V_{IS} = 10 V	-	200	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature[2]	normal operation	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	5	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V	-	50	V
	Short circuit load protection				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V	-	16	V
		V_{IS} = 5 V	-	24	V
P_{DSM}	Instantaneous overload dissipation	T_{mb} = 25 °C	-	2.1	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	V_{IS} = 0 V	-	50	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25$ °C; I_{DM} = 25 A; $V_{DD} \leq 25$ V; inductive load	-	1	J
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 85$ °C; I_{DM} = 16 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	80	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The input voltage for which the overload protection circuits are functional.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA		50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 4 A; $t_p \le 300$ µs; $\delta \le 0.01$		-	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 50 V; V_{IS} = 0 V		-	1	20	µA
I_{DSS}	Zero input voltage drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 125 °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 25 A; $t_p \le 300$ µs; $\delta \le 0.01$	V_{IS} = 10 V	-	22	28	mΩ
			V_{IS} = 5 V	-	30	35	mΩ

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	T_{mb} = 25 °C; L ≤ 10 µH				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	1.1	-	J
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	0.8	-	ms
	Over temperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 10 V; from $I_D \ge 2$ A[2]	150	-	-	°C

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
I_{IS}	Input supply current	V_{IS} = 10 V; normal operation	-	0.4	1.0	mA
V_{ISR}	Protection reset voltage[3]		2.0	2.6	3.5	V
V_{ISR}	Protection reset voltage	T_j = 150 °C	1.0	-	-	
I_{ISL}	Input supply current	V_{IS} = 10 V; protection latched	2	6	20	mA
$V_{(BR)IS}$	Input clamp voltage	I_I = 10 mA	11	13	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	1.5	-	kΩ

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum. Refer to OVERLOAD PROTECTION LIMITING VALUES.

2 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

3 The input voltage below which the overload protection circuits will be reset.

TRANSFER CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 25 A $t_p \leq$ 300 µs; $\delta \leq$ 0.01	17	28	-	S
$I_{D(SC)}$	Drain current[1]	V_{DS} = 13 V; V_{IS} = 10 V	-	150	-	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C. R_l = 50 Ω. Refer to waveform figures and test circuits.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	resistive load R_L = 1.1 Ω	-	5.5	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	13	-	µs
t_f	Fall time	resistive load R_L = 1.1 Ω	-	9	-	µs
$t_{d\,on}$	Turn-on delay time	V_{DD} = 13 V; V_{IS} = 10 V	-	1.5	-	µs
t_r	Rise time	inductive load I_{DM} = 11 A	-	1.3	-	µs
$t_{d\,off}$	Turn-off delay time	V_{DD} = 13 V; V_{IS} = 0 V	-	18	-	µs
t_f	Fall time	inductive load I_{DM} = 11 A	-	1.4	-	µs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq$ 25 °C; V_{IS} = 0 V	-	50	A

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 50 A; V_{IS} = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[2]	-	-	-	-

ENVELOPE CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from upper edge of tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

1 During overload before short circuit load protection operates.

2 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

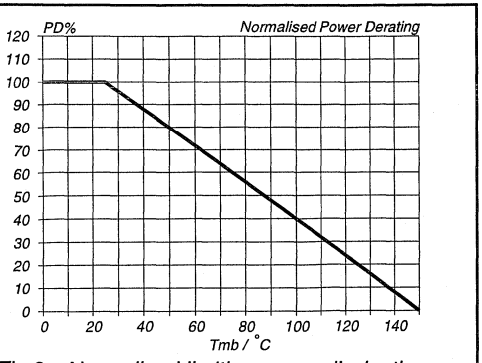


Fig.2. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D / P_D(25\ ^\circ C) = f(T_{mb})$

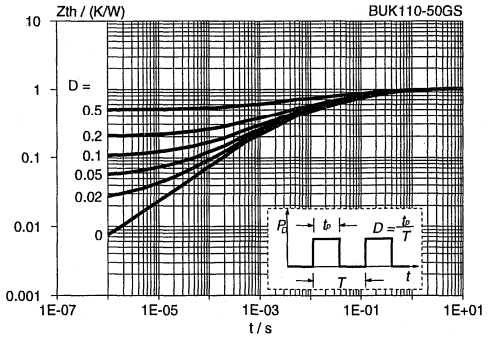


Fig.5. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

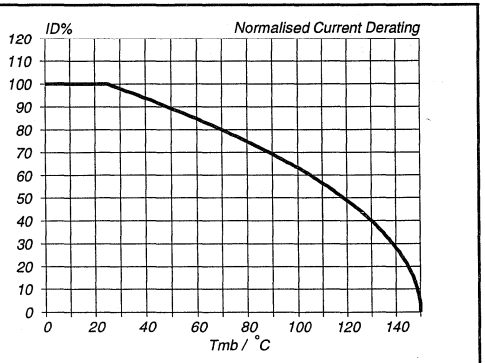


Fig.3. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D / I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

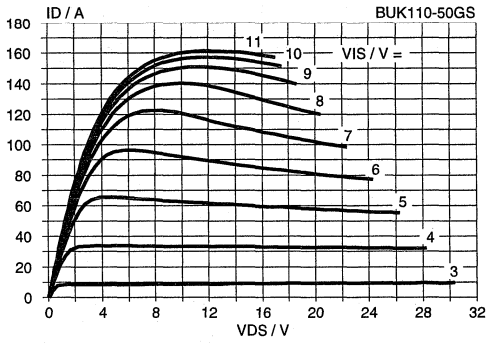


Fig.6. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

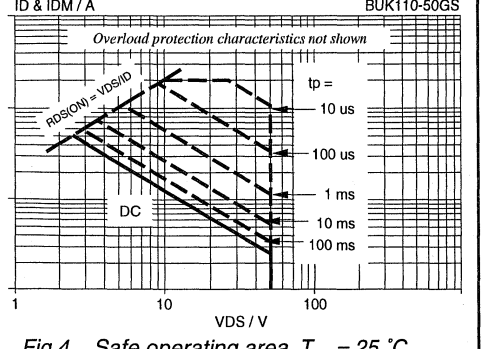


Fig.4. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

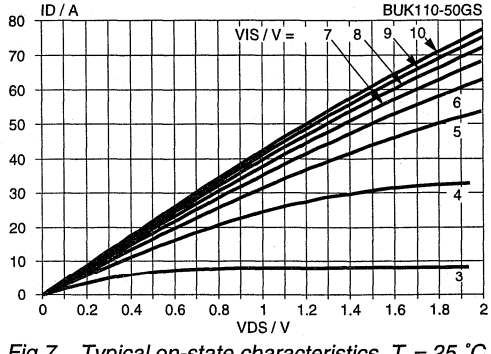


Fig.7. Typical on-state characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

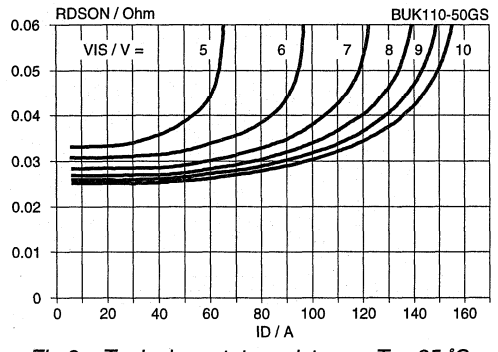


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

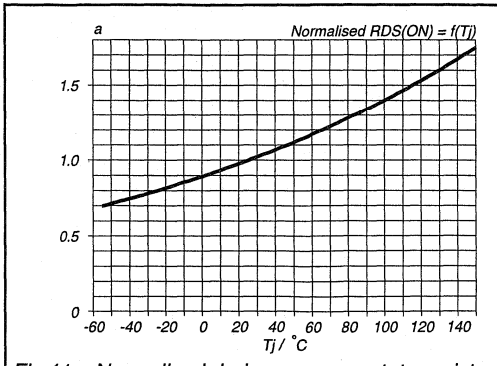


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25$ ˚C = $f(T_j)$; I_D = 25 A; V_{IS} = 10 V

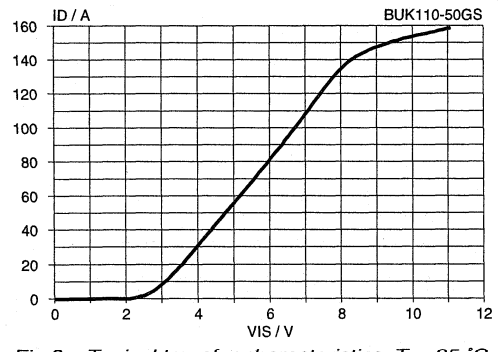


Fig.9. Typical transfer characteristics, T_j = 25 ˚C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

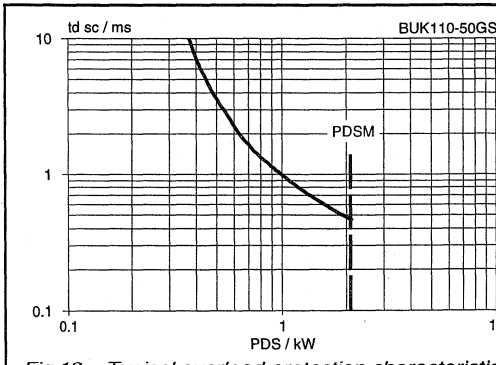


Fig.12. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{IS} \geq$ 5 V; T_j = 25 ˚C.

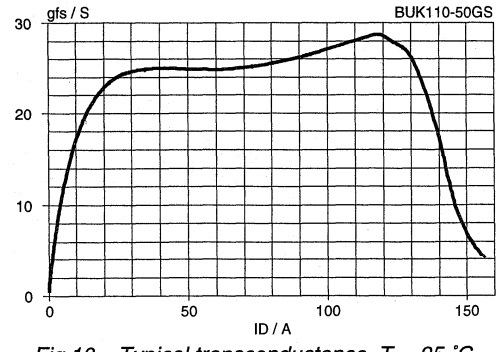


Fig.10. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

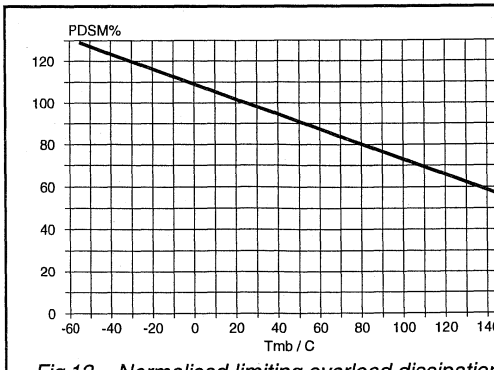


Fig.13. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ^\circ C) = f(T_{mb})$

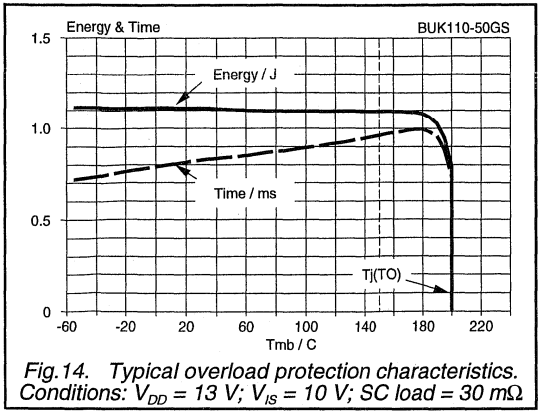


Fig.14. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; V_{IS} = 10 V; SC load = 30 mΩ

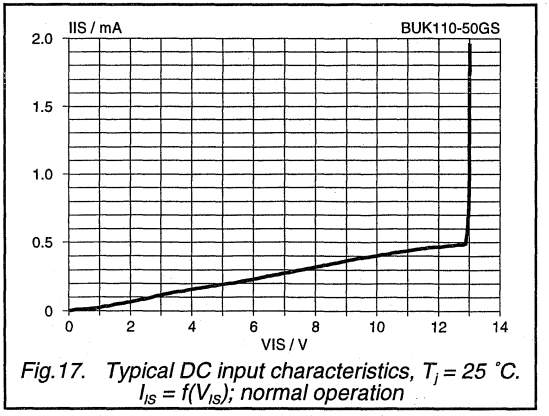


Fig.17. Typical DC input characteristics, T_j = 25 °C. $I_{IS} = f(V_{IS})$; normal operation

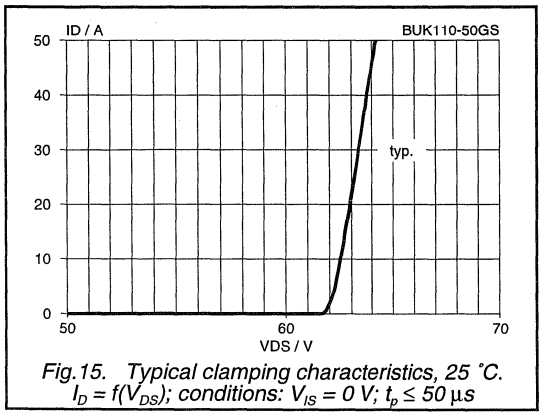


Fig.15. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: V_{IS} = 0 V; $t_p \leq 50$ µs

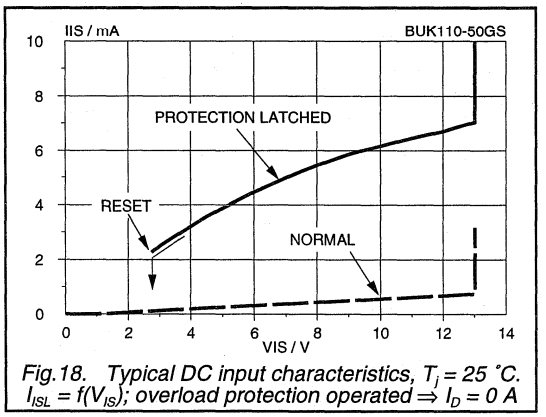


Fig.18. Typical DC input characteristics, T_j = 25 °C. $I_{ISL} = f(V_{IS})$; overload protection operated ⇒ I_D = 0 A

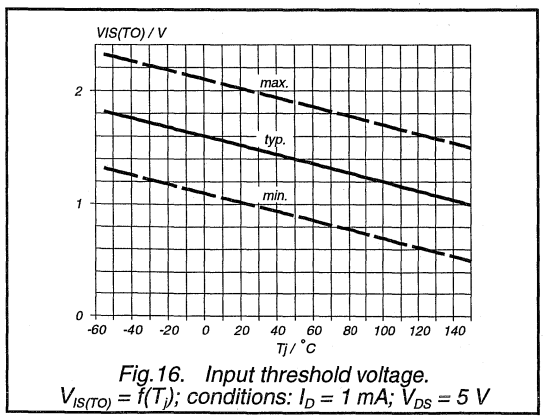


Fig.16. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

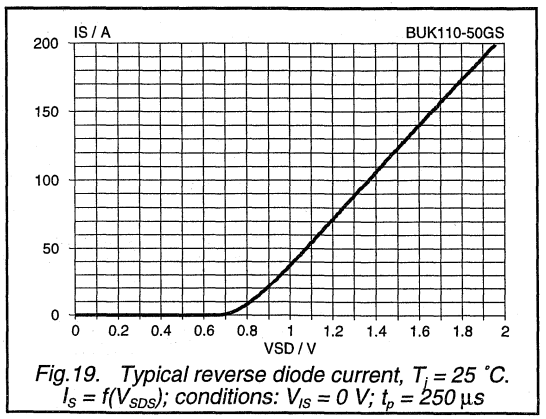


Fig.19. Typical reverse diode current, T_j = 25 °C. $I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

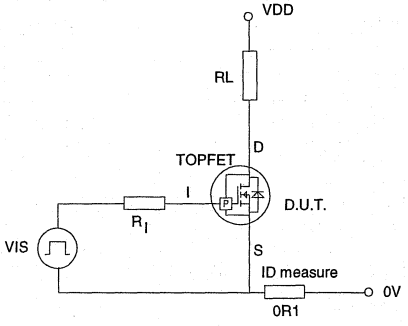


Fig.20. Test circuit for resistive load switching times.

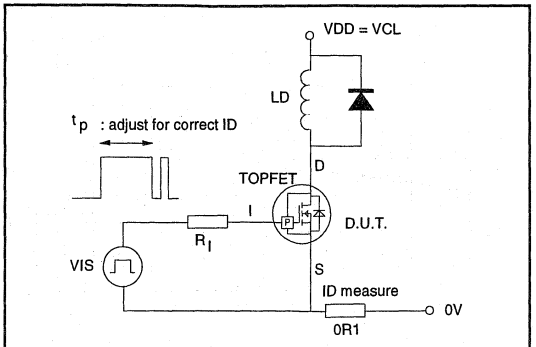


Fig.23. Test circuit for inductive load switching times.

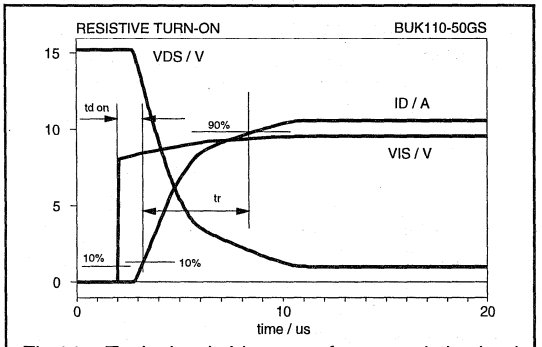


Fig.21. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

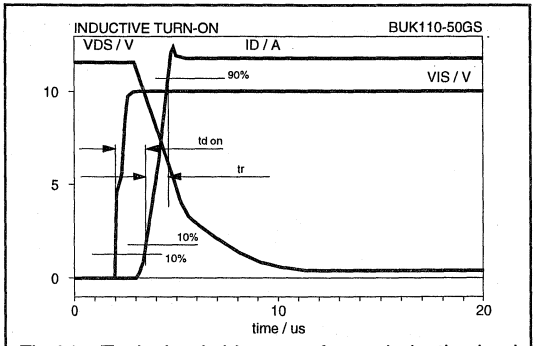


Fig.24. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 ˚C.

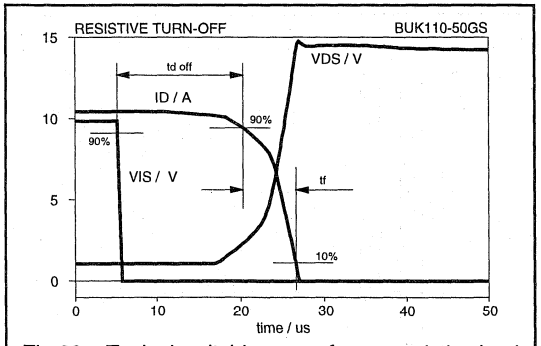


Fig.22. Typical switching waveforms, resistive load. V_{DD} = 13 V; R_L = 1.1 Ω; R_I = 50 Ω, T_j = 25 ˚C.

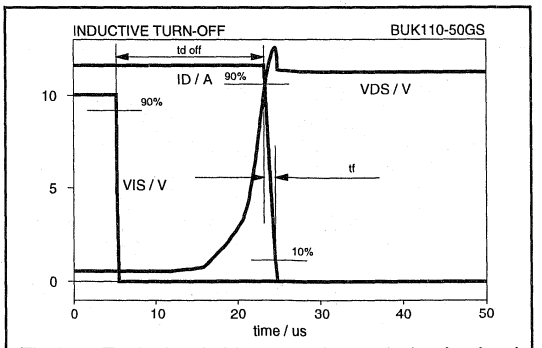


Fig.25. Typical switching waveforms, inductive load. V_{DD} = 13 V; I_D = 11 A; R_I = 50 Ω, T_j = 25 ˚C.

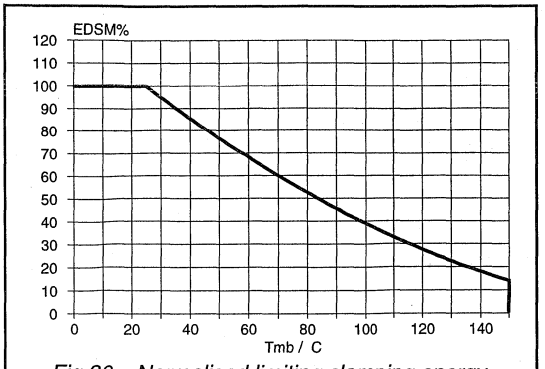


Fig.26. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: $I_D = 25$ A; $V_{IS} = 10$ V

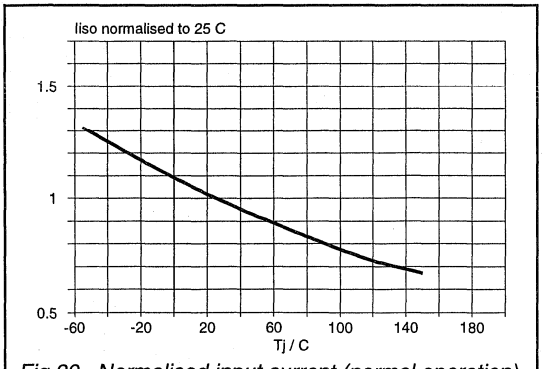


Fig.29. Normalised input current (normal operation). $I_{IS}/I_{IS}25\ ^\circ C = f(T_j)$; $V_{IS} = 10$ V

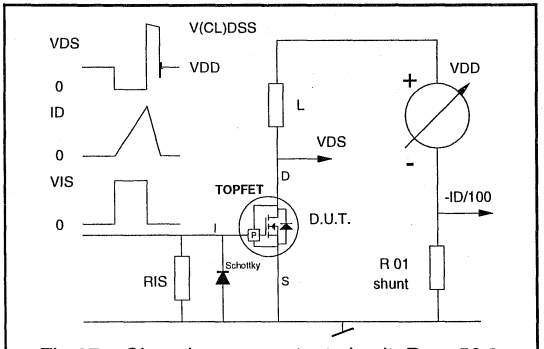


Fig.27. Clamping energy test circuit, $R_{IS} = 50\ \Omega$.

$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

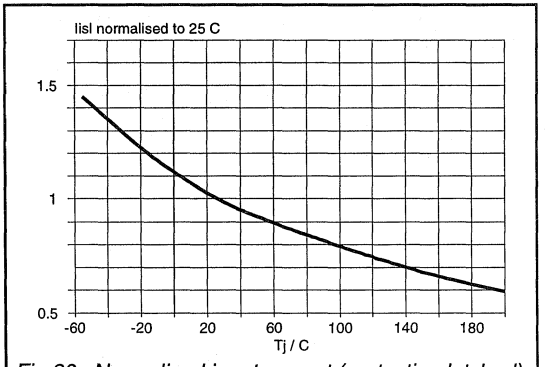


Fig.30. Normalised input current (protection latched). $I_{ISL}/I_{ISL}25\ ^\circ C = f(T_j)$; $V_{IS} = 10$ V

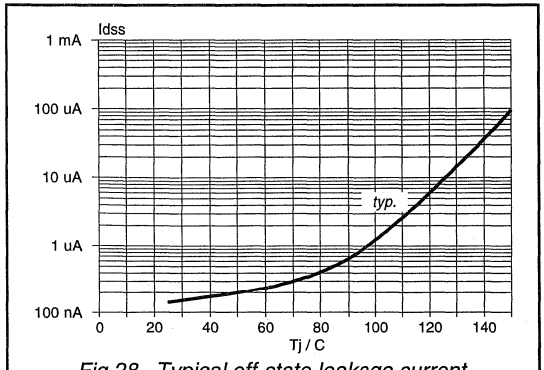


Fig.28. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $I_{IS} = 0$ V.

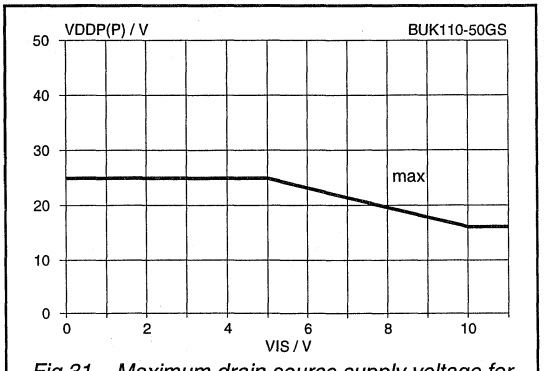


Fig.31. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150\ ^\circ C$

Logic level TOPFET
SMD version of BUK112-50GL

BUK111-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic SMD envelope, intended as a low side switch for automotive applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	12	A
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	93	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PS}	Protection supply voltage	5	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Low operating supply current
- Overtemperature protection
- Overload protection against short circuit load with drain current limiting
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- Off-state detection of open circuit load indicated by flag pin
- 5 V logic compatible input level
- Integral input resistors.
- ESD protection on all pins
- Over voltage clamping

FUNCTIONAL BLOCK DIAGRAM

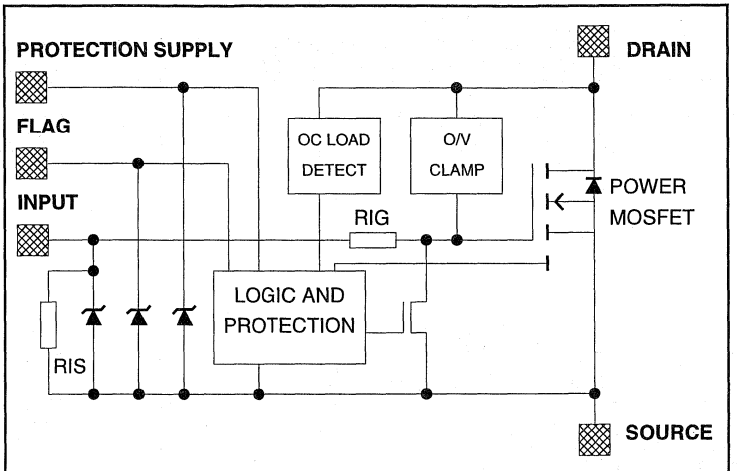


Fig.1. Elements of the TOPFET.

PINNING - SOT426

PIN	DESCRIPTION
1	input
2	flag
3	(connected to mb)
4	protection supply
5	source
mb	drain

PIN CONFIGURATION

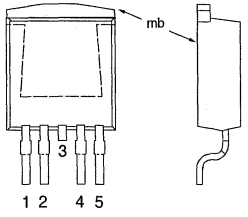


Fig. 2.

SYMBOL

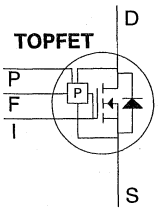


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Continuous voltage				
V_{DS}	Drain source voltage[1]	V_{IS} = 0 V	-	50	V
	Continuous currents				
I_D	Drain current	V_{PS} = 5 V; T_{mb} = 25 °C	-	self - limited	A
		V_{PS} = 0 V; T_{mb} = 94 °C	-	12	A
I_I	Input current	-	-5	5	mA
I_F	Flag current	-	-5	5	mA
I_P	Protection supply current	-	-5	5	mA
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	52	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	260	°C

ESD LIMITING VALUES

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Electrostatic discharge capacitor voltages	Human body model; C = 100 pF; R = 1.5 kΩ			
V_{C1}	Drain to source		-	4.5	kV
V_{C2}	Input, flag or protection to source		-	2	kV

OVERLOAD PROTECTION LIMITING VALUE

With the protection supply connected, TOPFET can protect itself from two types of overload - short circuit load and overtemperature.

For overload conditions an n-MOS transistor turns on between the gate and source to quickly discharge the power MOSFET gate capacitance.

The drain current is limited to reduce dissipation in case of short circuit load. Refer to OVERLOAD CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{PSP}	Protection supply voltage[3]	for valid protection	4.5	-	V

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	I_{DM} = 6 A; T_{mb} = 25°C	-	200	mJ
E_{DRM}	Repetitive clamping energy	I_{DM} = 3.1 A; $V_{DD} \leq$ 20 V; $T_{mb} \leq$ 120°C; f = 250 Hz	-	20	mJ

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	-	2.38	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

OUTPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{PS} = 0 V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Off-state					
$V_{(CL)DSS}$	Drain-source clamping voltage	I_D = 10 mA; -40°C ≤ T_{mb} ≤ 150°C	50	-	70	V
		I_{DM} = 0.75 A; t_p ≤ 300 µs; δ ≤ 0.01	50	60	70	V
I_{DSS}	Drain-source leakage current[1]	V_{IS} = 0 V; V_{DS} = 13 V	-	0.5	10	µA
		V_{DS} = 50 V	-	1	20	µA
		T_{mb} = 125 °C; V_{DS} = 40 V	-	10	100	µA
	On-state	t_p ≤ 300 µs; δ ≤ 0.01				
$R_{DS(ON)}$	Drain-source on-resistance	I_{DM} = 6 A; V_{IS} = 4.4 V; V_{PS} = 4.5 V	-	70	93	mΩ
		T_{mb} = 150 °C	-	135	165	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Normal operation					
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 13 V; V_{PS} = 0 V; I_D = 1 mA	1	1.5	2	V
		-40°C ≤ T_{mb} ≤ 150°C	0.5	-	2.5	V
I_{IS}	Input current	V_{IS} = 5 V -40°C ≤ T_{mb} ≤ 150°C	200	350	500	µA
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA	6	7.1	-	V
R_{IG}	Internal series resistance	to gate of power MOSFET	-	1.5	-	kΩ
	Overload protection latched					
I_{ISL}	Input current	V_{PS} = 5 V; V_{IS} = 5 V	1.5	3.2	4	mA

REVERSE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	Reverse drain voltage[2]	$-I_D$ = 6 A	-	0.8	-	V
$-V_{IS}$	Reverse input voltage	$-I_I$ = 5 mA	-	0.7	-	V
$-V_{PS}$	Reverse protection pin voltage	$-I_P$ = 5 mA	-	0.7	-	V
$-V_{FS}$	Reverse flag voltage	$-I_F$ = 5 mA	-	0.7	-	V

1 The drain current required for open circuit load detection is switched off when there is no protection supply, in order to ensure a low off-state quiescent current. Refer to OPEN CIRCUIT LOAD DETECTION CHARACTERISTICS.

2 Protection functions are disabled during reverse conduction.

PROTECTION SUPPLY CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Normal operation or protection latched					
I_{PS}, I_{PSL}	Supply current	V_{PS} = 4.5 V	-	330	400	µA
		-40°C ≤ T_{mb} ≤ 150°C	-	-	450	µA
$V_{(CL)PS}$	Clamping voltage	I_P = 1.5 mA	6	7.1	-	V
	Overload protection latched					
V_{PSR}	Reset voltage		-	2.1	-	V
		-40°C ≤ T_{mb} ≤ 150°C	1.5	-	3	V
t_{pr}	Reset time	V_{PS} = 0 V	-	25	-	µs
		-40°C ≤ T_{mb} ≤ 150°C	-	-	150	µs

OPEN CIRCUIT LOAD DETECTION CHARACTERISTICS

An open circuit load condition can be detected while the TOPFET is in the off-state.
-40°C ≤ T_{mb} ≤ 150°C; V_{PS} = 5 V; V_{DS} = 13 V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DSP}	Off-state drain current[1]	V_{IS} = 0 V	0.5	1.4	2	mA
I_{DSF}	Off-state drain threshold current	V_{IS} = 0 V; I_F = 100 µA	0.4	1.1	-	mA
V_{ISF}	Input threshold voltage[2]	I_F = 100 µA; I_D = 100 µA; T_{mb} = 25 °C	-	1.2	-	V

TRUTH TABLE

For normal, open-circuit load and overload conditions or inadequate protection supply voltage.

CONDITION	PROTECTION	INPUT	FLAG	OUTPUT
Normal on-state	1	1	0	1
Normal off-state	1	0	0	0
Open circuit load	1	1	0	1
Open circuit load	1	0	1	0
Short circuit load	1	1	1	0
Over temperature	1	X	1	0
Low protection supply voltage	0	1	1	1
Low protection supply voltage	0	0	1	0

For protection '0' equals low, '1' equals high.
For input '0' equals low, '1' equals high, 'X' equals don't care.
For flag '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

1 The drain source current which flows when the protection supply is high and the input is low.

2 For open circuit load indication, V_{IS} must be less than V_{ISF}.

OVERLOAD CHARACTERISTICS

T_{mb} = 25 °C; V_{PS} = 5 V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection	V_{IS} = 5 V				
I_D	Drain current limiting	V_{DS} = 13 V -40°C ≤ T_{mb} ≤ 150°C	12	24	36	A
$P_{D(TO)}$	Overload power threshold[1]	for protection to operate	-	100	-	W
E_{DSC}	Characteristic energy	which determines trip time[2]	-	200	-	mJ
I_{DM}	Peak drain current[3]	V_{DD} = 13 V; R_L ≤ 10 mΩ	-	45	-	A
	Overtemperature protection					
$T_{j(TO)}$	Threshold temperature	I_D ≥ 1 A	150	185	215	°C

FLAG CHARACTERISTICS

The flag is an open drain transistor which requires an external pull-up circuit.
T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation; V_{PS} = 5 V				
V_{FSF}	Flag voltage	I_F = 100 µA	-	0.7	-	V
		-40°C ≤ T_{mb} ≤ 150°C	-	-	0.9	V
I_{FSF}	Flag saturation current	V_{FS} = 5 V	-	10	-	mA
	Flag 'high'	overload or fault				
I_{FSO}	Flag leakage current	V_{FS} = 5 V	-	0.1	1	µA
		T_{mb} = 150°C	-	1	10	µA
$V_{(CL)FS}$	Flag clamping voltage	I_F = 100 µA	6	6.9	-	V
V_{PSF}	Protection supply threshold voltage[4]	I_F = 100 µA; V_{DS} = 5 V	2.5	3	4	V
		-40°C ≤ T_{mb} ≤ 150°C	2	-	4	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} = 5 V	-	50	-	kΩ

1 Refer to figure 15.

2 Trip time $t_{d\,sc} \approx E_{DSC} / [P_D - P_{D(TO)}]$. Refer also to figure 15.

3 For short circuit load connected after turn-on.

4 When V_{PS} is less than V_{PSF} the flag pin indicates low protection supply voltage. Refer to TRUTH TABLE.

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Resistive load	R_L = 4 Ω; I_D = 3 A				
$t_{d\,on}$	Turn-on delay time	V_{IS}: 0 V ⇒ 5 V	-	0.6	-	µs
t_r	Rise time		-	2.8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS}: 5 V ⇒ 0 V	-	3.5	-	µs
t_f	Fall time		-	3.2	-	µs
	Inductive load	I_D = 3 A; V_{DD} = 13 V; with freewheel diode				
$t_{d\,on}$	Turn-on delay time	V_{IS}: 0 V ⇒ 5 V	-	0.9	-	µs
t_r	Rise time		-	1.2	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS}: 5 V ⇒ 0 V	-	6.7	-	µs
t_f	Fall time		-	0.6	-	µs

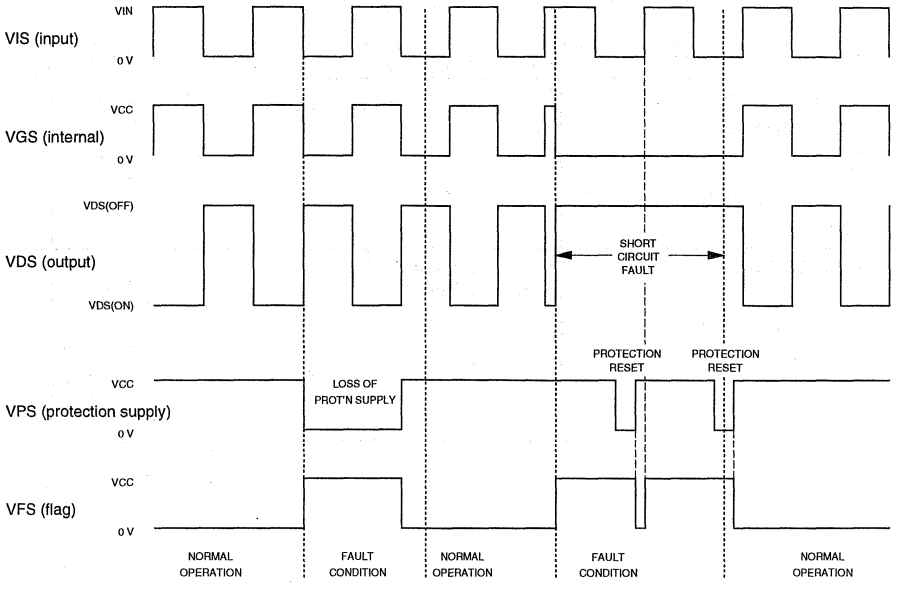


Fig. 4. Waveforms for normal and fault conditions.

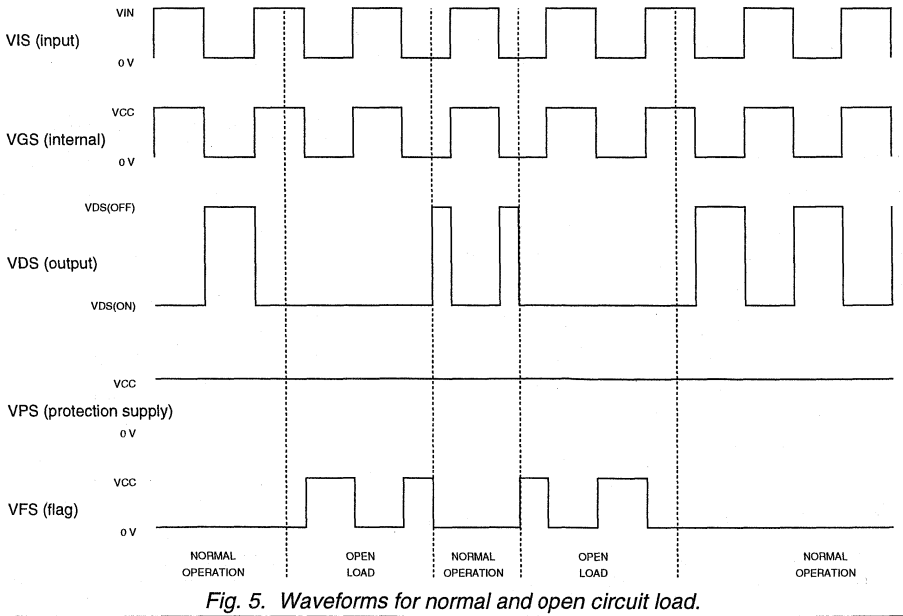


Fig. 5. Waveforms for normal and open circuit load.

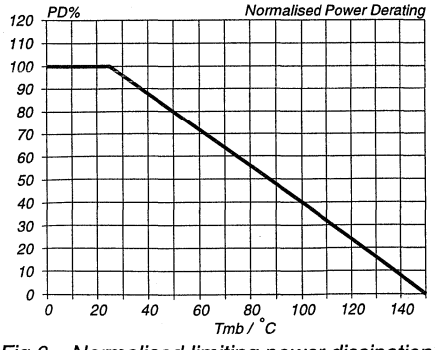


Fig.6. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25^\circ C) = f(T_{mb})$

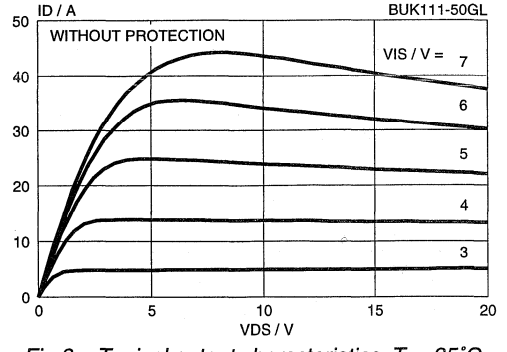


Fig.9. Typical output characteristics, $T_j = 25^\circ C$.
$I_D = f(V_{DS})$; $t_p = 250\ \mu s$; $V_{PS} = 0\ V$; parameter V_{IS}

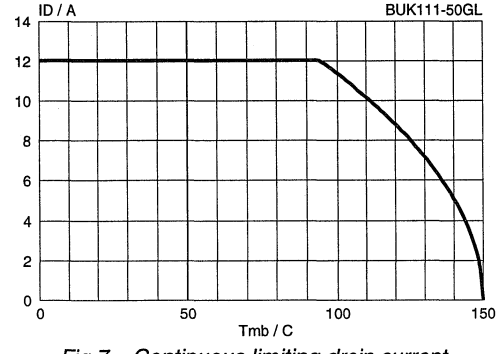


Fig.7. Continuous limiting drain current.
$I_D = f(T_{mb})$; conditions: $V_{IS} = 5\ V$; $V_{PS} = 5\ V$

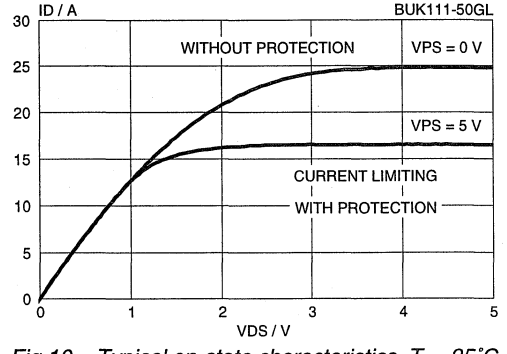


Fig.10. Typical on-state characteristics, $T_j = 25^\circ C$.
$I_D = f(V_{DS})$; $V_{IS} = 5\ V$; $t_p = 250\ \mu s$; parameter V_{PS}

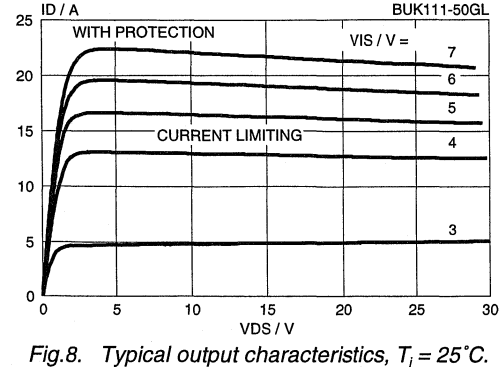


Fig.8. Typical output characteristics, $T_j = 25^\circ C$.
$I_D = f(V_{DS})$; $t_p = 250\ \mu s$; $V_{PS} = 5\ V$; parameter V_{IS}

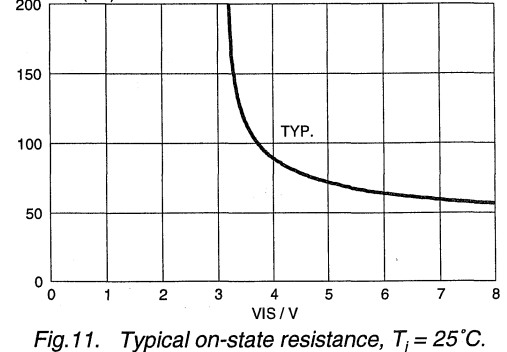


Fig.11. Typical on-state resistance, $T_j = 25^\circ C$.
$R_{DS(ON)} = f(V_{IS})$; $t_p = 250\ \mu s$; parameter V_{IS}

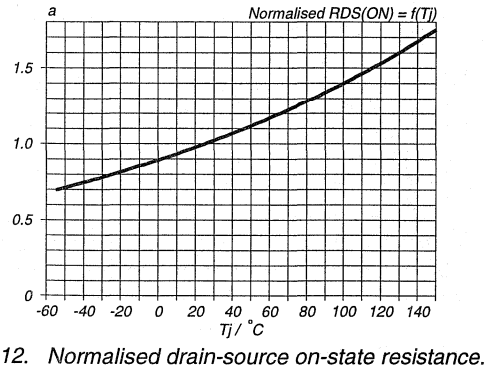


Fig.12. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25°C = f(T_j)$; I_D = 6 A; $V_{IS} \geq 4.4$ V

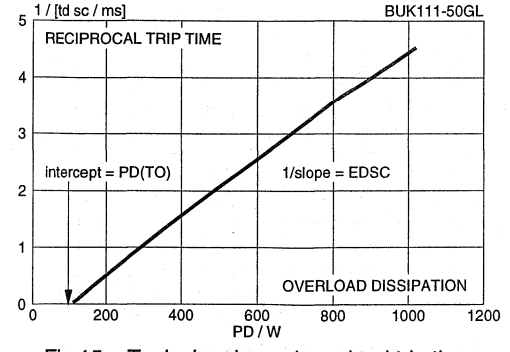


Fig.15. Typical reciprocal overload trip time. $1/t_{d\,sc} = f(P_D)$; conditions: V_{PS} = 5 V, T_{mb} = 25°C

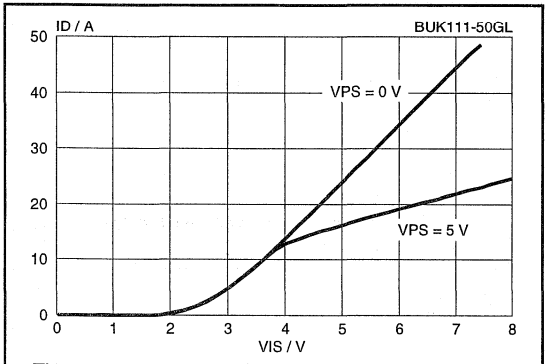


Fig.13. Typical transfer characteristics, T_j = 25°C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

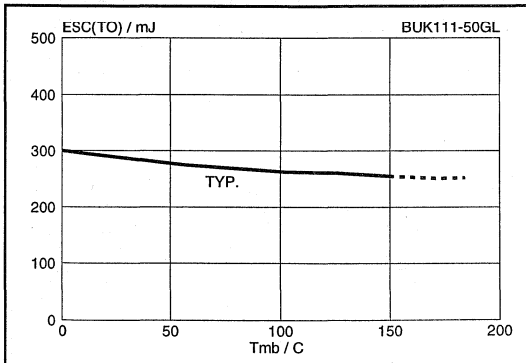


Fig.16. Typical overload protection energy. $E_{SC(TO)} = f(T_{mb})$; V_{DD} = 13 V; V_{PS} = 5 V, V_{IS} = 5 V

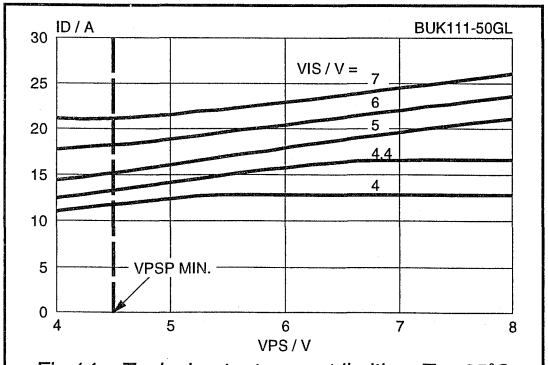


Fig.14. Typical output current limiting, T_j = 25°C. $I_D = f(V_{PS})$; t_p = 250 µs; V_{DS} = 10 V; parameter V_{IS}

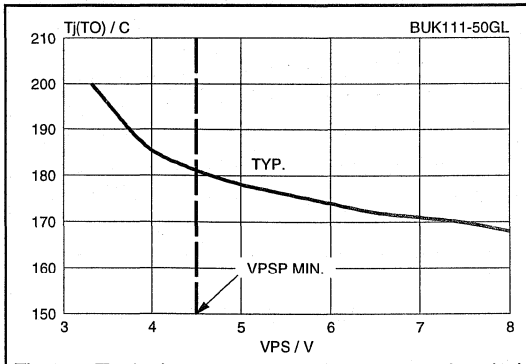


Fig.17. Typical overtemperature protection threshold. $T_{j(TO)} = f(V_{PS})$; V_{IS} = 5 V; $I_D \geq 1$ A

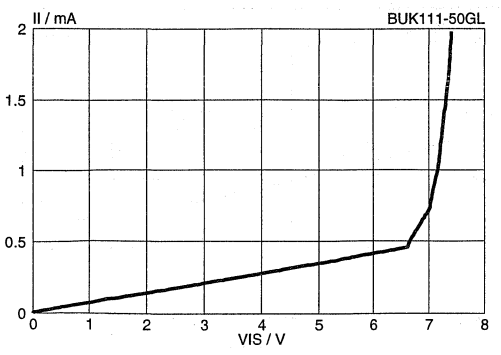


Fig.18. Typical DC input characteristic. $I_I = f(V_{IS})$ normal operation; $T_j = 25^\circ C$

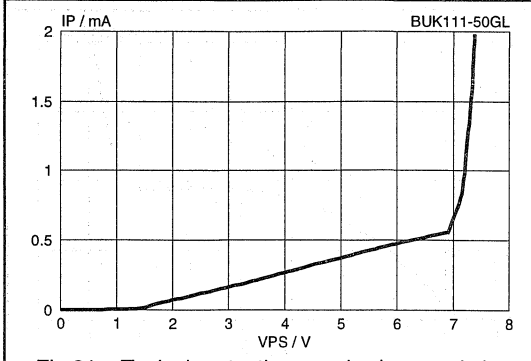


Fig.21. Typical protection supply characteristics. $I_P = f(V_{PS})$; normal or overload operation; $T_j = 25^\circ C$

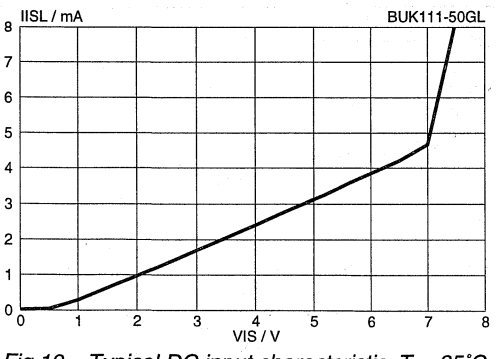


Fig.19. Typical DC input characteristic, $T_j = 25^\circ C$. $I_{ISL} = f(V_{IS})$ overload protection latched; $V_{PS} = 5$ V

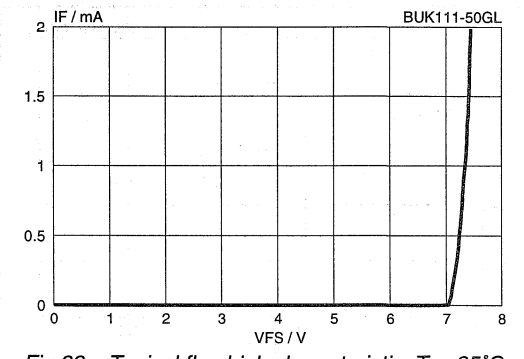


Fig.22. Typical flag high characteristic, $T_j = 25^\circ C$. $I_F = f(V_{FS})$; refer to TRUTH TABLE

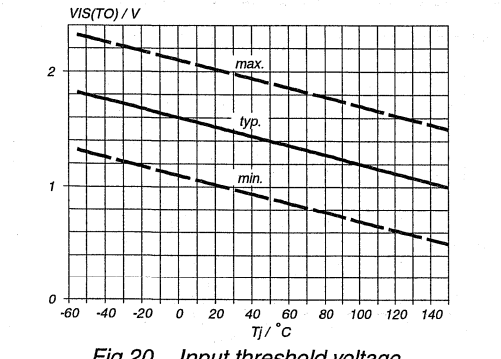


Fig.20. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

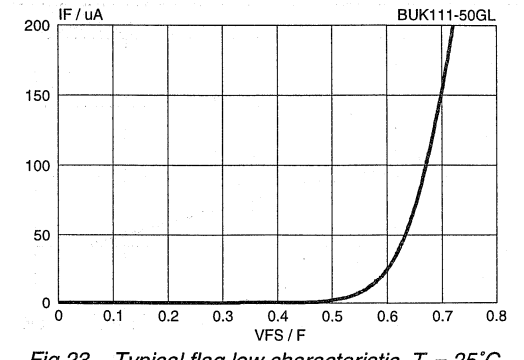


Fig.23. Typical flag low characteristic, $T_j = 25^\circ C$. $I_F = f(V_{FS})$; $V_{PS} = 5$ V; refer to TRUTH TABLE

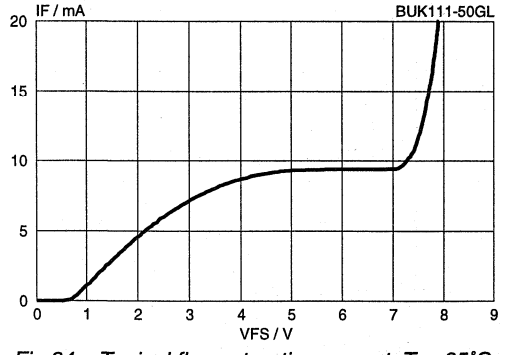


Fig.24. Typical flag saturation current, T_j = 25˚C. $I_F = f(V_{FS})$; flag 'low'; external R_F = 0 kΩ; V_{PS} = 5 V

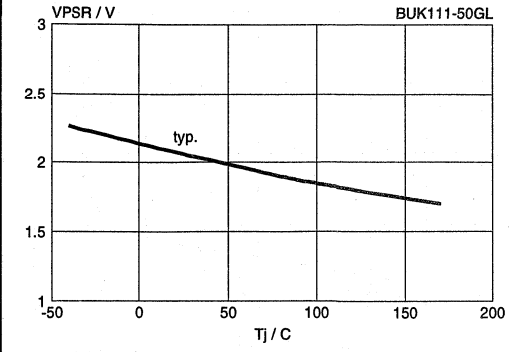


Fig.27. Protection supply reset voltage. $V_{PSR} = f(T_j)$

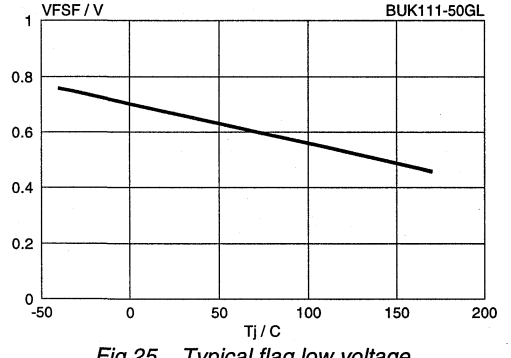


Fig.25. Typical flag low voltage. $V_{FSF} = f(T_j)$; V_{PS} = 5 V; V_{IS} = 5 V; V_{DS} = 0 V

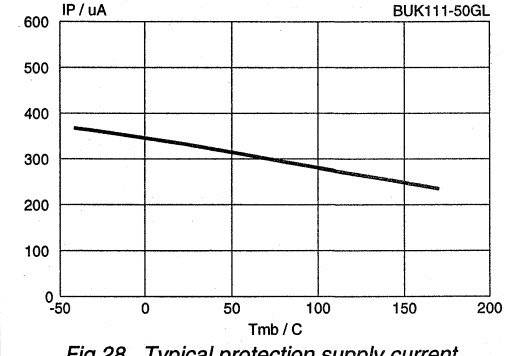


Fig.28. Typical protection supply current. $I_P = f(T_j)$; V_{PS} = 4.5 V

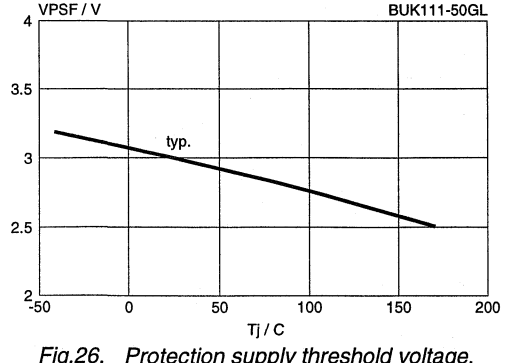


Fig.26. Protection supply threshold voltage. $V_{PSF} = f(T_j)$; condition: V_{DS} = 5 V

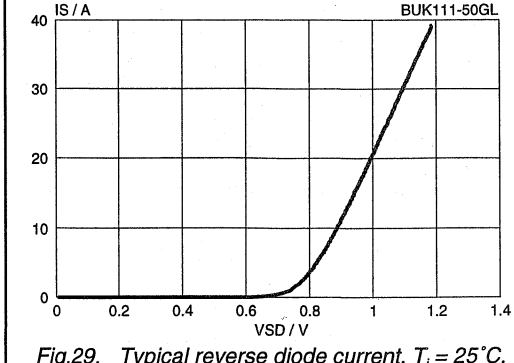


Fig.29. Typical reverse diode current, T_j = 25˚C. $I_S = f(V_{SD})$; conditions: V_{IS} = 0 V; t_p = 250 µs

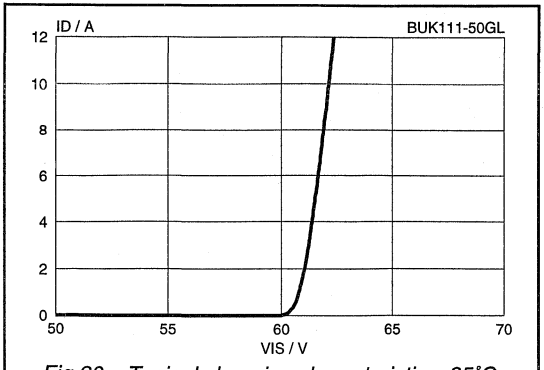


Fig.30. Typical clamping characteristics, 25˚C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

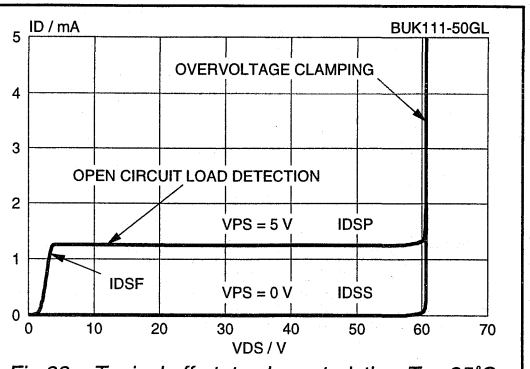


Fig.33. Typical off-state characteristics, $T_j = 25$˚C. $I_D = f(V_{DS})$; $V_{IS} = 0$ V; parameter V_{PS}

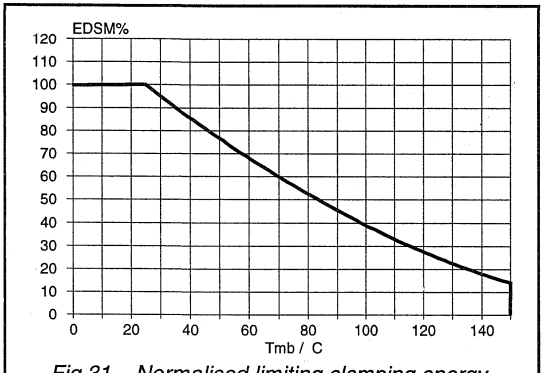


Fig.31. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: $I_D = 6$ A

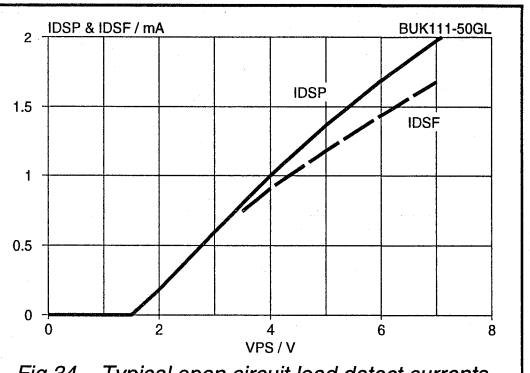


Fig.34. Typical open circuit load detect currents. I_{DSP} & $I_{DSF} = f(V_{PS})$; $V_{IS} = 0$ V; $V_{DS} \geq 5$ V; $T_j = 25$˚C

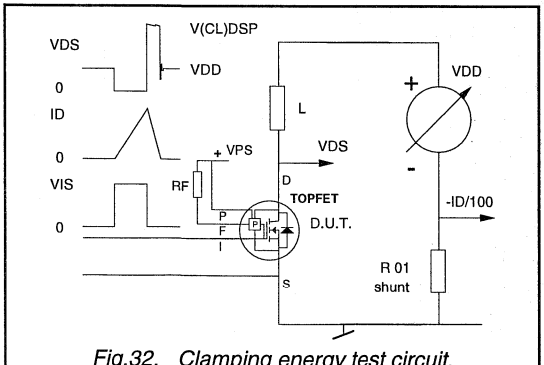


Fig.32. Clamping energy test circuit.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$$

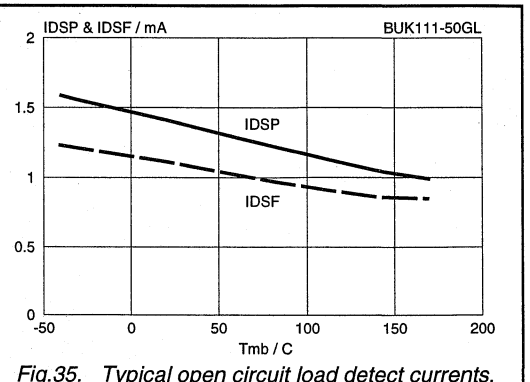


Fig.35. Typical open circuit load detect currents. I_{DSP} & $I_{DSF} = f(T_j)$; $V_{PS} = 5$ V; $V_{IS} = 0$ V

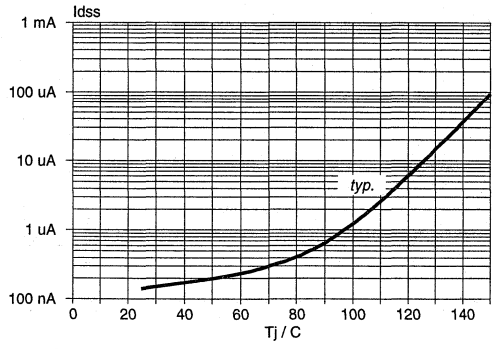


Fig.36. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: V_{DS} = 40 V; V_{IS} = 0 V.

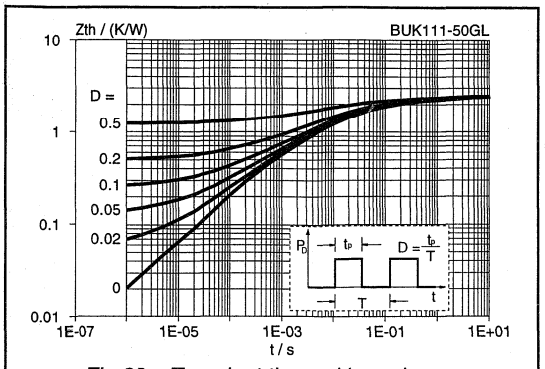


Fig.38. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

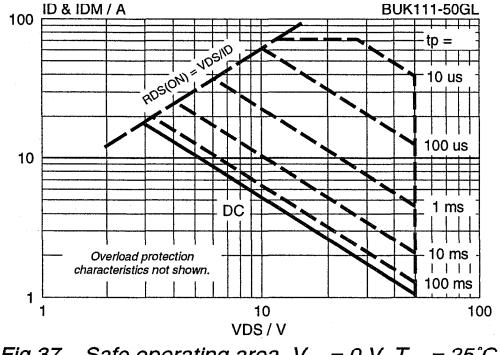


Fig.37. Safe operating area, V_{PS} = 0 V, T_{mb} = 25˚C. I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

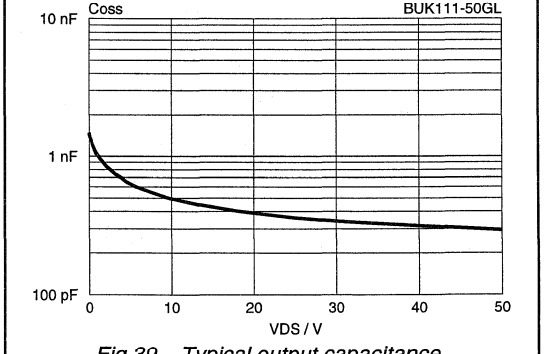


Fig.39. Typical output capacitance. $C_{oss} = f(V_{DS})$; conditions: V_{IS} = 0 V; f = 1 MHz

APPLICATION INFORMATION

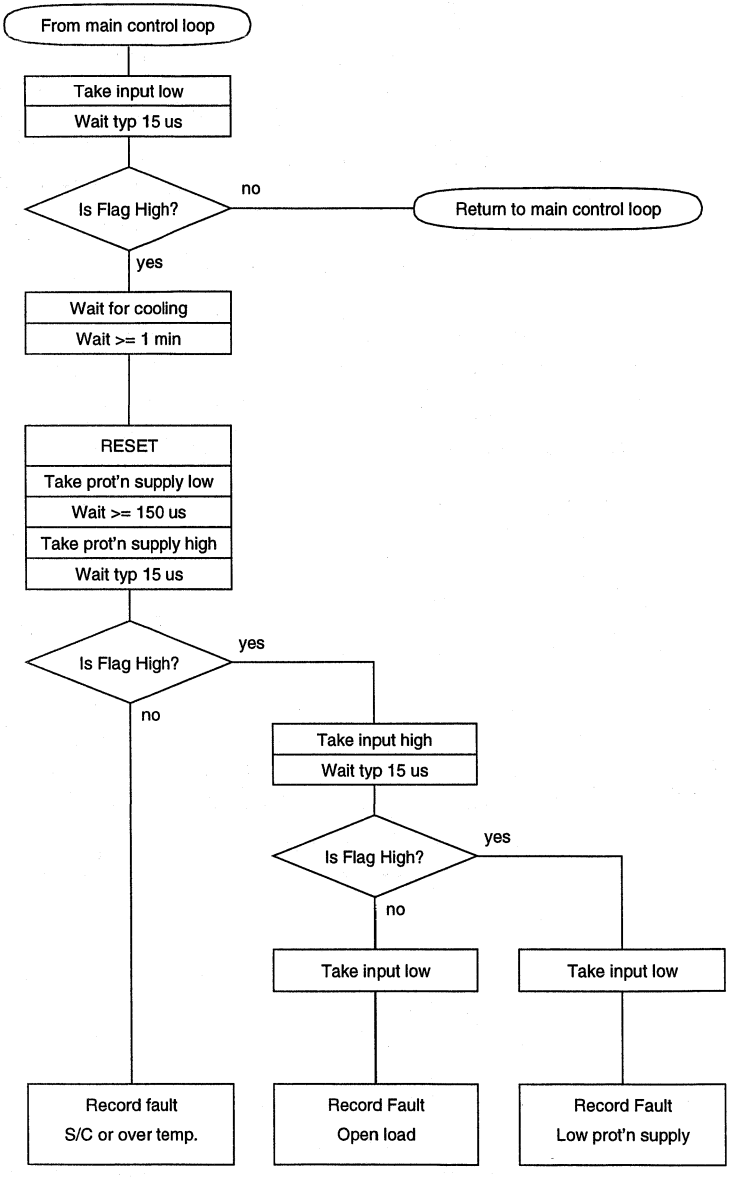


Fig. 40. Possible fault diagnosis procedure.

PowerMOS transistor Logic level TOPFET

BUK112-50GL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a low side switch for automotive applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	12	A
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	93	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PS}	Protection supply voltage	5	V

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Low operating supply current
- Overtemperature protection
- Overload protection against short circuit load with drain current limiting
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- Off-state detection of open circuit load indicated by flag pin
- 5 V logic compatible input level
- Integral input resistors.
- ESD protection on all pins
- Over voltage clamping

FUNCTIONAL BLOCK DIAGRAM

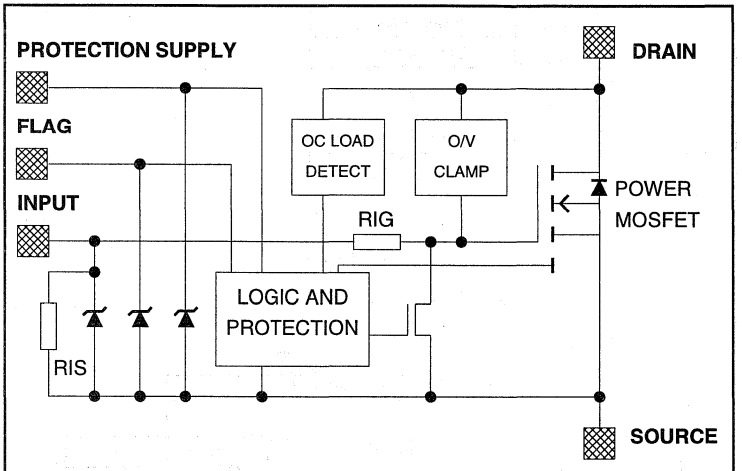


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION

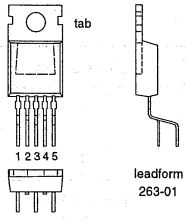


Fig. 2.

SYMBOL

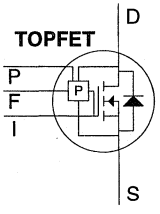


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Continuous voltage				
V_{DS}	Drain source voltage[1]	V_{IS} = 0 V	-	50	V
	Continuous currents				
I_D	Drain current	V_{PS} = 5 V; T_{mb} = 25 °C	-	self - limited	A
		V_{PS} = 0 V; T_{mb} = 94 °C	-	12	A
I_I	Input current	-	-5	5	mA
I_F	Flag current	-	-5	5	mA
I_P	Protection supply current	-	-5	5	mA
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	52	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	260	°C

ESD LIMITING VALUES

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Electrostatic discharge capacitor voltages	Human body model; C = 100 pF; R = 1.5 kΩ			
V_{C1}	Drain to source		-	4.5	kV
V_{C2}	Input, flag or protection to source		-	2	kV

OVERLOAD PROTECTION LIMITING VALUE

With the protection supply connected, TOPFET can protect itself from two types of overload - short circuit load and overtemperature.

For overload conditions an n-MOS transistor turns on between the gate and source to quickly discharge the power MOSFET gate capacitance.

The drain current is limited to reduce dissipation in case of short circuit load. Refer to OVERLOAD CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{PSP}	Protection supply voltage[3]	for valid protection	4.5	-	V

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	I_{DM} = 6 A; T_{mb} = 25°C	-	200	mJ
E_{DRM}	Repetitive clamping energy	I_{DM} = 3.1 A; $V_{DD} \leq$ 20 V; $T_{mb} \leq$ 120°C; f = 250 Hz	-	20	mJ

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	-	2.38	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	-	K/W

OUTPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{PS} = 0 V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Off-state					
$V_{(CL)DSS}$	Drain-source clamping voltage	I_D = 10 mA; -40°C ≤ T_{mb} ≤ 150°C	50	-	70	V
		I_{DM} = 0.75 A; t_p ≤ 300 µs; δ ≤ 0.01	50	60	70	V
I_{DSS}	Drain-source leakage current[1]	V_{IS} = 0 V; V_{DS} = 13 V	-	0.5	10	µA
		V_{DS} = 50 V	-	1	20	µA
		T_{mb} = 125 °C; V_{DS} = 40 V	-	10	100	µA
	On-state	t_p ≤ 300 µs; δ ≤ 0.01				
$R_{DS(ON)}$	Drain-source on-resistance	I_{DM} = 6 A; V_{IS} = 4.4 V; V_{PS} = 4.5 V	-	70	93	mΩ
		T_{mb} = 150 °C	-	135	165	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Normal operation					
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 13 V; V_{PS} = 0 V; I_D = 1 mA	1	1.5	2	V
		-40°C ≤ T_{mb} ≤ 150°C	0.5	-	2.5	V
I_{IS}	Input current	V_{IS} = 5 V -40°C ≤ T_{mb} ≤ 150°C	200	350	500	µA
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA	6	7.1	-	V
R_{IG}	Internal series resistance	to gate of power MOSFET	-	1.5	-	kΩ
	Overload protection latched					
I_{ISL}	Input current	V_{PS} = 5 V; V_{IS} = 5 V	1.5	3.2	4	mA

REVERSE CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	Reverse drain voltage[2]	$-I_D$ = 6 A	-	0.8	-	V
$-V_{IS}$	Reverse input voltage	$-I_I$ = 5 mA	-	0.7	-	V
$-V_{PS}$	Reverse protection pin voltage	$-I_P$ = 5 mA	-	0.7	-	V
$-V_{FS}$	Reverse flag voltage	$-I_F$ = 5 mA	-	0.7	-	V

1 The drain current required for open circuit load detection is switched off when there is no protection supply, in order to ensure a low off-state quiescent current. Refer to OPEN CIRCUIT LOAD DETECTION CHARACTERISTICS.

2 Protection functions are disabled during reverse conduction.

PROTECTION SUPPLY CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Normal operation or protection latched					
I_{PS}, I_{PSL}	Supply current	V_{PS} = 4.5 V	-	330	400	µA
		-40°C ≤ T_{mb} ≤ 150°C	-	-	450	µA
$V_{(CL)PS}$	Clamping voltage	I_P = 1.5 mA	6	7.1	-	V
	Overload protection latched					
V_{PSR}	Reset voltage		-	2.1	-	V
		-40°C ≤ T_{mb} ≤ 150°C	1.5	-	3	V
t_{pr}	Reset time	V_{PS} = 0 V	-	25	-	µs
		-40°C ≤ T_{mb} ≤ 150°C	-	-	150	µs

OPEN CIRCUIT LOAD DETECTION CHARACTERISTICS

An open circuit load condition can be detected while the TOPFET is in the off-state.
-40°C ≤ T_{mb} ≤ 150°C; V_{PS} = 5 V; V_{DS} = 13 V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DSP}	Off-state drain current[1]	V_{IS} = 0 V	0.5	1.4	2	mA
I_{DSF}	Off-state drain threshold current	V_{IS} = 0 V; I_F = 100 µA	0.4	1.1	-	mA
V_{ISF}	Input threshold voltage[2]	I_F = 100 µA; I_D = 100 µA; T_{mb} = 25 °C	-	1.2	-	V

TRUTH TABLE

For normal, open-circuit load and overload conditions or inadequate protection supply voltage.

CONDITION	PROTECTION	INPUT	FLAG	OUTPUT
Normal on-state	1	1	0	1
Normal off-state	1	0	0	0
Open circuit load	1	1	0	1
Open circuit load	1	0	1	0
Short circuit load	1	1	1	0
Over temperature	1	X	1	0
Low protection supply voltage	0	1	1	1
Low protection supply voltage	0	0	1	0

For protection '0' equals low, '1' equals high.
For input '0' equals low, '1' equals high, 'X' equals don't care.
For flag '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

1 The drain source current which flows when the protection supply is high and the input is low.

2 For open circuit load indication, V_{IS} must be less than V_{ISF}.

OVERLOAD CHARACTERISTICS

T_{mb} = 25 °C; V_{PS} = 5 V unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection	V_{IS} = 5 V				
I_D	Drain current limiting	V_{DS} = 13 V -40°C ≤ T_{mb} ≤ 150°C	12	24	36	A
$P_{D(TO)}$	Overload power threshold[1]	for protection to operate	-	100	-	W
E_{DSC}	Characteristic energy	which determines trip time[2]	-	200	-	mJ
I_{DM}	Peak drain current[3]	V_{DD} = 13 V; R_L ≤ 10 mΩ	-	45	-	A
	Overtemperature protection					
$T_{j(TO)}$	Threshold temperature	I_D ≥ 1 A	150	185	215	°C

FLAG CHARACTERISTICS

The flag is an open drain transistor which requires an external pull-up circuit.
T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation; V_{PS} = 5 V				
V_{FSF}	Flag voltage	I_F = 100 µA	-	0.7	-	V
		-40°C ≤ T_{mb} ≤ 150°C	-	-	0.9	V
I_{FSF}	Flag saturation current	V_{FS} = 5 V	-	10	-	mA
	Flag 'high'	overload or fault				
I_{FSO}	Flag leakage current	V_{FS} = 5 V	-	0.1	1	µA
		T_{mb} = 150°C	-	1	10	µA
$V_{(CL)FS}$	Flag clamping voltage	I_F = 100 µA	6	6.9	-	V
V_{PSF}	Protection supply threshold voltage[4]	I_F = 100 µA; V_{DS} = 5 V	2.5	3	4	V
		-40°C ≤ T_{mb} ≤ 150°C	2	-	4	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} = 5 V	-	50	-	kΩ

1 Refer to figure 15.

2 Trip time $t_{d\,sc} \approx E_{DSC} / [P_D - P_{D(TO)}]$. Refer also to figure 15.

3 For short circuit load connected after turn-on.

4 When V_{PS} is less than V_{PSF} the flag pin indicates low protection supply voltage. Refer to TRUTH TABLE.

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Resistive load	R_L = 4 Ω; I_D = 3 A				
$t_{d\,on}$	Turn-on delay time	V_{IS}: 0 V ⇒ 5 V	-	0.6	-	µs
t_r	Rise time		-	2.8	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS}: 5 V ⇒ 0 V	-	3.5	-	µs
t_f	Fall time		-	3.2	-	µs
	Inductive load	I_D = 3 A; V_{DD} = 13 V; with freewheel diode				
$t_{d\,on}$	Turn-on delay time	V_{IS}: 0 V ⇒ 5 V	-	0.9	-	µs
t_r	Rise time		-	1.2	-	µs
$t_{d\,off}$	Turn-off delay time	V_{IS}: 5 V ⇒ 0 V	-	6.7	-	µs
t_f	Fall time		-	0.6	-	µs

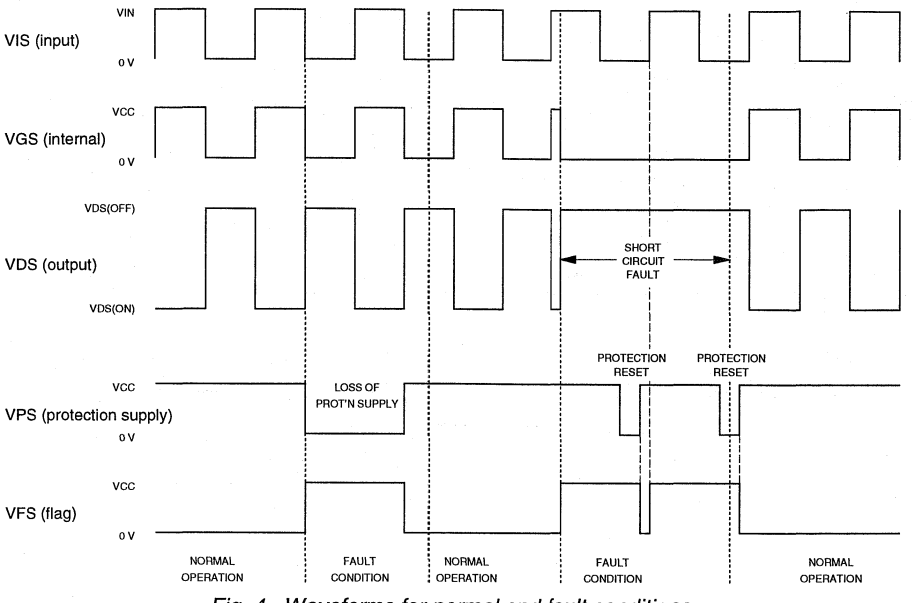


Fig. 4. Waveforms for normal and fault conditions.

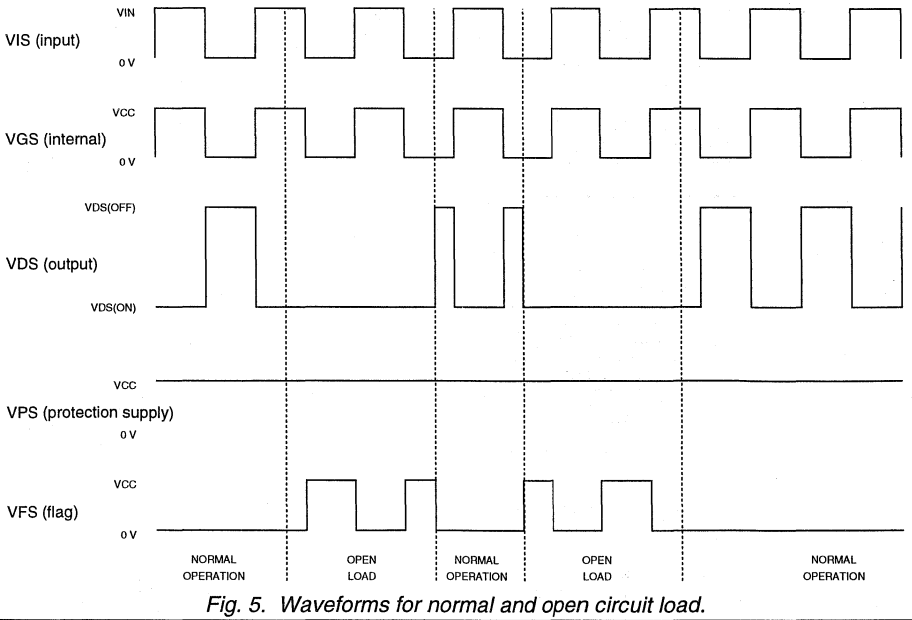


Fig. 5. Waveforms for normal and open circuit load.

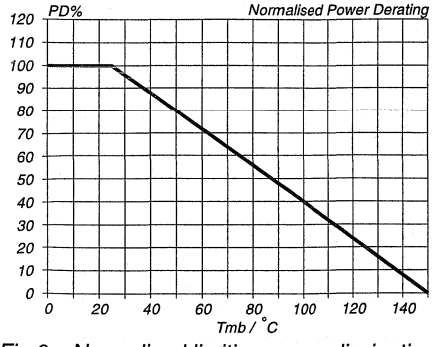


Fig.6. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25^\circ C) = f(T_{mb})$

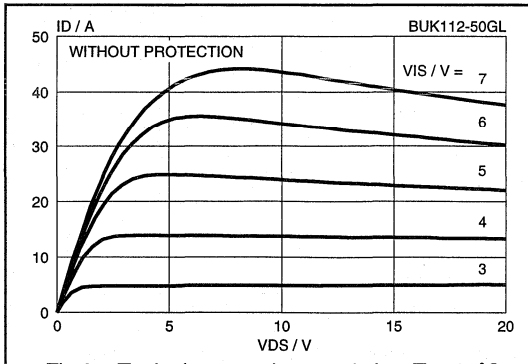


Fig.9. Typical output characteristics, $T_j = 25^\circ C$.
$I_D = f(V_{DS})$; $t_p = 250$ µs; $V_{PS} = 0$ V; parameter V_{IS}

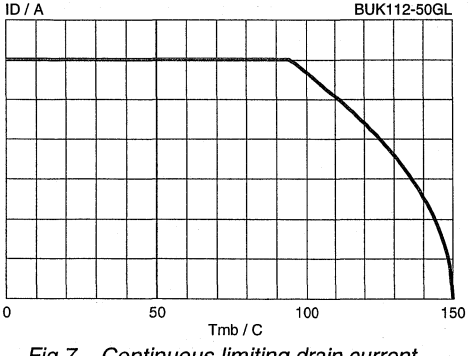


Fig.7. Continuous limiting drain current.
$I_D = f(T_{mb})$; conditions: $V_{IS} = 5$ V; $V_{PS} = 5$ V

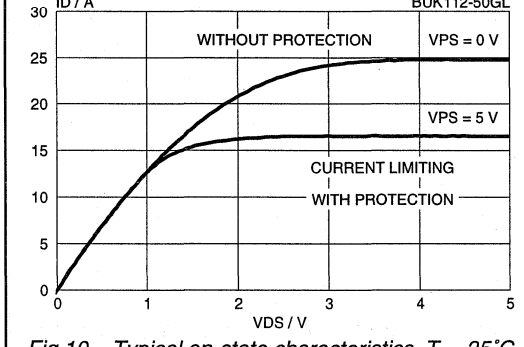


Fig.10. Typical on-state characteristics, $T_j = 25^\circ C$.
$I_D = f(V_{DS})$; $V_{IS} = 5$ V; $t_p = 250$ µs; parameter V_{PS}

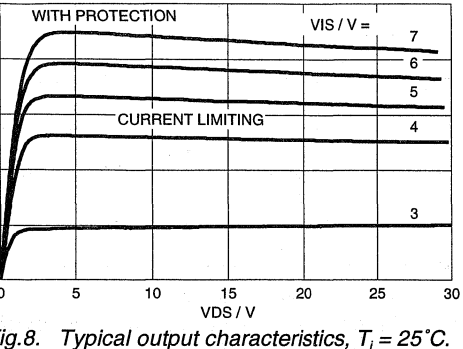


Fig.8. Typical output characteristics, $T_j = 25^\circ C$.
$I_D = f(V_{DS})$; $t_p = 250$ µs; $V_{PS} = 5$ V; parameter V_{IS}

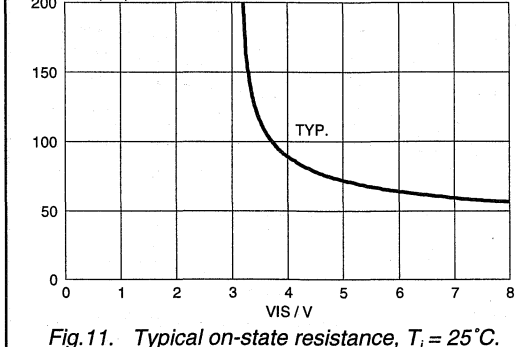


Fig.11. Typical on-state resistance, $T_j = 25^\circ C$.
$R_{DS(ON)} = f(V_{IS})$; $t_p = 250$ µs; parameter V_{IS}

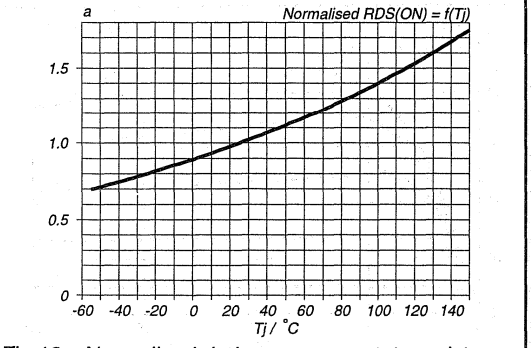


Fig.12. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25^{\circ}C = f(T_j)$; $I_D = 6$ A; $V_{IS} \geq 4.4$ V

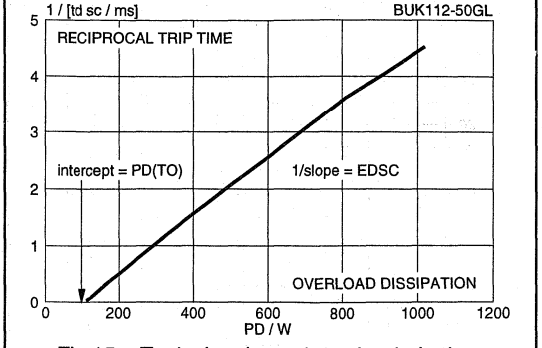


Fig.15. Typical reciprocal overload trip time. $1/t_{d\,sc} = f(P_D)$; conditions: $V_{PS} = 5$ V, $T_{mb} = 25^{\circ}C$

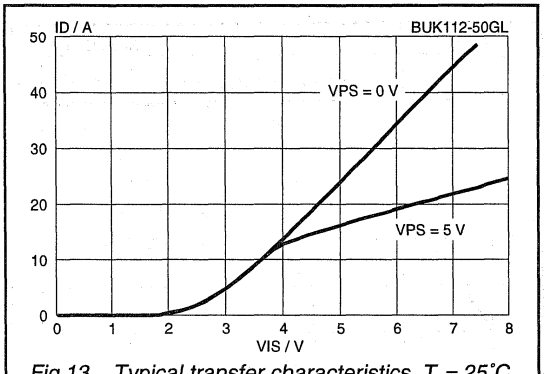


Fig.13. Typical transfer characteristics, $T_j = 25^{\circ}C$. $I_D = f(V_{IS})$; conditions: $V_{DS} = 10$ V; $t_p = 250$ µs

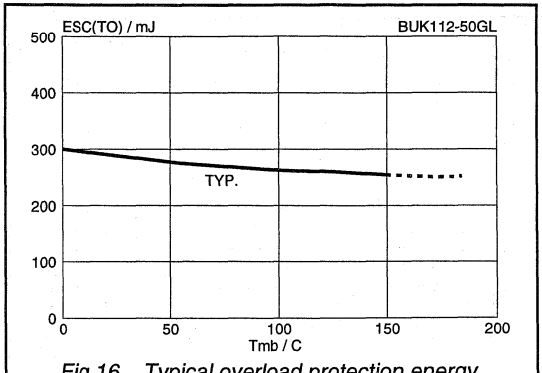


Fig.16. Typical overload protection energy. $E_{SC(TO)} = f(T_{mb})$; $V_{DD} = 13$ V; $V_{PS} = 5$ V, $V_{IS} = 5$ V

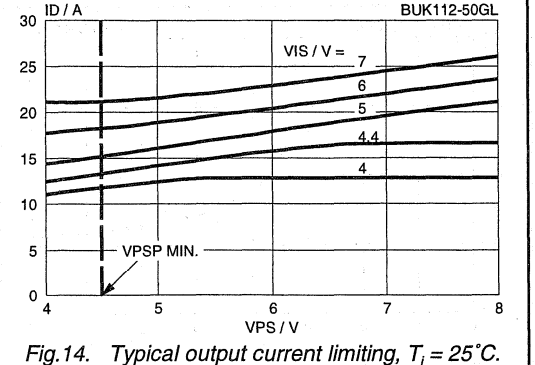


Fig.14. Typical output current limiting, $T_j = 25^{\circ}C$. $I_D = f(V_{PS})$; $t_p = 250$ µs; $V_{DS} = 10$ V; parameter V_{IS}

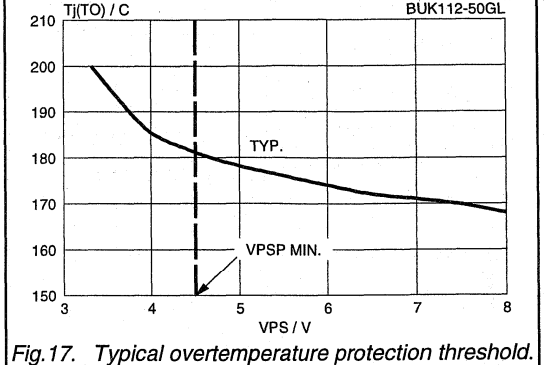


Fig.17. Typical overtemperature protection threshold. $T_{j(TO)} = f(V_{PS})$; $V_{IS} = 5$ V; $I_D \geq 1$ A

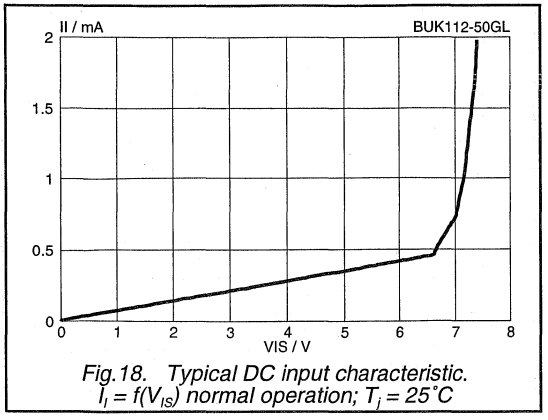


Fig.18. Typical DC input characteristic. $I_I = f(V_{IS})$ normal operation; $T_j = 25°C$

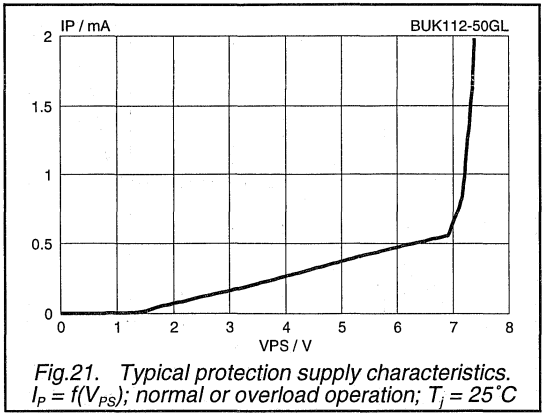


Fig.21. Typical protection supply characteristics. $I_P = f(V_{PS})$; normal or overload operation; $T_j = 25°C$

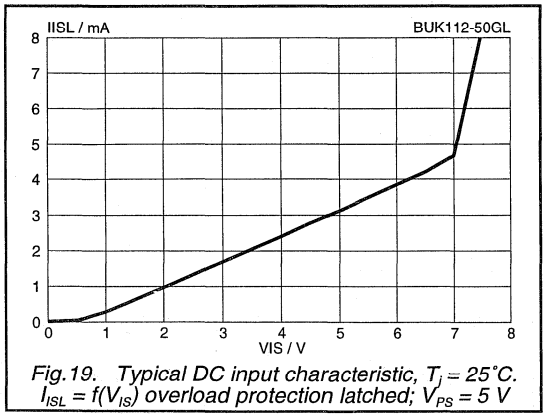


Fig.19. Typical DC input characteristic, $T_j = 25°C$. $I_{ISL} = f(V_{IS})$ overload protection latched; $V_{PS} = 5$ V

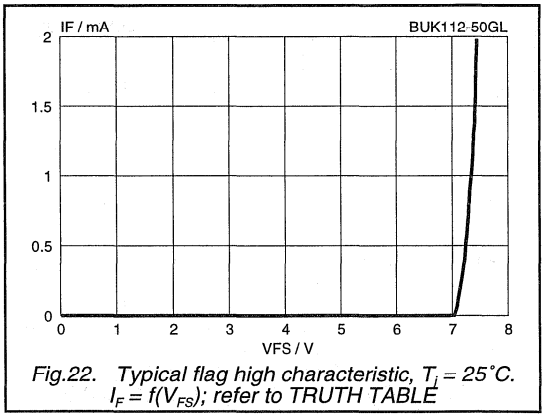


Fig.22. Typical flag high characteristic, $T_j = 25°C$. $I_F = f(V_{FS})$; refer to TRUTH TABLE

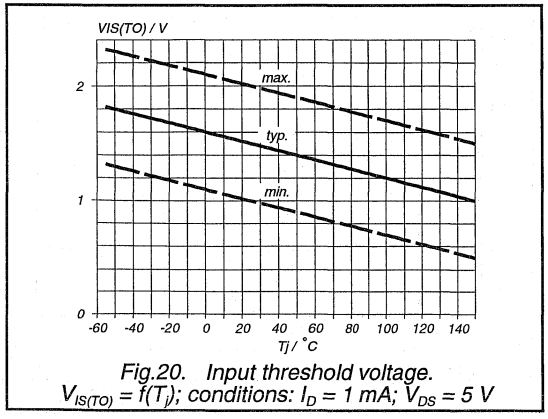


Fig.20. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = 5$ V

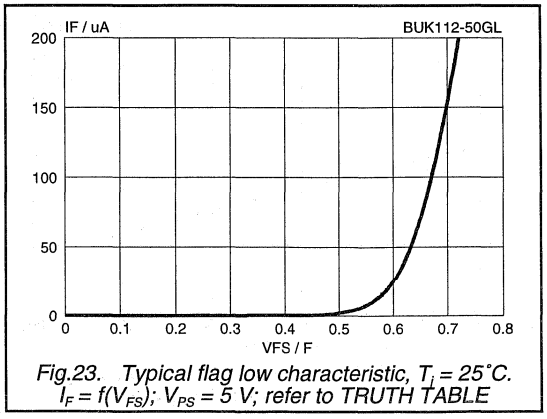


Fig.23. Typical flag low characteristic, $T_j = 25°C$. $I_F = f(V_{FS})$; $V_{PS} = 5$ V; refer to TRUTH TABLE

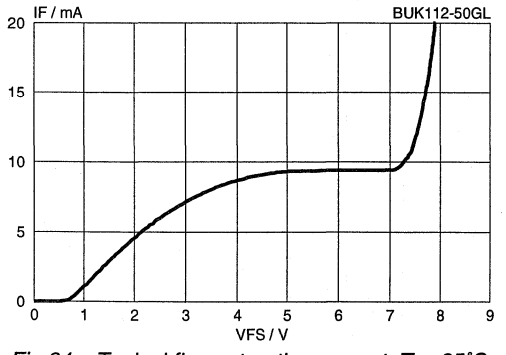


Fig.24. Typical flag saturation current, T_j = 25˚C. $I_F = f(V_{FS})$; flag 'low'; external R_F = 0 kΩ; V_{PS} = 5 V

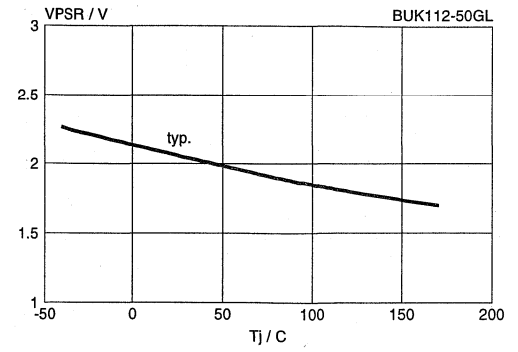


Fig.27. Protection supply reset voltage. $V_{PSR} = f(T_j)$

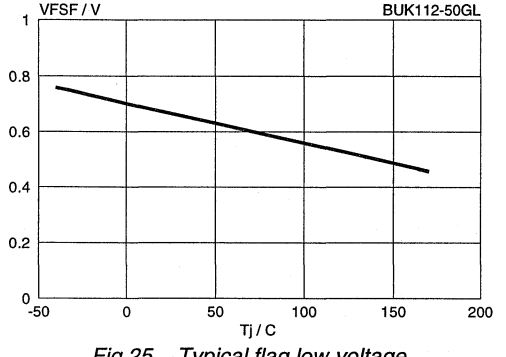


Fig.25. Typical flag low voltage. $V_{FSF} = f(T_j)$; V_{PS} = 5 V; V_{IS} = 5 V; V_{DS} = 0 V

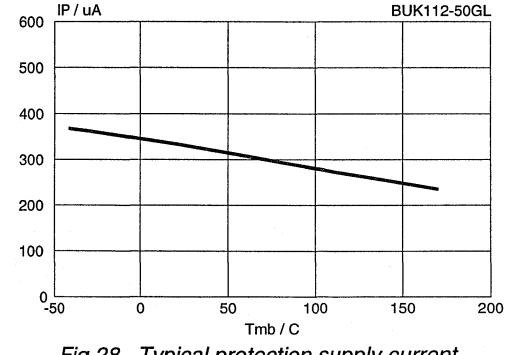


Fig.28. Typical protection supply current. $I_P = f(T_j)$; V_{PS} = 4.5 V

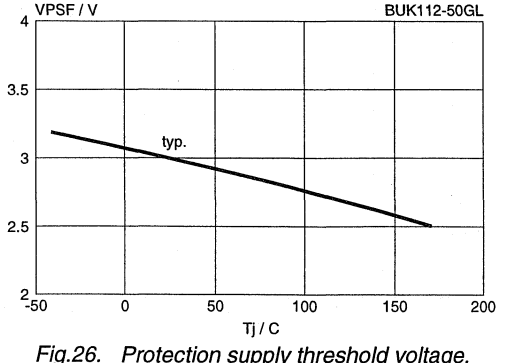


Fig.26. Protection supply threshold voltage. $V_{PSF} = f(T_j)$; condition: V_{DS} = 5 V

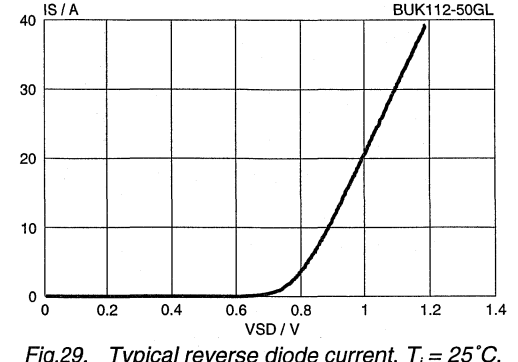


Fig.29. Typical reverse diode current, T_j = 25˚C. $I_S = f(V_{SD})$; conditions: V_{IS} = 0 V; t_p = 250 µs

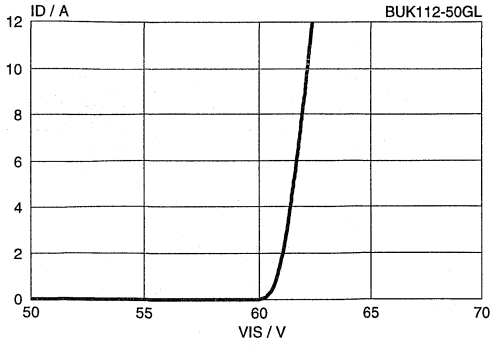


Fig.30. Typical clamping characteristics, 25˚C. $I_D = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $t_p \leq 50$ µs

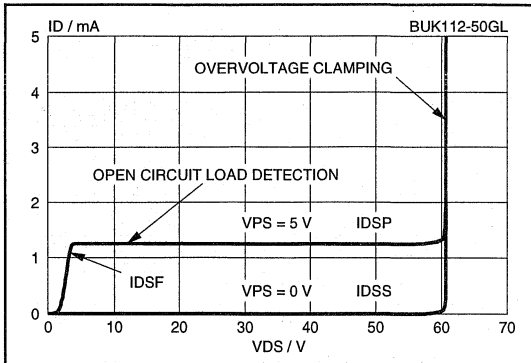


Fig.33. Typical off-state characteristics, $T_j = 25$˚C. $I_D = f(V_{DS})$; $V_{IS} = 0$ V; parameter V_{PS}

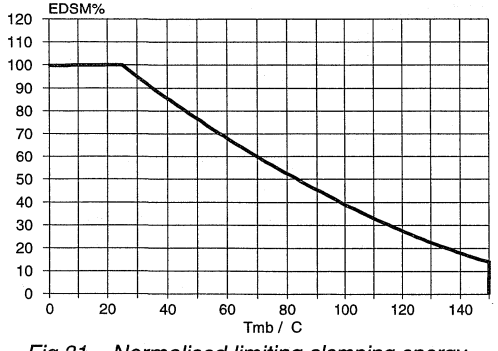


Fig.31. Normalised limiting clamping energy. $E_{DSM}\% = f(T_{mb})$; conditions: $I_D = 6$ A

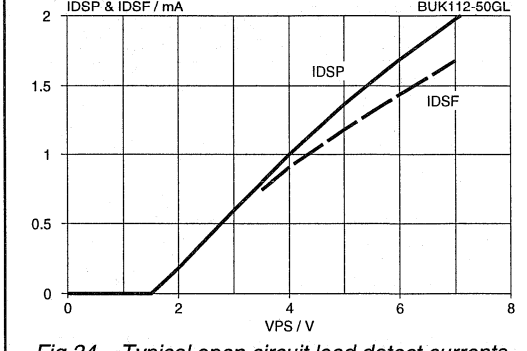


Fig.34. Typical open circuit load detect currents. I_{DSP} & $I_{DSF} = f(V_{PS})$; $V_{IS} = 0$ V; $V_{DS} \geq 5$ V; $T_j = 25$˚C

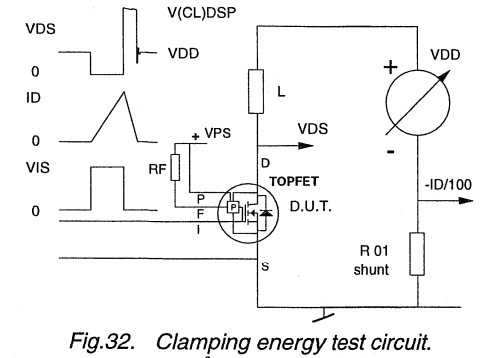


Fig.32. Clamping energy test circuit.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSS}/(V_{(CL)DSS} - V_{DD})$

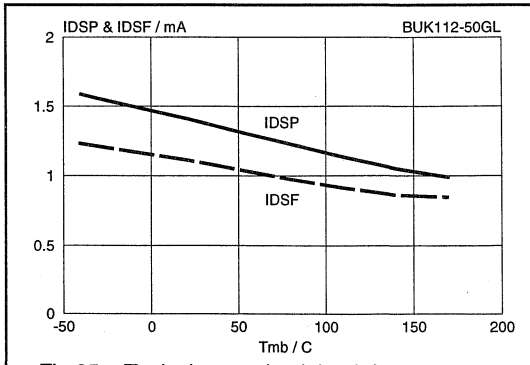


Fig.35. Typical open circuit load detect currents. I_{DSP} & $I_{DSF} = f(T_j)$; $V_{PS} = 5$ V; $V_{IS} = 0$ V

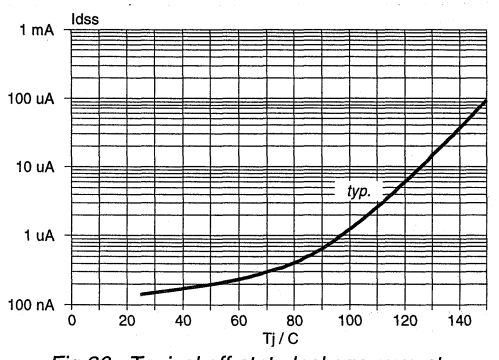


Fig.36. Typical off-state leakage current. $I_{DSS} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $V_{IS} = 0$ V.

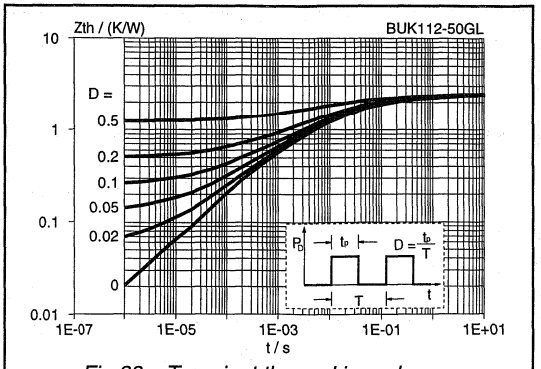


Fig.38. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

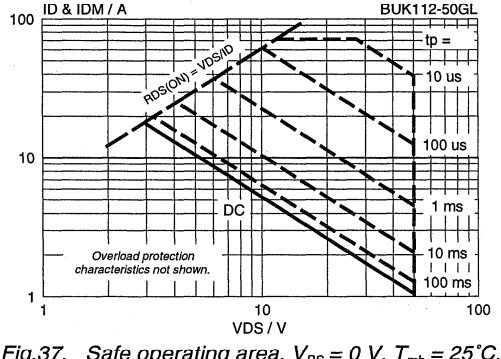


Fig.37. Safe operating area, $V_{PS} = 0$ V, $T_{mb} = 25$°C. I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

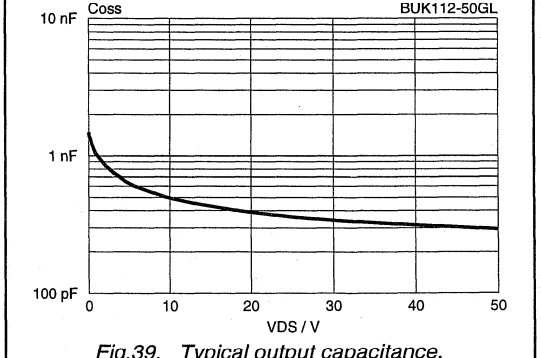


Fig.39. Typical output capacitance. $C_{oss} = f(V_{DS})$; conditions: $V_{IS} = 0$ V; f = 1 MHz

APPLICATION INFORMATION

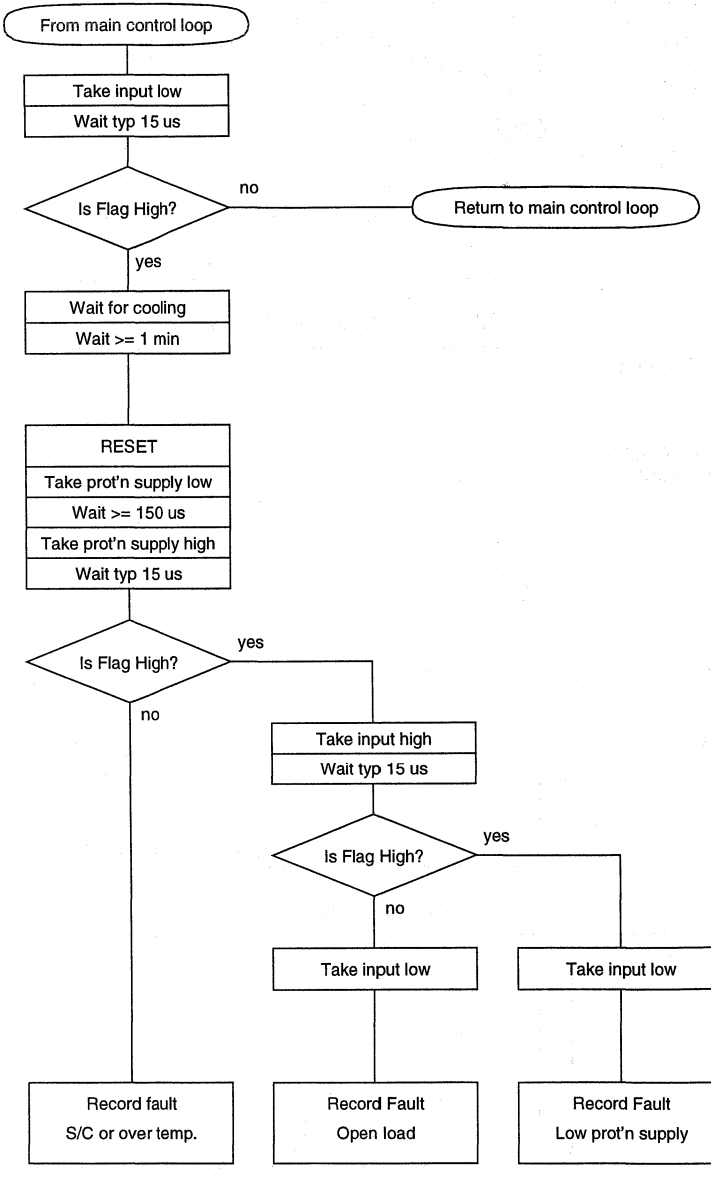


Fig. 40. Possible fault diagnosis procedure.

PowerMOS transistor Logic level TOPFET

BUK113-50DL

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 125°C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage	-	50	V
I_D	Drain current limiting	4	8	A
P_{tot}	Total power dissipation	-	4	W
T_j	Continuous junction temperature	-	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	-	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

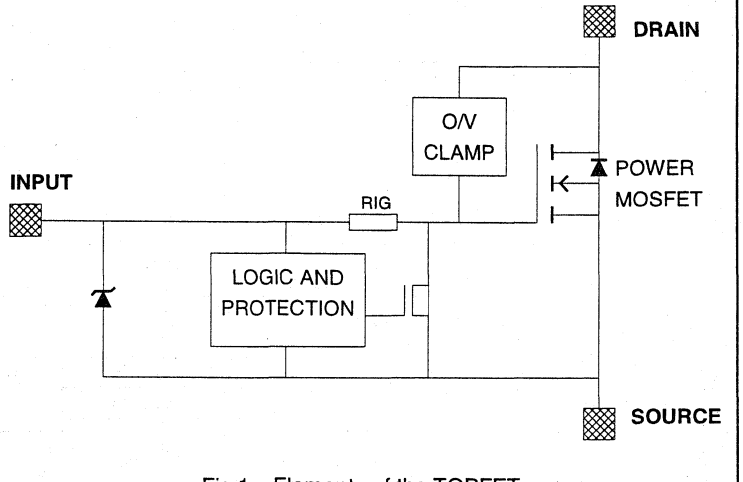
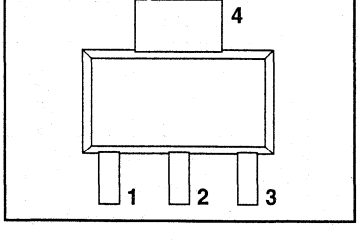


Fig.1. Elements of the TOPFET.

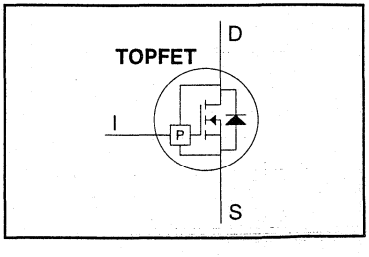
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current[2]	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{sp} = 90$ °C	-	4	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Continuous junction temperature	normal operation	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}sp}$	Junction to solder point	measured to pin 4 solder point	-	12	15	K/W
	Application information					
$R_{th\ j\text{-}a}$	Junction to ambient	on PCB of fig. 3	-	70	-	K/W
		on minimum footprint PCB	-	100	-	K/W

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 The input voltage for which the overload protection circuits are functional.

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	V_{IS} = 5 V	4	6	8	A
	Short circuit load protection					
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	*tbf*	-	J
	Overtemperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V	150	165	-	°C

STATIC CHARACTERISTICS

T_b = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 200 mA; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	V_{DS} = 45 V; V_{IS} = 0 V	-	0.5	2	µA
I_{DSS}	Off-state drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Off-state drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 100 °C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 1 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	150	200	mΩ

INPUT CHARACTERISTICS

T_b = 25 °C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	-	330	450	µA
			V_{IS} = 4 V	-	170	270	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	500	650	µA
			V_{IS} = 3.5 V	-	250	400	µA
V_{ISR}	Protection latch reset voltage[2]			1	2.2	3.5	V
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET		-	33	-	kΩ

SHADED BOXES

Values shown within shaded boxes are estimated for the objective specification.
These will not be fixed until the evaluation of prototype samples.

1 Continuous input voltage. The specified pulse width is for the drain current.

2 The input voltage below which the overload protection circuits will be reset.

Logic level TOPFET
SMD version of BUK104-50L/S

BUK114-50L/S

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin surface mounting plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_{tot}	Total power dissipation	40	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	125	mΩ
	V_{IS} = 7 V	100	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK114-50L	5	V
	BUK114-50S	10	V

FUNCTIONAL BLOCK DIAGRAM

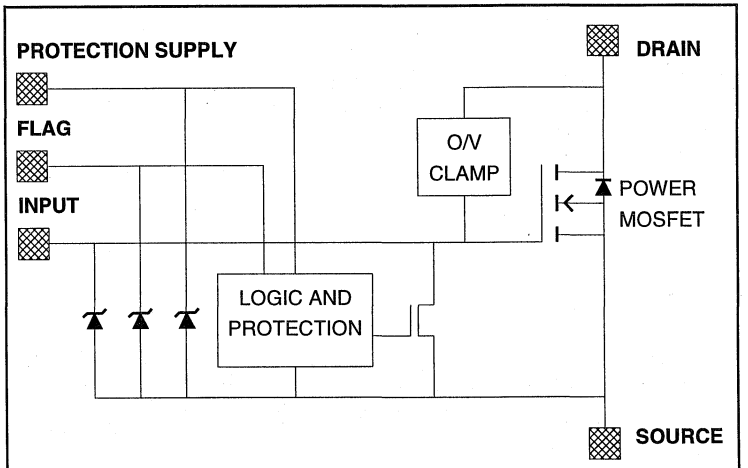


Fig.1. Elements of the TOPFET.

PINNING - SOT426

PIN	DESCRIPTION
1	input
2	flag
3	(connected to mb)
4	protection supply
5	source
mb	drain

PIN CONFIGURATION

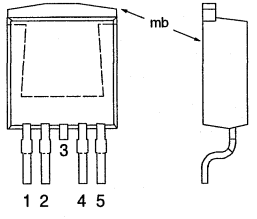


Fig. 2.

SYMBOL

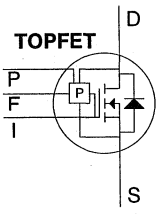


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Voltages				
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
V_{FS}	Continuous flag voltage	-	0	11	V
V_{PS}	Continuous supply voltage	-	0	11	V
	Currents	V_{IS} =	-	7 / 5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	15 / 13	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	9.5 / 8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	60 / 54	A
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		V_{IS} =	7 / 5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection			
		BUK114-50L	4.4 / 4	-	V
		BUK114-50S	5.4 / 5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$			
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH			
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	25	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	45	V
P_{DSM}	Instantaneous overload dissipation		-	0.8	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	15	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 15$ A; $R_{IS} \geq 100\ \Omega$	-	200	mJ
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 95$ °C; $I_{DM} = 4$ A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	15	A

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2.5	3.1	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300$ µs; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 7.5$ A; $t_p \leq 300$ µs; $\delta \leq 0.01$	$V_{IS} = 7$ V	-	75	100	mΩ
			$V_{IS} = 5$ V	-	95	125	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH; $R_I \geq 2$ kΩ				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	150	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	375	-	µs
	Over temperature protection	$V_{PS} = V_{PSN}$; $R_I \geq 2$ kΩ				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 0.65$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10$ V; $I_{DM} = 7.5$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	5	9	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	25	-	A
		$V_{IS} = 10$ V		40	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK114-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK114-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 15$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	8	-	ns
t_r	Rise time		-	13	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	100	-	ns
t_f	Fall time		-	45	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	415	600	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	275	400	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	55	80	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.
The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK114-50L	2.5	3.3	4	V
		BUK114-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

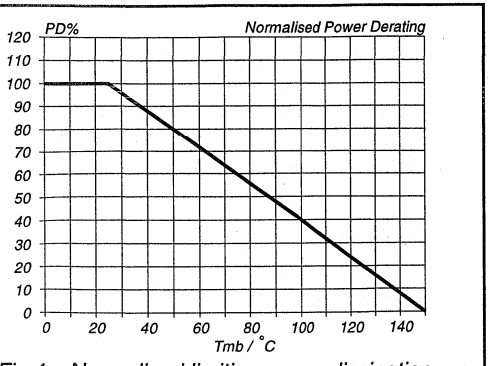


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

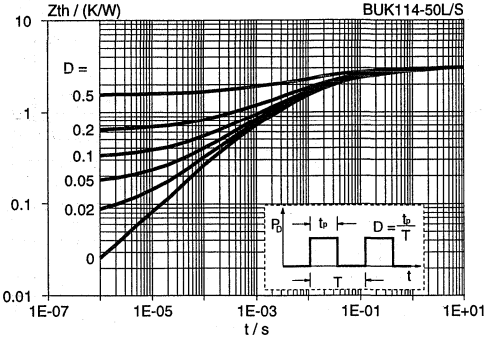


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

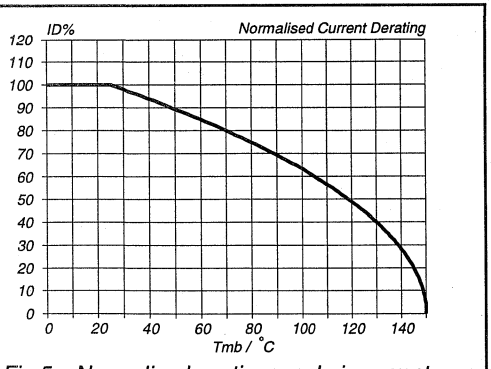


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

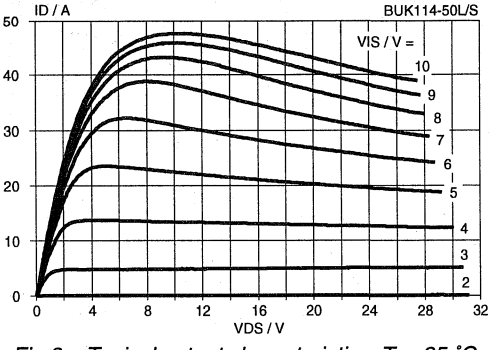


Fig.8. Typical output characteristics, $T_j = 25$ °C.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

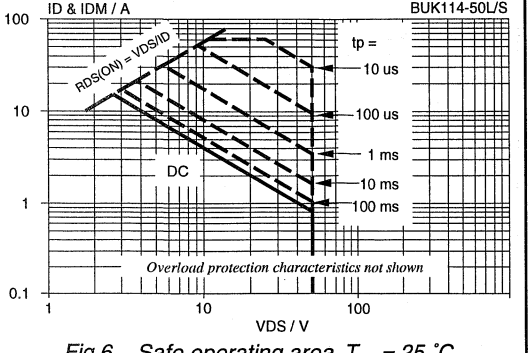


Fig.6. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

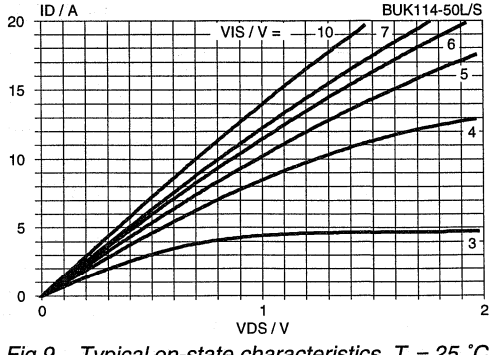


Fig.9. Typical on-state characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

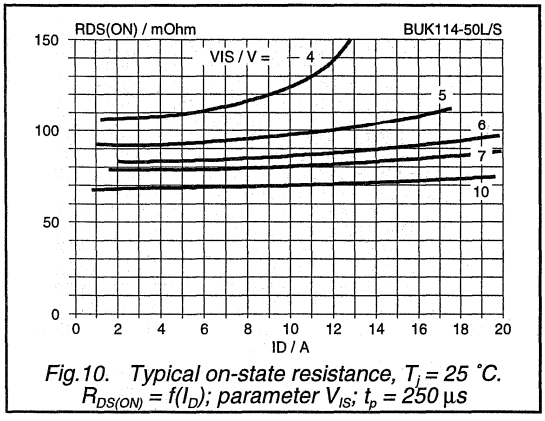


Fig.10. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

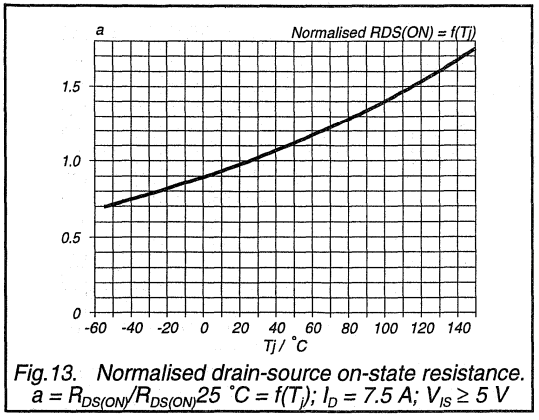


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 7.5 A; $V_{IS} \geq 5$ V

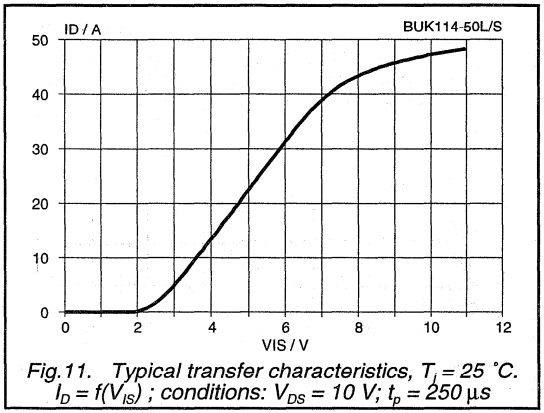


Fig.11. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

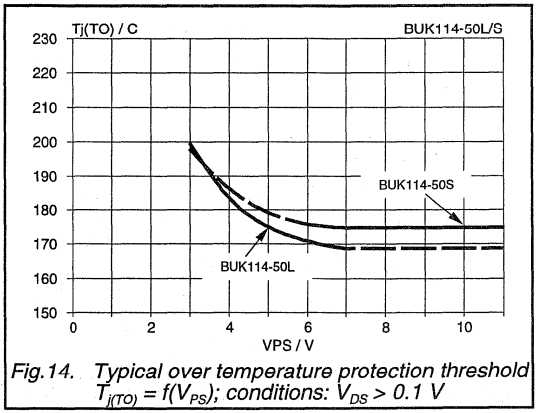


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

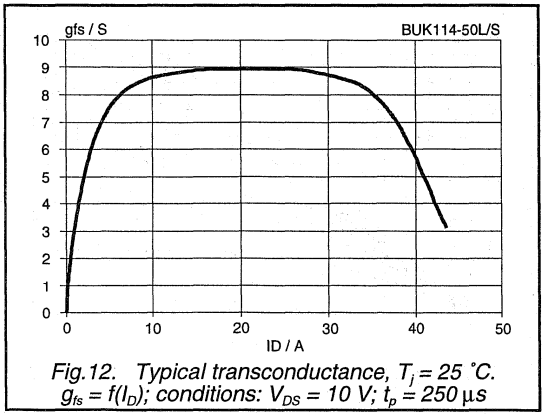


Fig.12. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

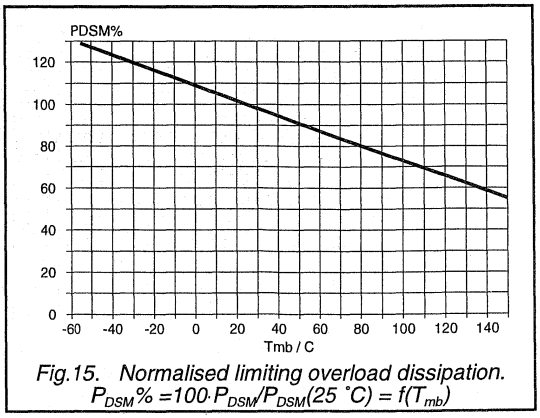


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

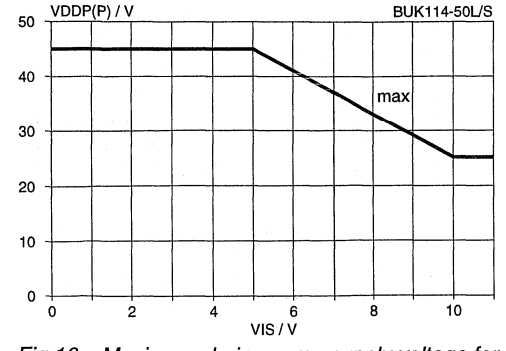


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ °C

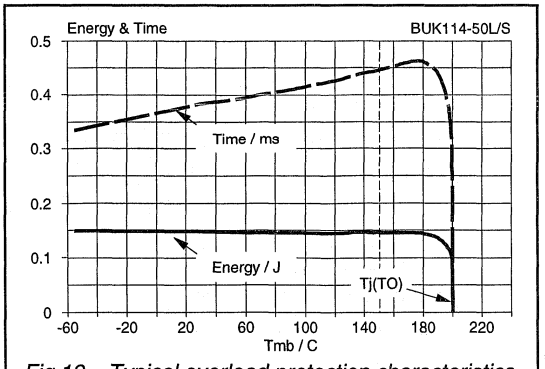


Fig.19. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; $V_{PS} = V_{PSN}$, V_{IS} = 7 V; SC load

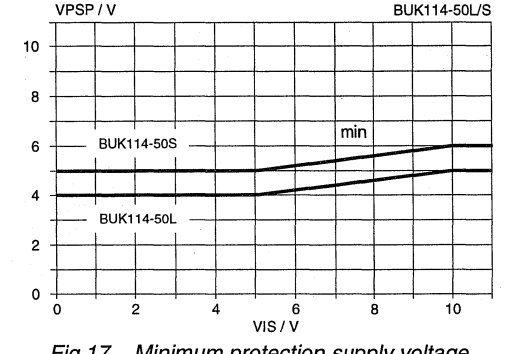


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ °C

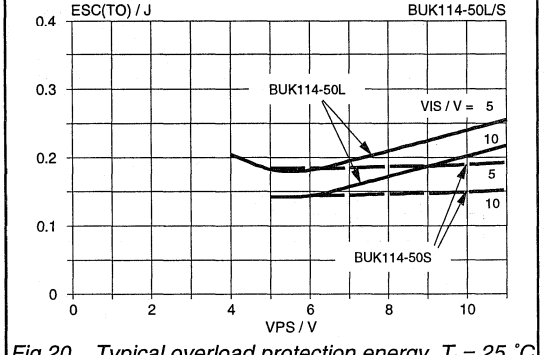


Fig.20. Typical overload protection energy, T_j = 25 °C $E_{SC(TO)} = f(V_{PS})$; conditions: V_{DS} = 13 V, parameter V_{IS}

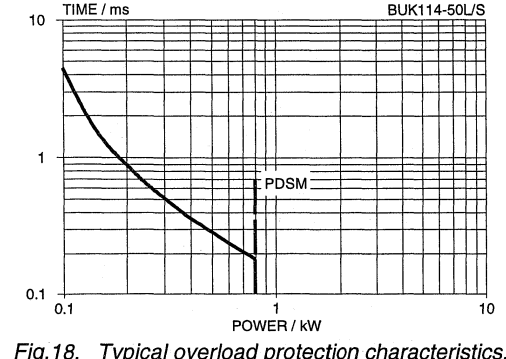


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

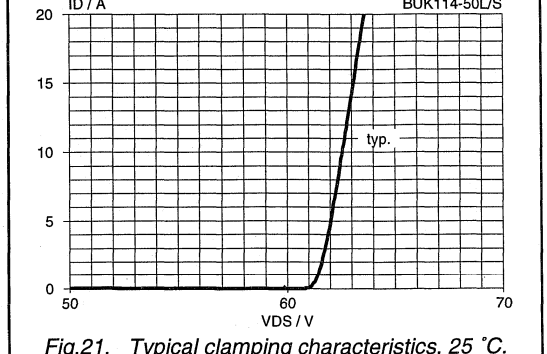


Fig.21. Typical clamping characteristics, 25 °C. $I_D = f(V_{DS})$; conditions: R_{IS} = 100 Ω; $t_p \leq 50$ µs

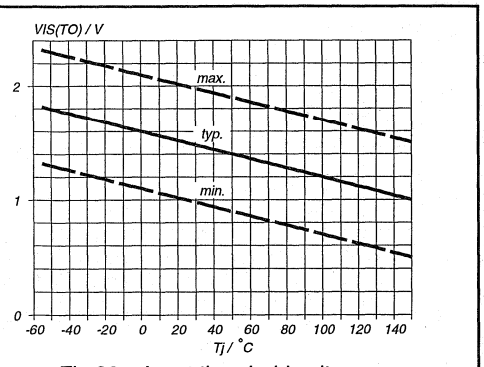


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

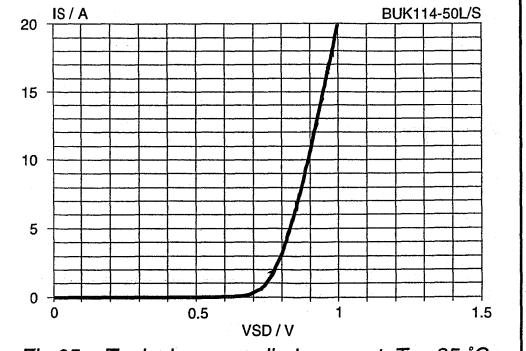


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

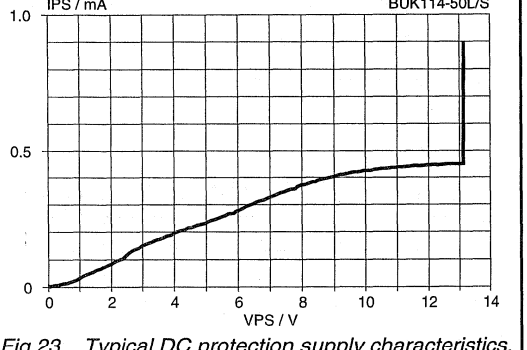


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

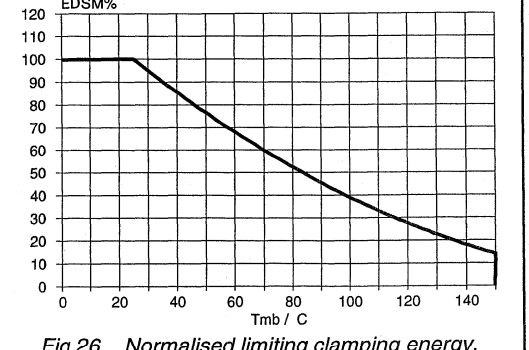


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A

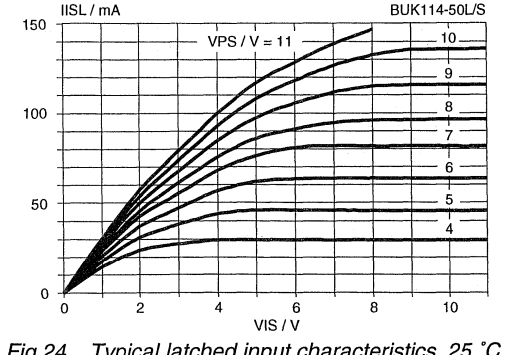


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

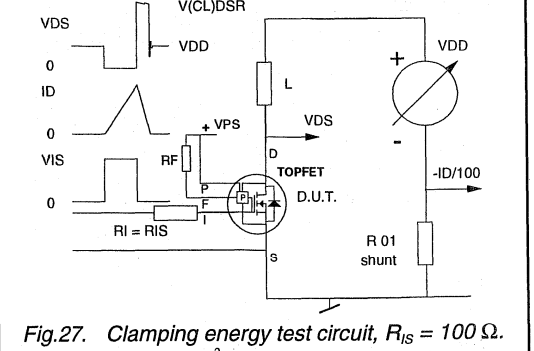


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$

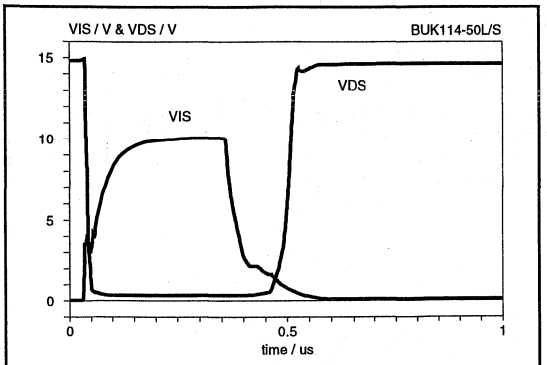


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

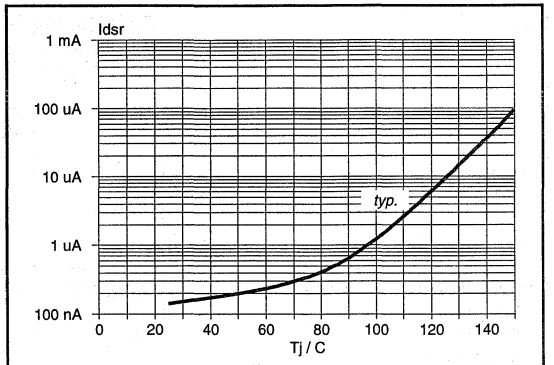


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

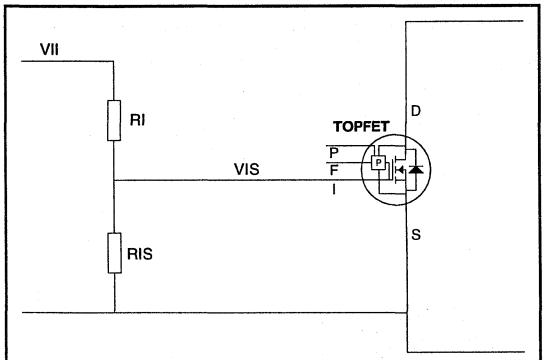


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

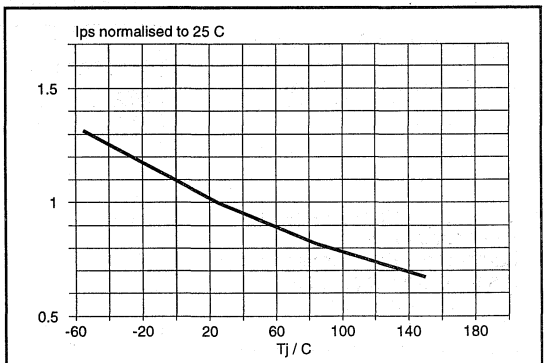


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25\ ^\circ C = f(T_j)$; $V_{PS} = V_{PSN}$

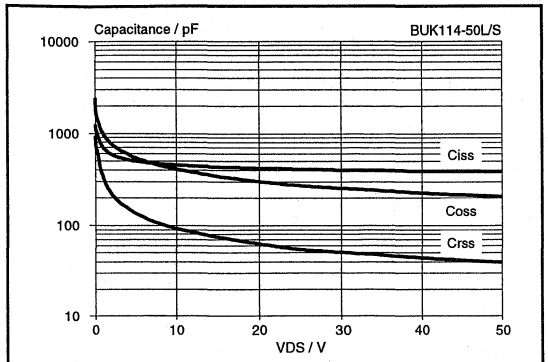


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

Logic level TOPFET
SMD version of BUK106-50L/S

BUK116-50L/S

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin surface mounting plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_{tot}	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	35	mΩ
	V_{IS} = 8 V	28	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK116-50L	5	V
	BUK116-50S	10	V

FUNCTIONAL BLOCK DIAGRAM

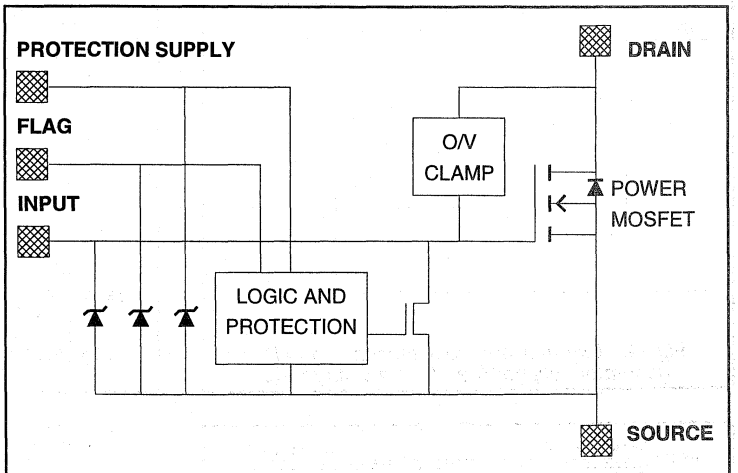


Fig.1. Elements of the TOPFET.

PINNING - SOT426

PIN	DESCRIPTION
1	input
2	flag
3	(connected to mb)
4	protection supply
5	source
mb	drain

PIN CONFIGURATION

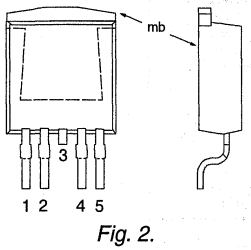


Fig. 2.

SYMBOL

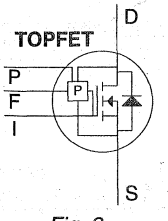


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Voltages				
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
V_{FS}	Continuous flag voltage	-	0	11	V
V_{PS}	Continuous supply voltage	-	0	11	V
	Currents	V_{IS} =	-	8 / 5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ °C	-	50 / 45	A
I_D	Continuous drain current	$T_{mb} \leq 100$ °C	-	31 / 28	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ °C	-	200 / 180	A
	Thermal				
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature[2]	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		V_{IS} =	8 / 5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection			
		BUK116-50L	4.4 / 4	-	V
		BUK116-50S	5.4 / 5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$			
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; L ≤ 10 µH			
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-	24	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-	45	V
P_{DSM}	Instantaneous overload dissipation		-	4	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	50	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	$I_{DM} = 27$ A; $R_{IS} \geq 100\ \Omega$	-	1	J
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 85$ °C; $I_{DM} = 16$ A; $V_{DD} \leq 20$ V; $f = 250$ Hz	-	80	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25$ °C; $V_{IS} = V_{PS} = V_{FS} = 0$ V	-	50	A

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1.0	K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_D = 10$ mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; $I_{DM} = 1$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12$ V; $V_{IS} = 0$ V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 50$ V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	$V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$; $T_j = 125$ °C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 25$ A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$	$V_{IS} = 8$ V	-	22	28	mΩ
			$V_{IS} = 5$ V	-	28	35	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; $T_{mb} = 25$ °C; $L \leq 10$ µH				
$E_{DS(TO)}$	Overload threshold energy	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	550	-	mJ
$t_{d\,sc}$	Response time	$V_{DD} = 13$ V; $V_{IS} = 10$ V	-	0.4	-	ms
	Over temperature protection	$V_{PS} = V_{PSN}$				
$T_{j(TO)}$	Threshold junction temperature	from $I_D \geq 2.5$ A[3]	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 12$ V; $I_{DM} = 25$ A $t_p \leq 300$ µs; $\delta \leq 0.01$	17	28	-	S
I_D	Drain current[4]	$V_{DS} = 13$ V; $V_{IS} = 5$ V	-	80	-	A
		$V_{IS} = 10$ V		160	-	A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK116-50L $V_{PS} = 5$ V	-	0.2	0.35	mA
		BUK116-50S $V_{PS} = 10$ V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		$T_j = 150$ °C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	$I_P = 1.35$ mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 20$ A; $V_{IS} = V_{PS} = V_{FS} = 0$ V; $t_p = 300$ µs	-	0.9	1.2	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
	Normal operation						
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.0	1.5	2.0	V
			T_{mb} = 150 °C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V		-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA		11	13	-	V
	Overload protection latched						
R_{ISL}	Input resistance[1]	V_{PS} = 5 V	I_I = 5 mA;	-	55	-	Ω
			T_{mb} = 150 °C	-	95	-	Ω
		V_{PS} = 10 V	I_I = 5 mA;	-	35	-	Ω
			T_{mb} = 150 °C	-	60	-	Ω
	Application information						
	External input resistances for	(see figure 29)					
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω;	V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω;	V_{II} = 5 V	1	-	-	kΩ
			V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\,on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	10	-	ns
t_r	Rise time		-	35	-	ns
$t_{d\,off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	280	-	ns
t_f	Fall time		-	120	-	ns

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	1250	1800	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	650	1000	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	150	250	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates. The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK116-50L	2.5	3.3	4	V
		BUK116-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

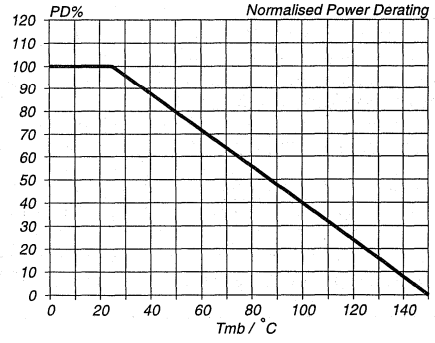


Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

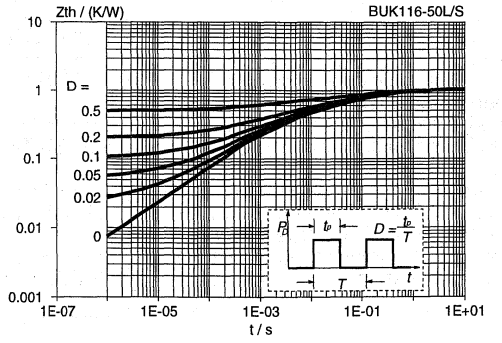


Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

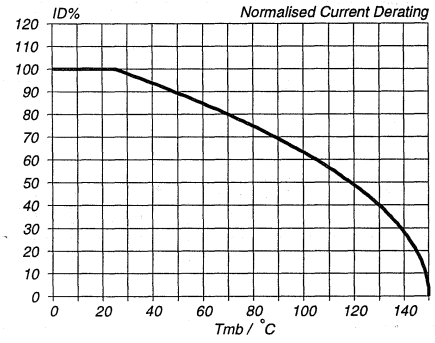


Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

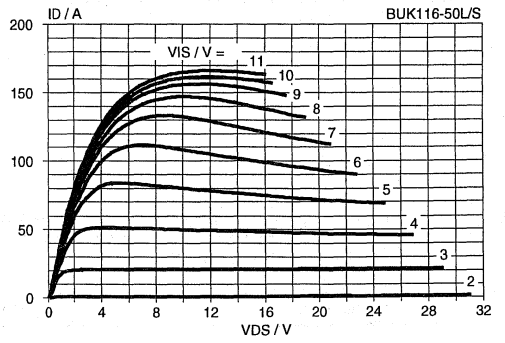


Fig.8. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\,sc}$

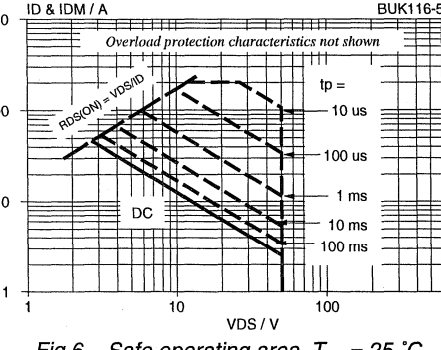


Fig.6. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

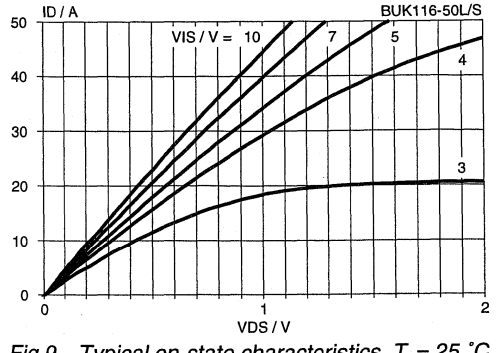


Fig.9. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

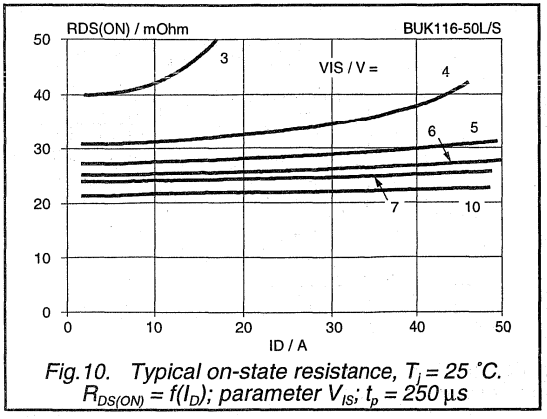


Fig.10. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

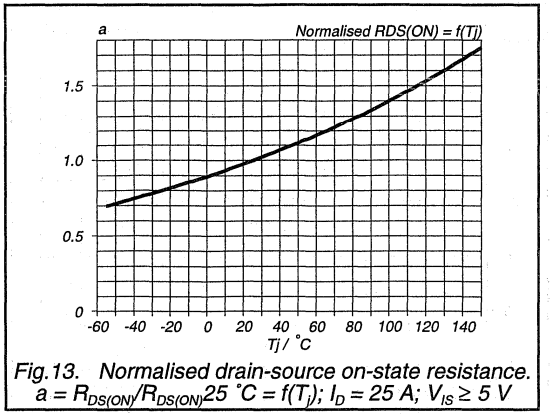


Fig.13. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ °C = f(T_j)$; I_D = 25 A; $V_{IS} \geq 5$ V

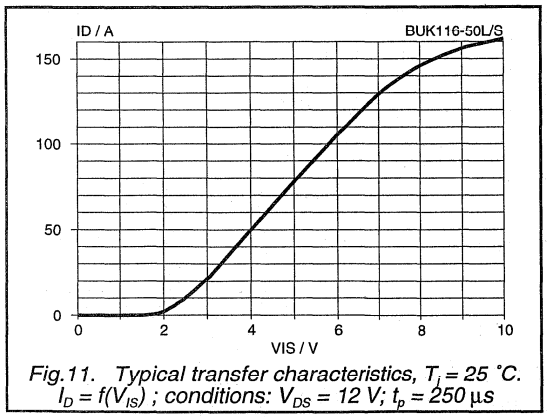


Fig.11. Typical transfer characteristics, T_j = 25 °C. $I_D = f(V_{IS})$; conditions: V_{DS} = 12 V; t_p = 250 µs

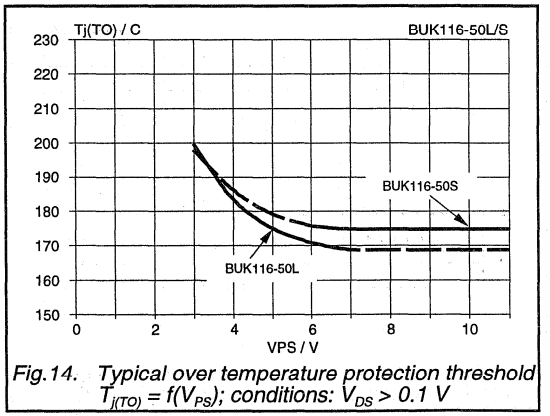


Fig.14. Typical over temperature protection threshold $T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

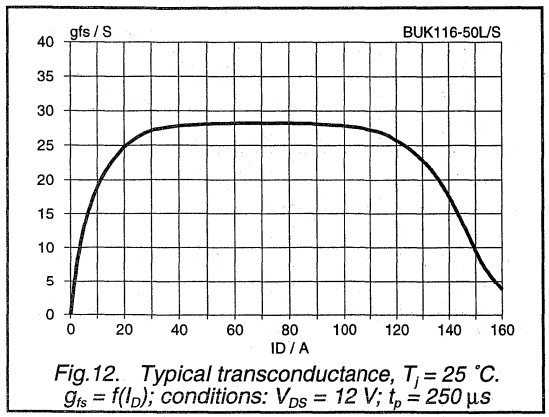


Fig.12. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 12 V; t_p = 250 µs

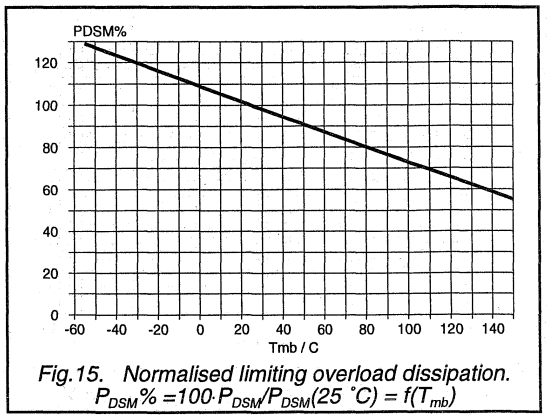


Fig.15. Normalised limiting overload dissipation. $P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ °C) = f(T_{mb})$

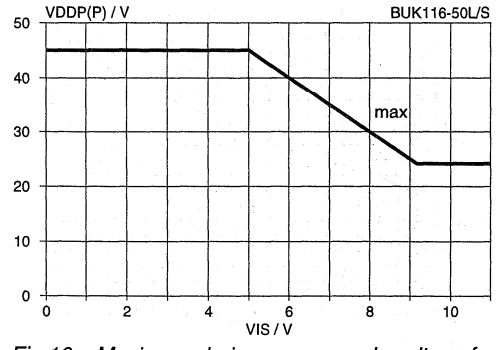


Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ ˚C

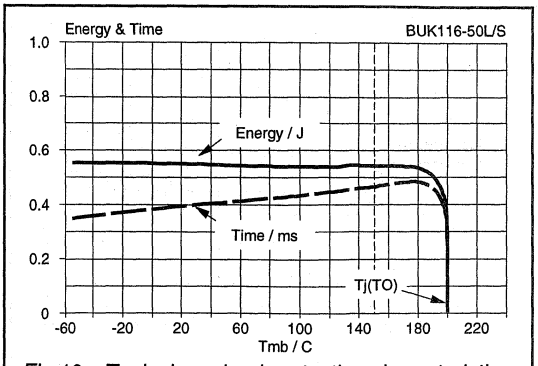


Fig.19. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; $V_{PS} = V_{PSN}$, V_{IS} = 8 V; SC load

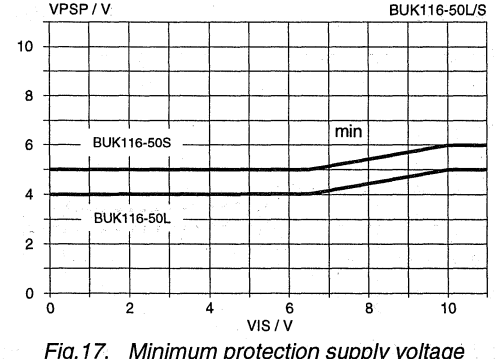


Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ ˚C

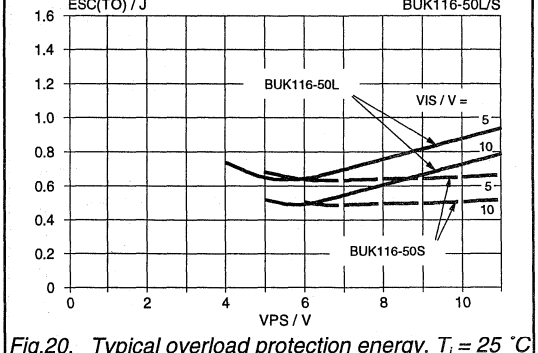


Fig.20. Typical overload protection energy, T_j = 25 ˚C $E_{SC(TO)} = f(V_{PS})$; conditions: V_{DS} = 13 V, parameter V_{IS}

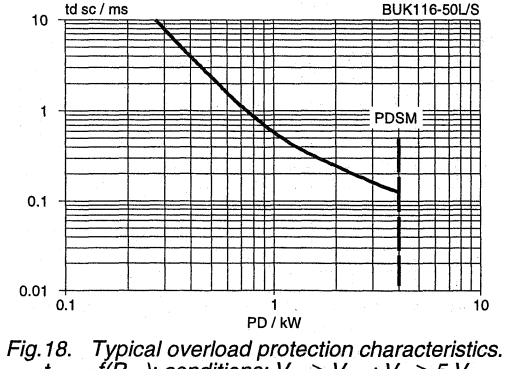


Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

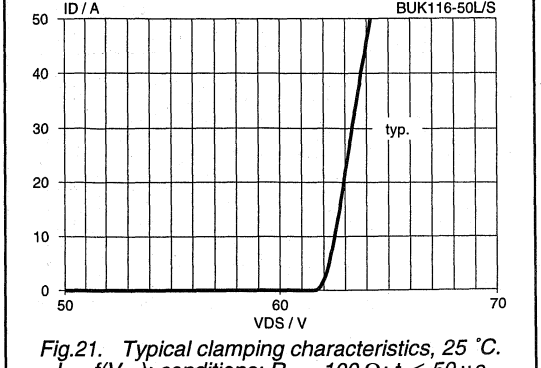


Fig.21. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: R_{IS} = 100 Ω; $t_p \leq 50$ µs

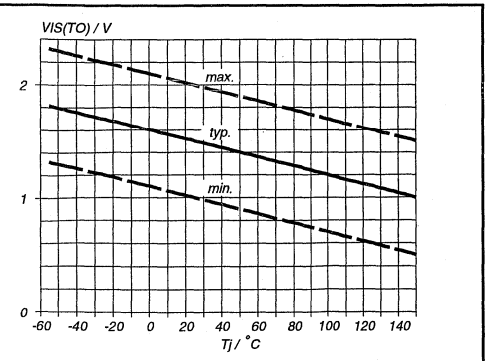


Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

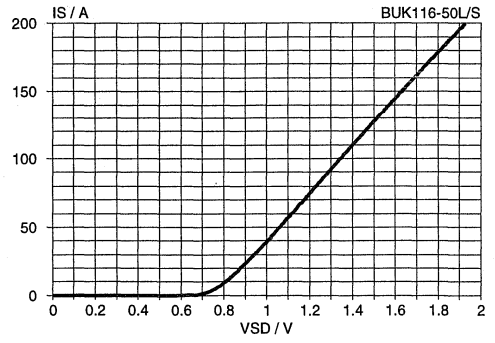


Fig.25. Typical reverse diode current, T_j = 25 °C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

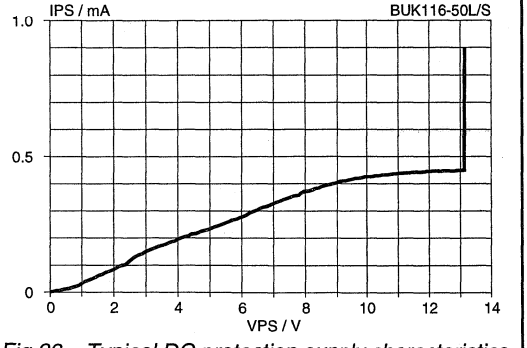


Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 °C

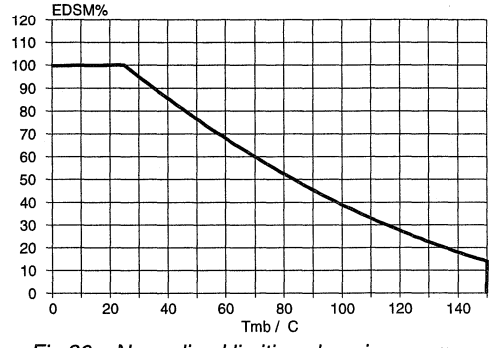


Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; conditions: I_D = 27 A

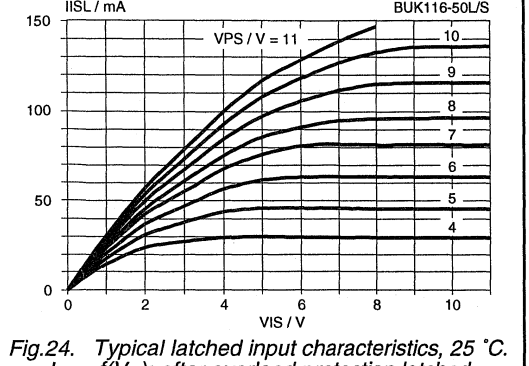


Fig.24. Typical latched input characteristics, 25 °C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

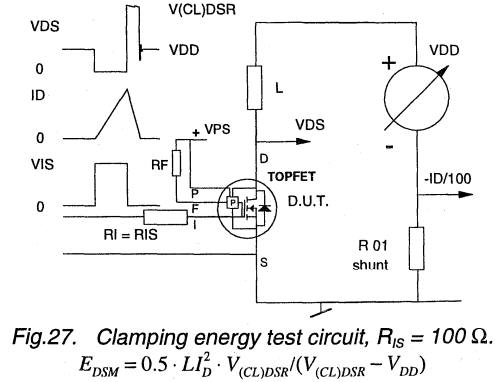


Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$

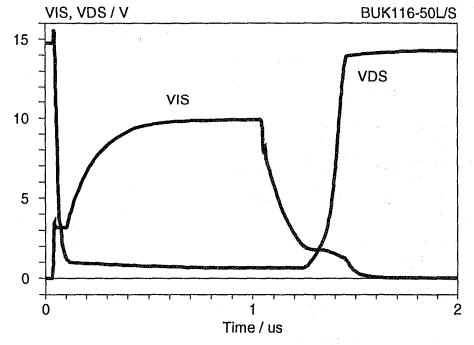


Fig.28. Typical resistive load switching waveforms $R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ °C

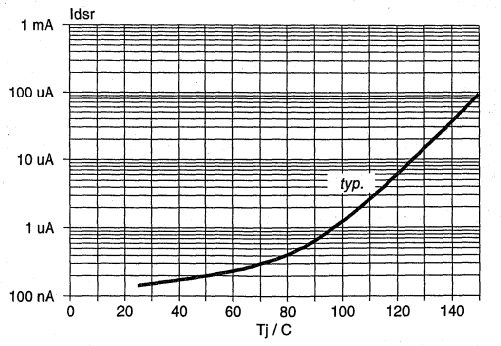


Fig.31. Typical off-state leakage current. $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

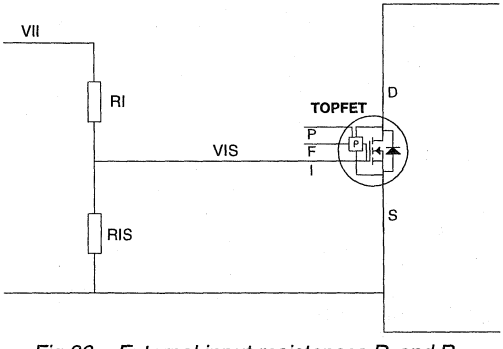


Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

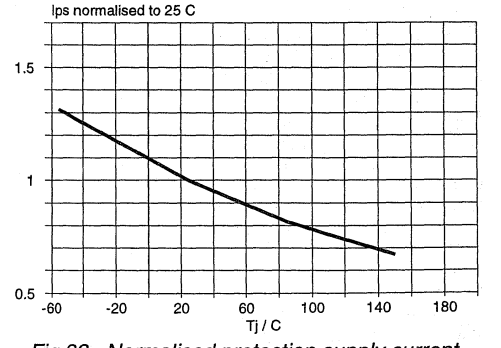


Fig.32. Normalised protection supply current. $I_{PS}/I_{PS}25$ °C = $f(T_j)$; $V_{PS} = V_{PSN}$

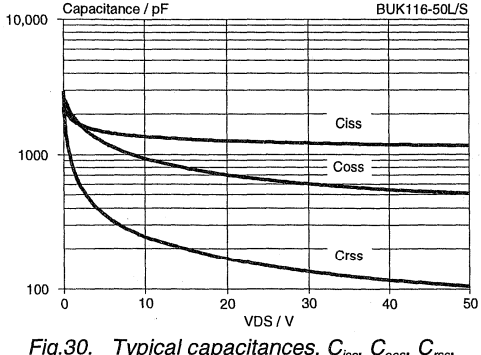


Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; $f = 1$ MHz

PowerMOS transistor TOPFET high side switch

BUK200-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	3.5	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	10	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	100	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

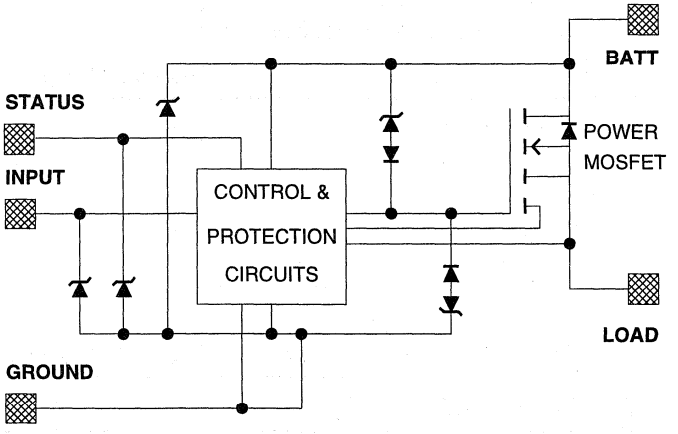


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

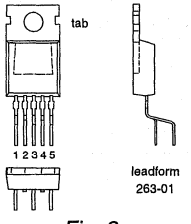


Fig. 2.

SYMBOL

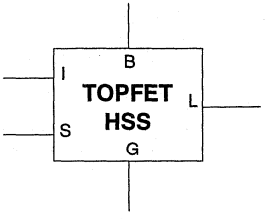


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115$ °C	-	10	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	62.5	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.5	2	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	3.5	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 5 A; t_p = 300 µs	-	77	100	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1 A; t_p = 300 µs	-	116	150	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	50	200	350	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	8.5	10.3	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 80 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	35	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 8.5 V; t_p = 300 µs	23	33	43	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	330	460	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

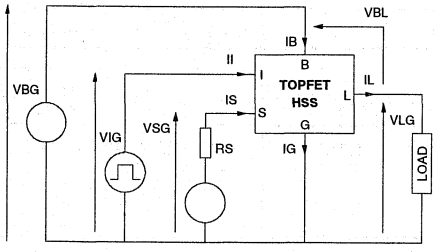


Fig.4. High side switch measurements schematic. (current and voltage conventions)

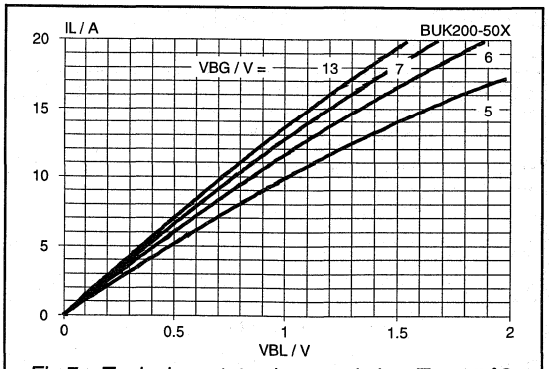


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

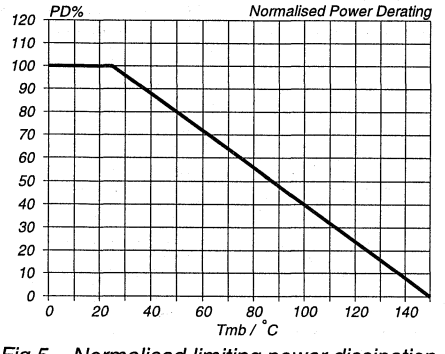


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

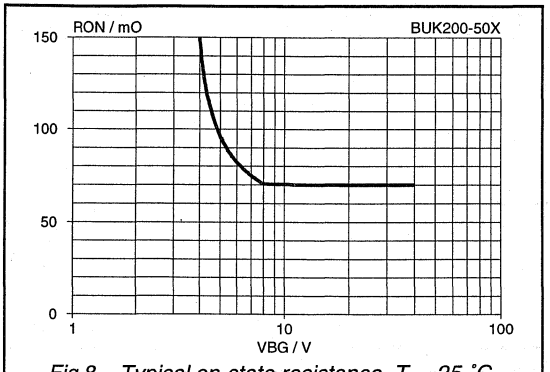


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 5 A; t_p = 300 µs

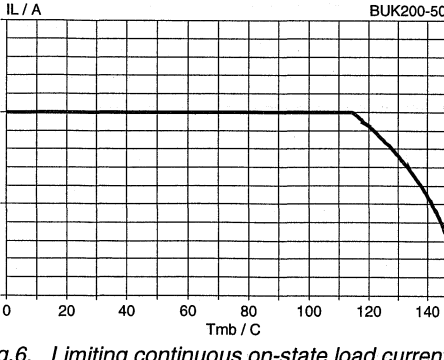


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

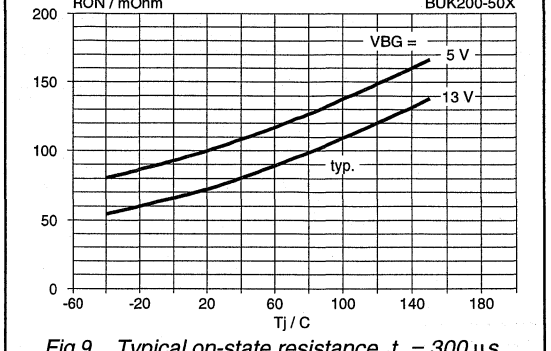


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1 A

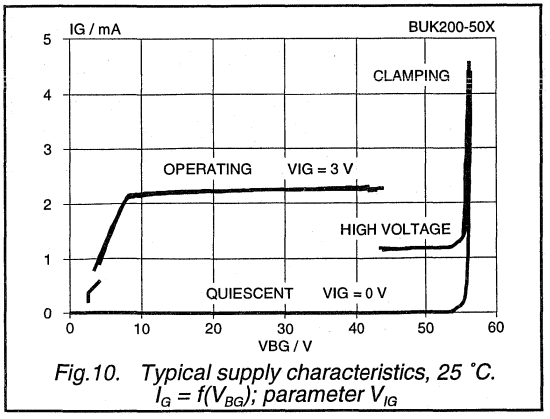


Fig.10. Typical supply characteristics, 25 °C.
$I_G = f(V_{BG})$; parameter V_{IG}

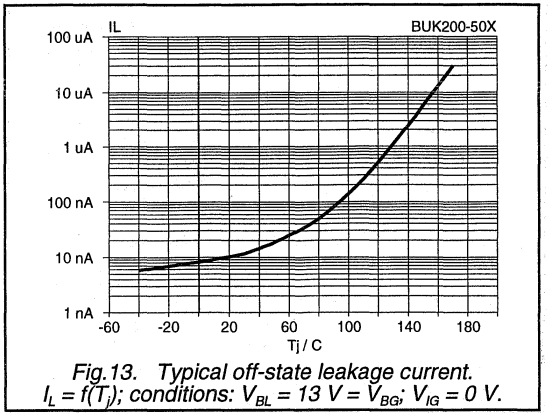


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

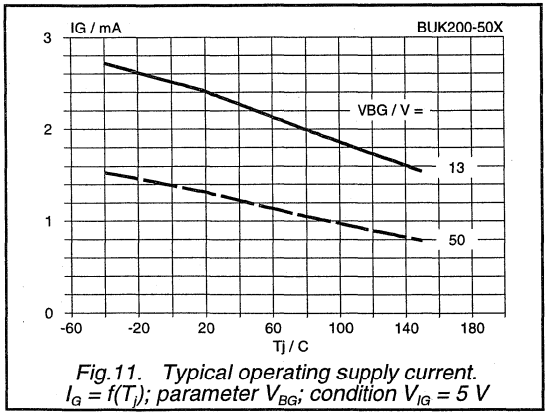


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

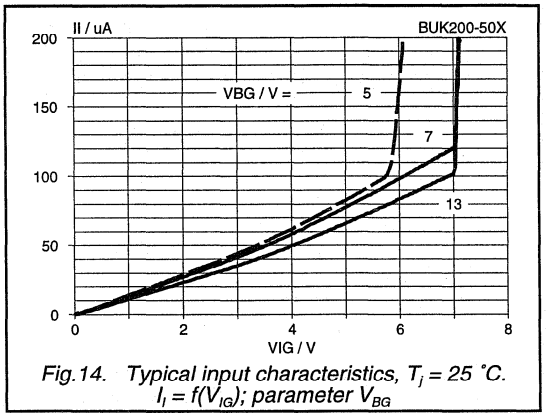


Fig.14. Typical input characteristics, T_j = 25 °C.
$I_I = f(V_{IG})$; parameter V_{BG}

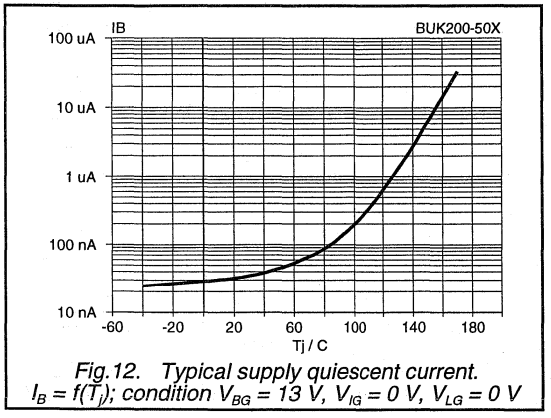


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

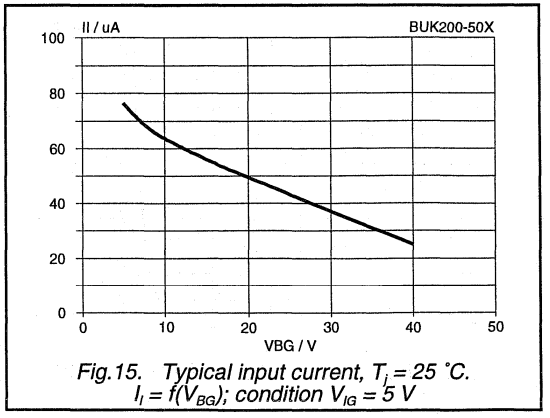


Fig.15. Typical input current, T_j = 25 °C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

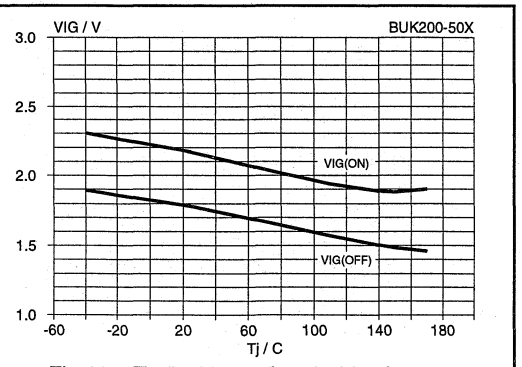


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 50 mA

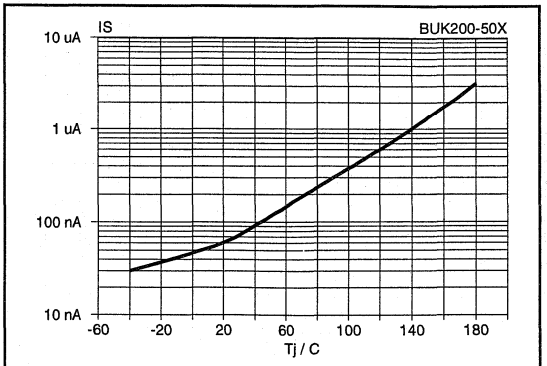


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

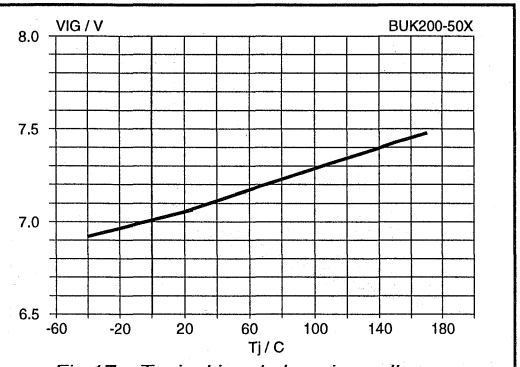


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

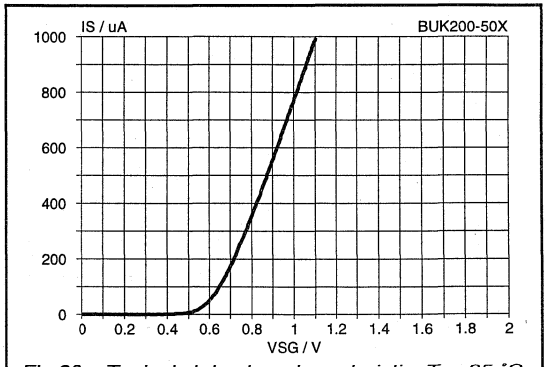


Fig.20. Typical status low characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

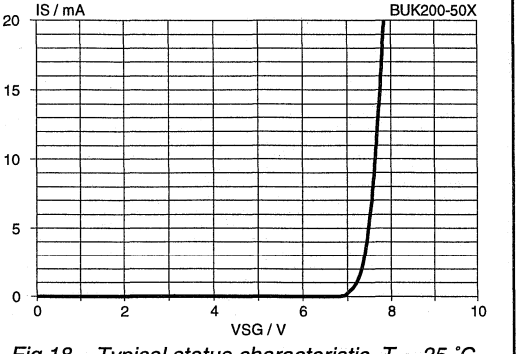


Fig.18. Typical status characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

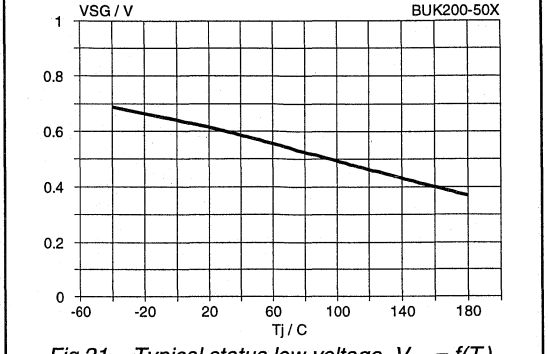


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

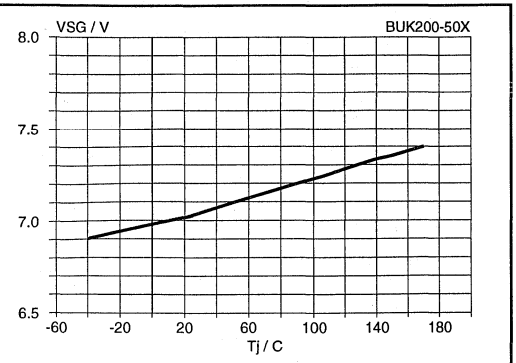


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

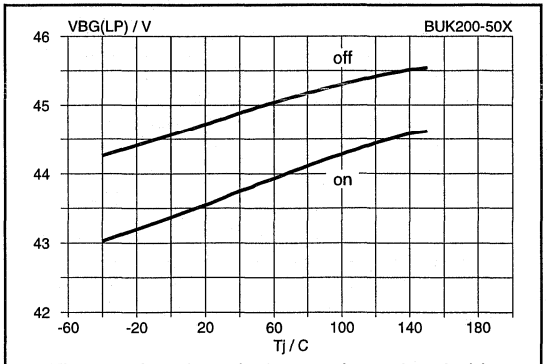


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 50\ mA$

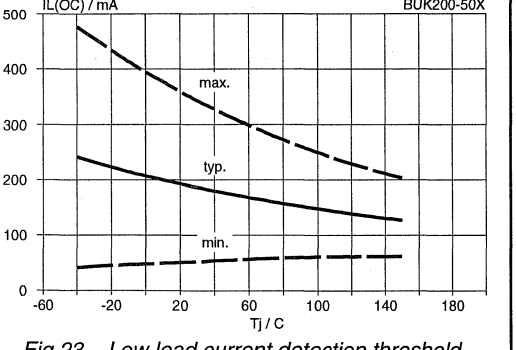


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

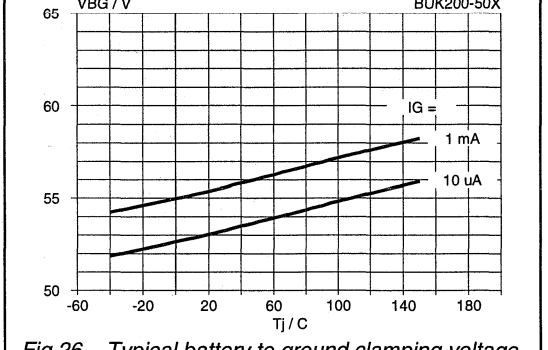


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

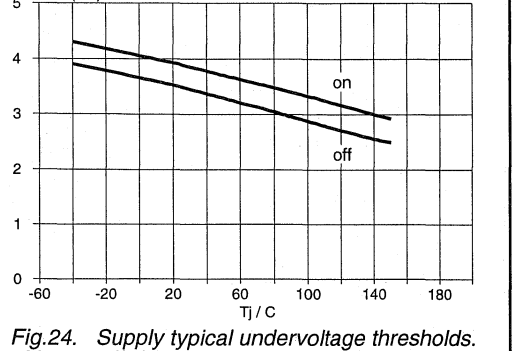


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 50\ mA$

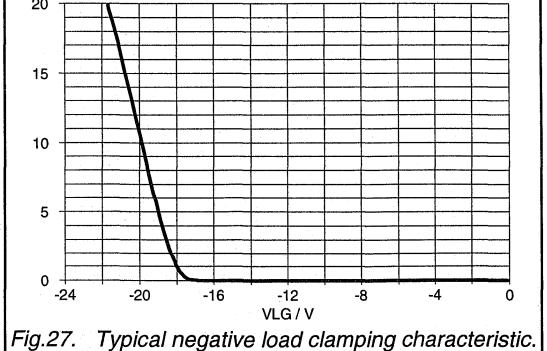


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

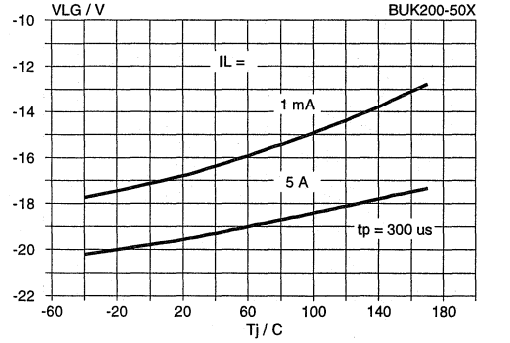


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

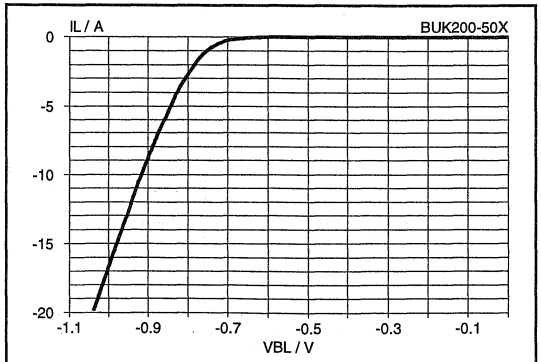


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

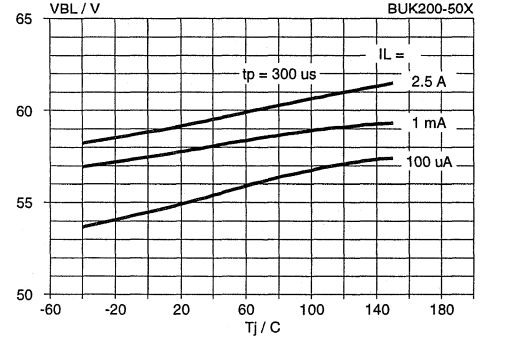


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

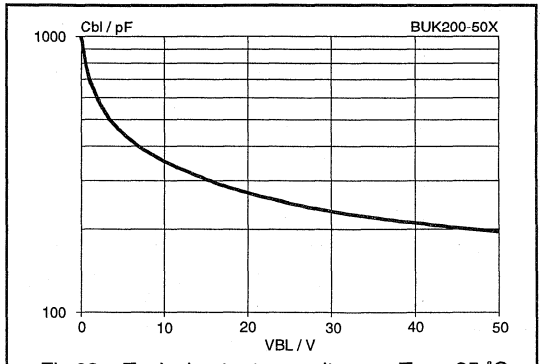


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

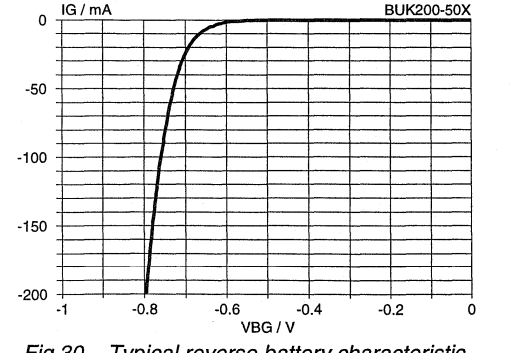


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

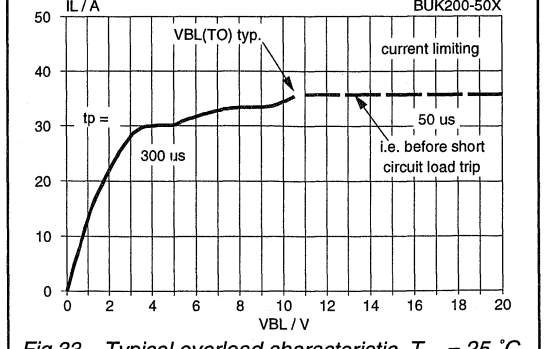


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

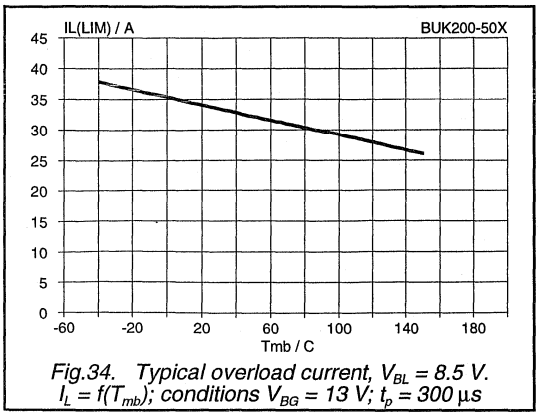


Fig.34. Typical overload current, V_{BL} = 8.5 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

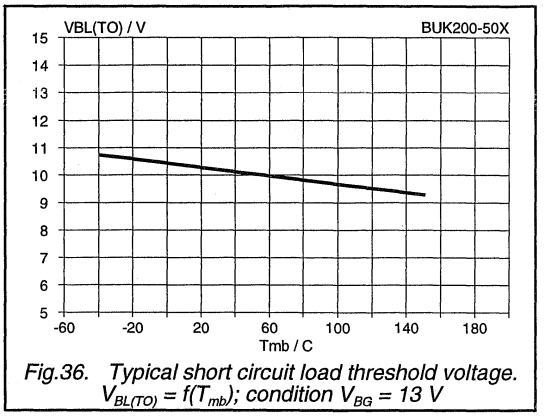


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

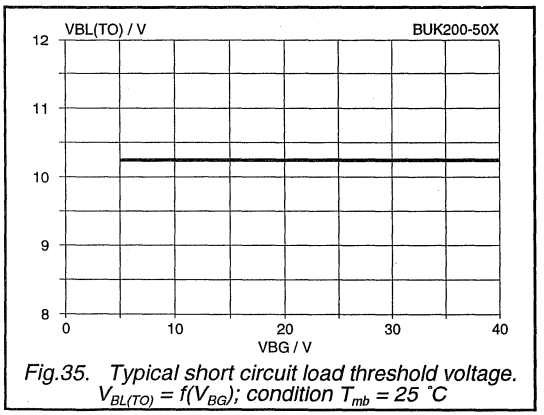


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

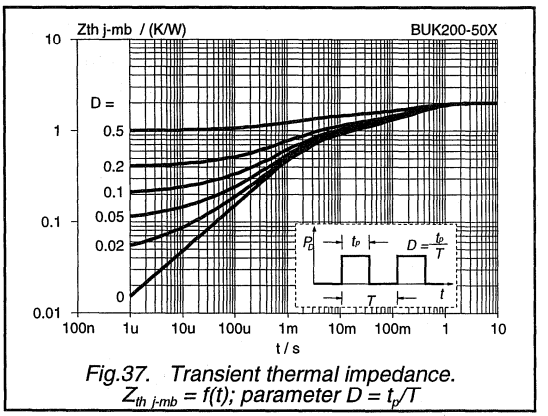


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK200-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	3.5	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	10	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	100	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

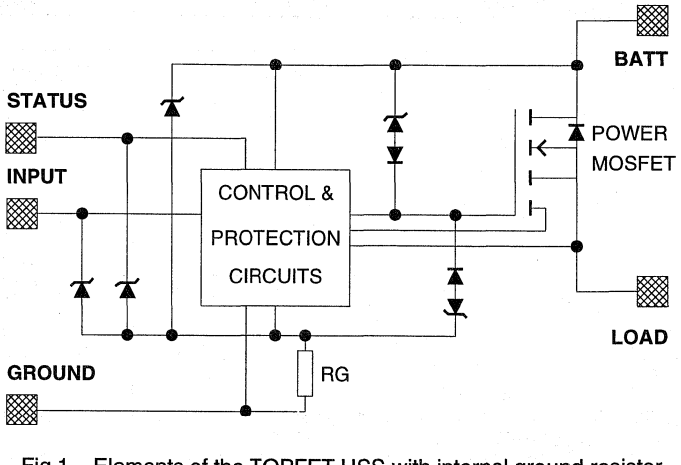


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

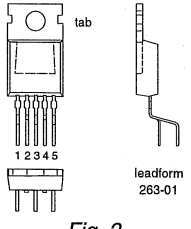


Fig. 2.

SYMBOL

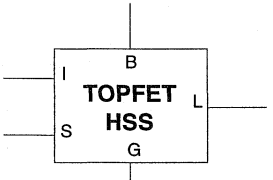


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115\ ^\circ C$	-	10	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	62.5	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.5	2	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	3.5	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 5 A; t_p = 300 µs	-	77	100	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1 A; t_p = 300 µs	-	116	150	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	50	200	350	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	8.5	10.3	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 80 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	35	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 8.5 V; t_p = 300 µs	23	33	43	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	330	460	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

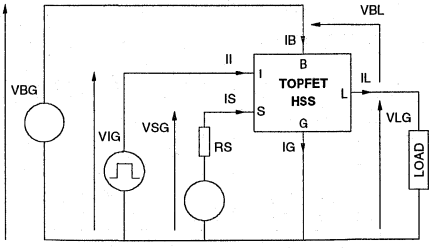


Fig.4. High side switch measurements schematic. (current and voltage conventions)

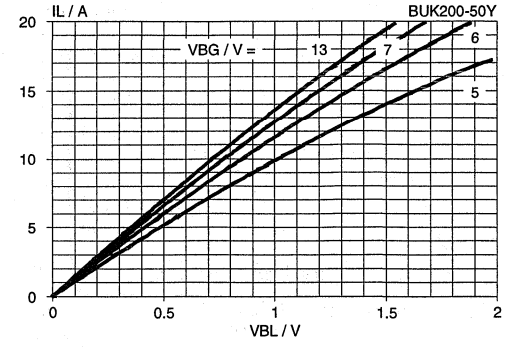


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

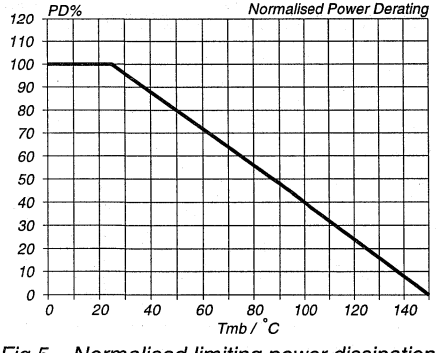


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

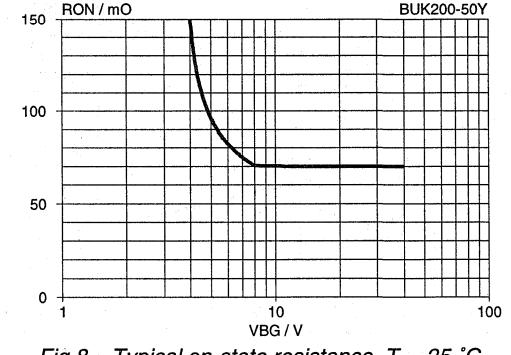


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 5 A; t_p = 300 µs

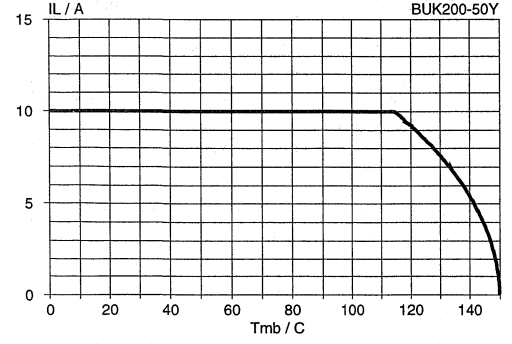


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

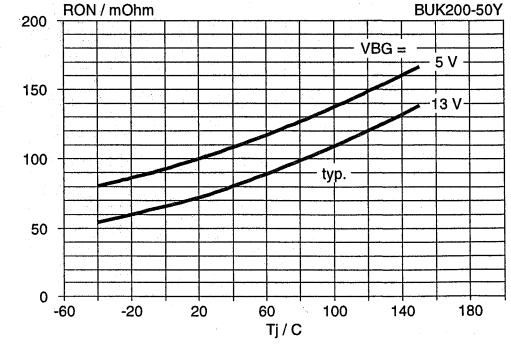


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1 A

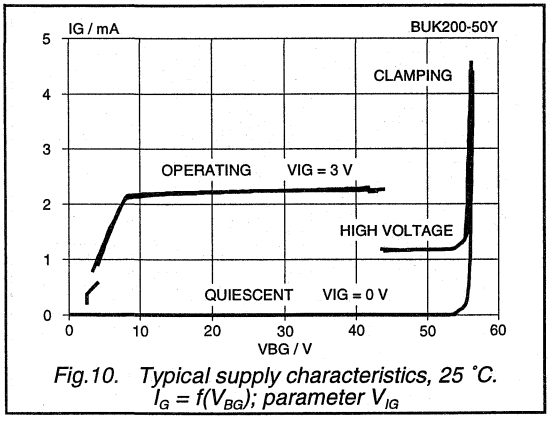


Fig.10. Typical supply characteristics, 25 °C. $I_G = f(V_{BG})$; parameter V_{IG}

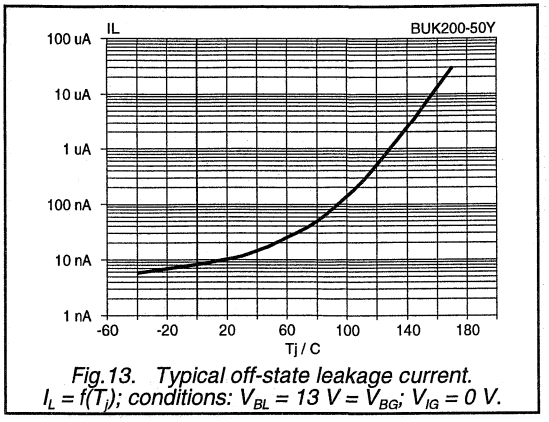


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: $V_{BL} = 13$ V = V_{BG}; $V_{IG} = 0$ V.

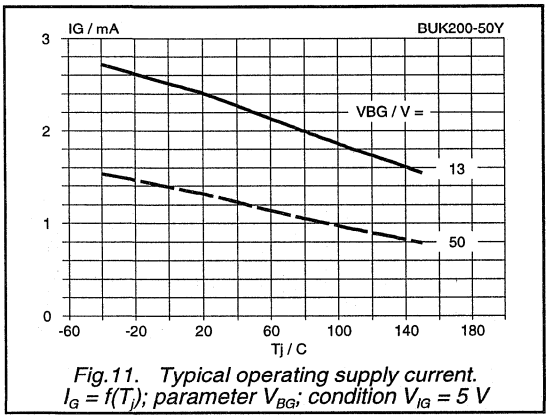


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition $V_{IG} = 5$ V

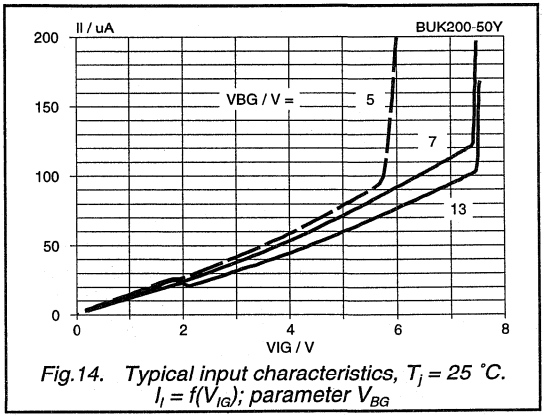


Fig.14. Typical input characteristics, $T_j = 25$ °C. $I_I = f(V_{IG})$; parameter V_{BG}

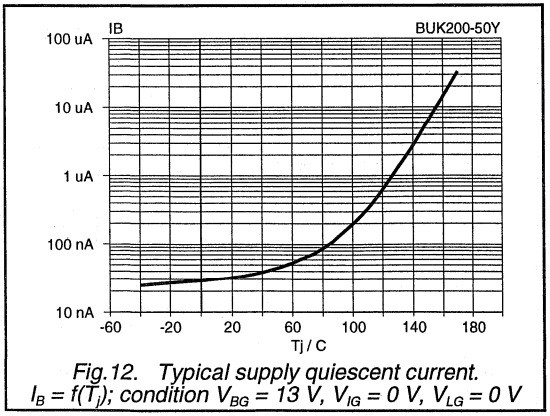


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition $V_{BG} = 13$ V, $V_{IG} = 0$ V, $V_{LG} = 0$ V

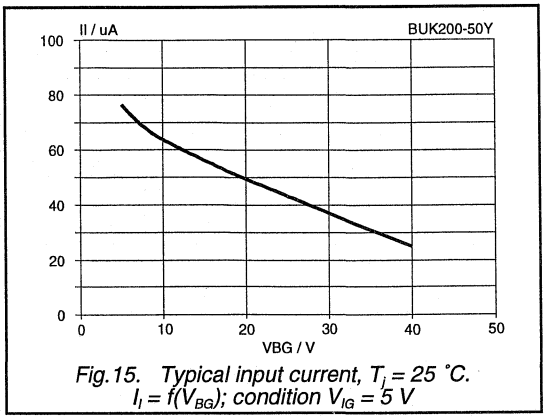


Fig.15. Typical input current, $T_j = 25$ °C. $I_I = f(V_{BG})$; condition $V_{IG} = 5$ V

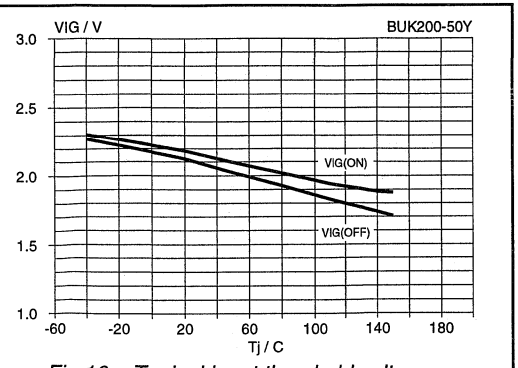


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions $V_{BG} = 13$ V, $I_L = 50$ mA

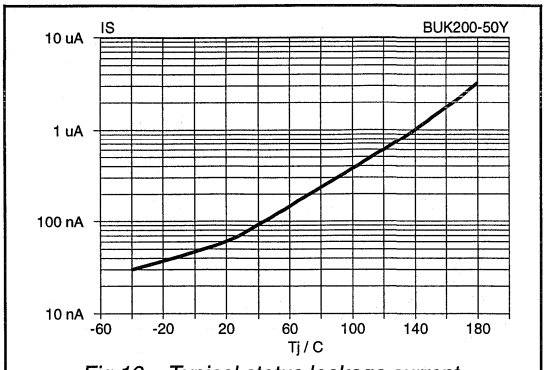


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions $V_{SG} = 5$ V, $V_{IG} = V_{BG} = 0$ V

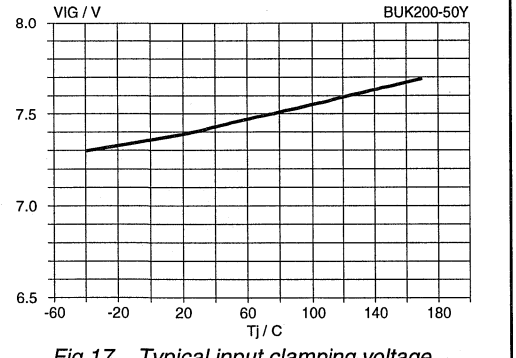


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions $I_I = 200$ µA, $V_{BG} = 13$ V

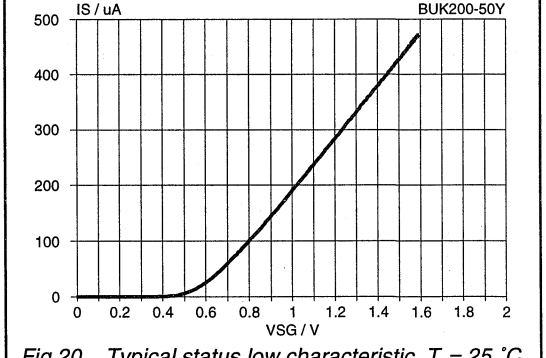


Fig.20. Typical status low characteristic, $T_j = 25$ °C. $I_S = f(V_{SG})$; conditions $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

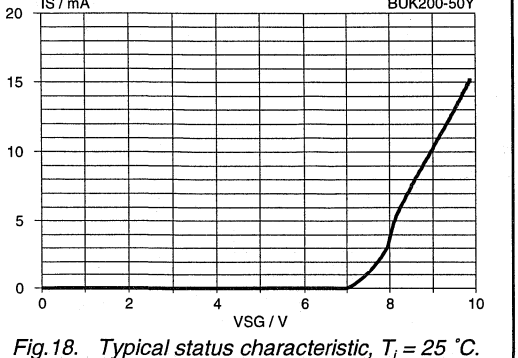


Fig.18. Typical status characteristic, $T_j = 25$ °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG} = 0$ V

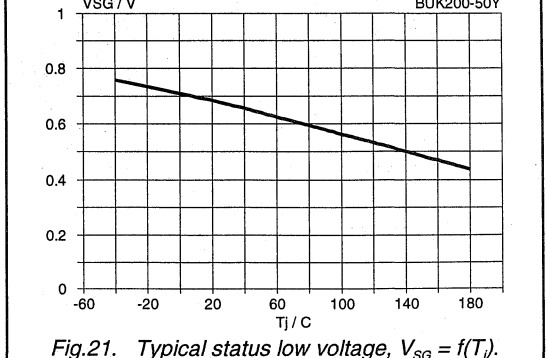


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions $I_S = 50$ µA, $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

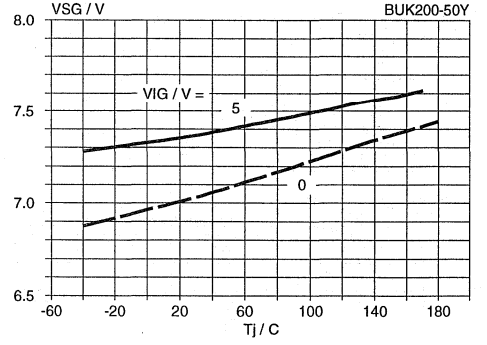


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100$ µA, $V_{BG} = 13$ V

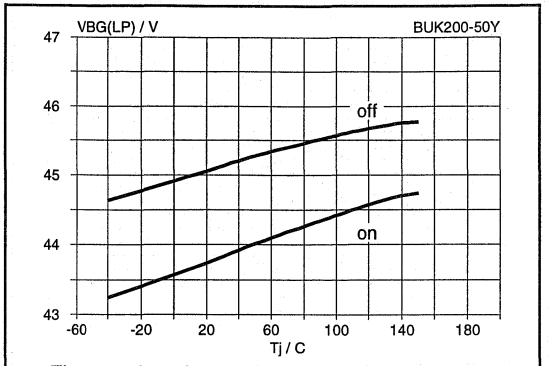


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5$ V; $I_L = 50$ mA

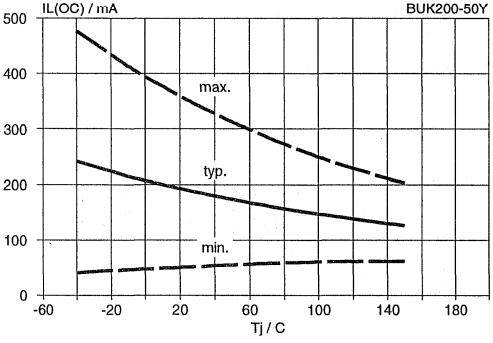


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5$ V; $V_{BG} = 13$ V

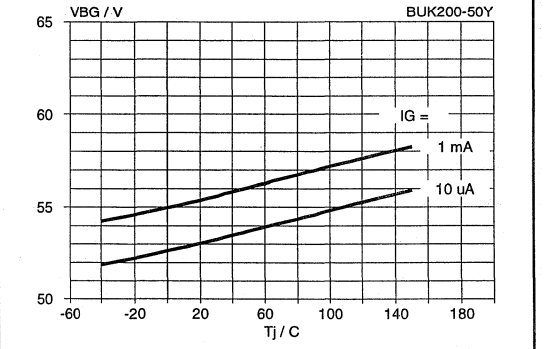


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

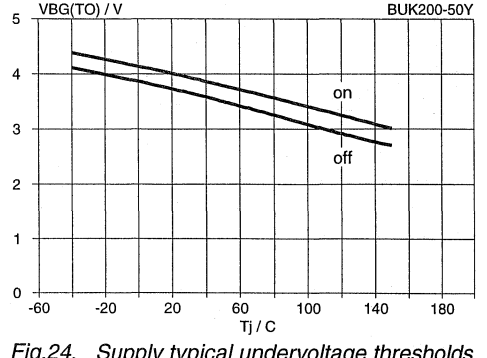


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3$ V; $I_L = 50$ mA

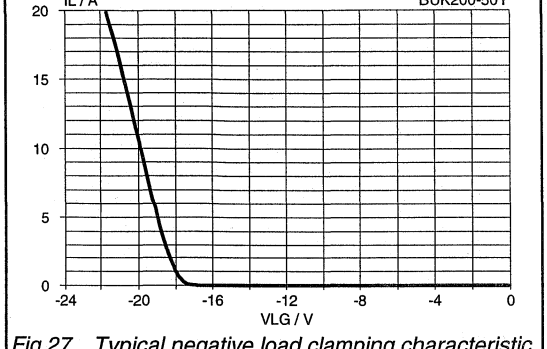


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0$ V, $t_p = 300$ µs, 25 °C

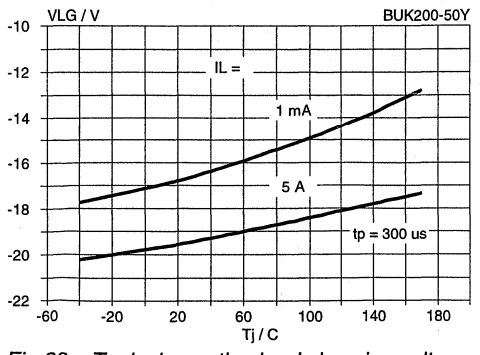


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

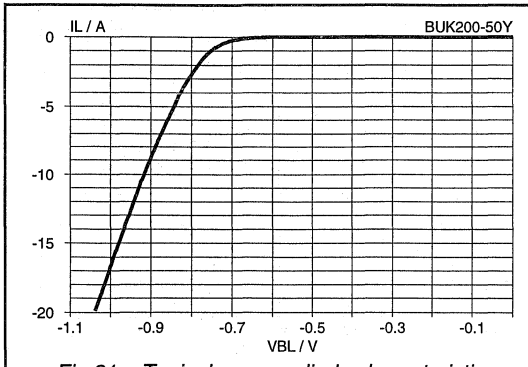


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

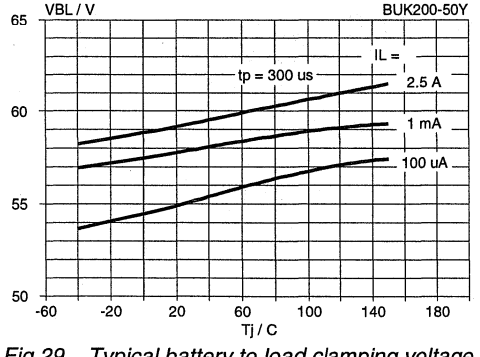


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

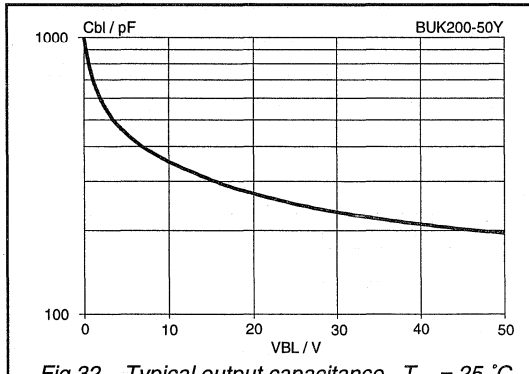


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

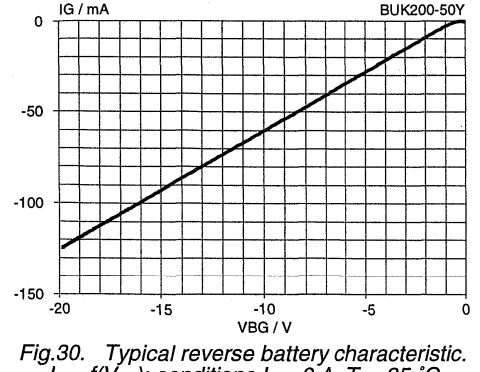


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

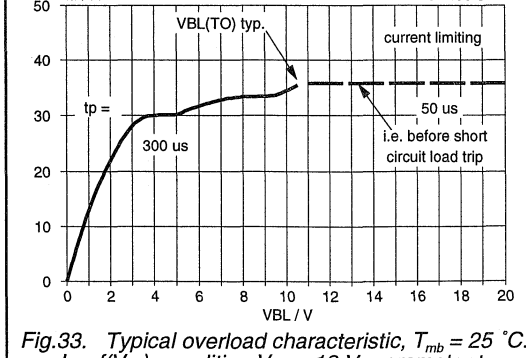


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

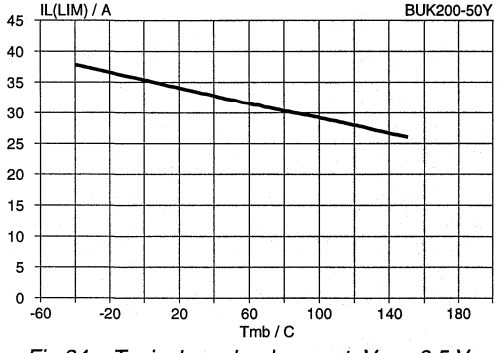


Fig.34. Typical overload current, V_{BL} = 8.5 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

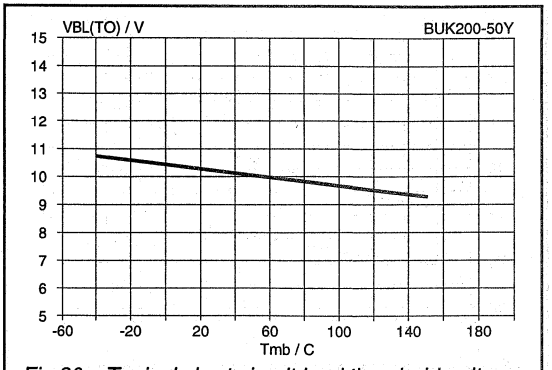


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

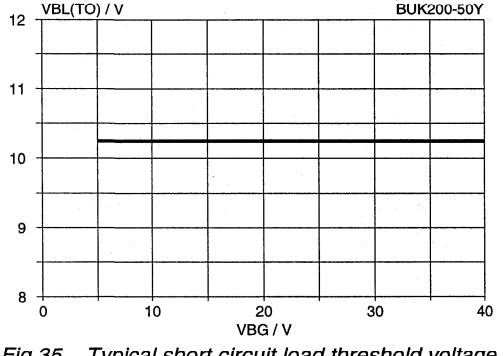


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 ˚C

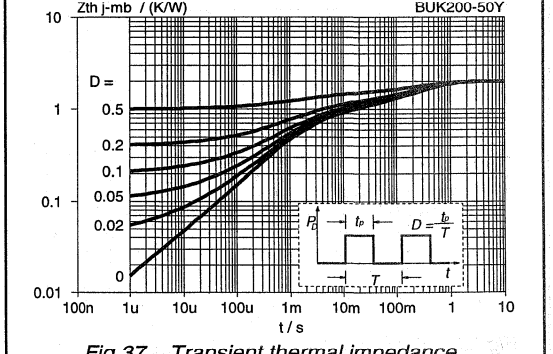


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK201-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	15	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	60	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

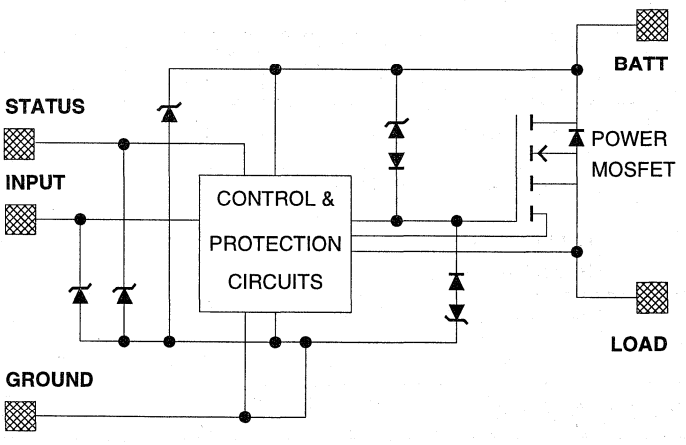


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

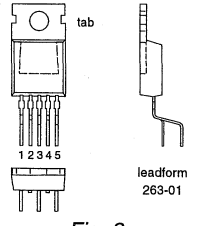


Fig. 2.

SYMBOL

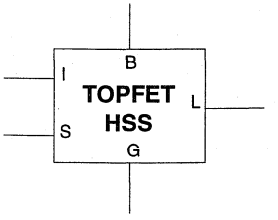


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115$ °C	-	15	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	83.3	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	T_{mb} = 150 °C prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.2	1.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 7.5 A; t_p = 300 µs	-	45	60	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1.5 A; t_p = 300 µs	-	70	90	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	100	350	600	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 140 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 7.5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	28	40	52	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	415	580	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

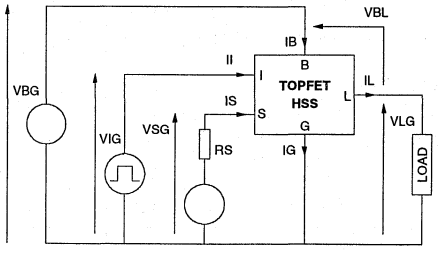


Fig.4. High side switch measurements schematic. (current and voltage conventions)

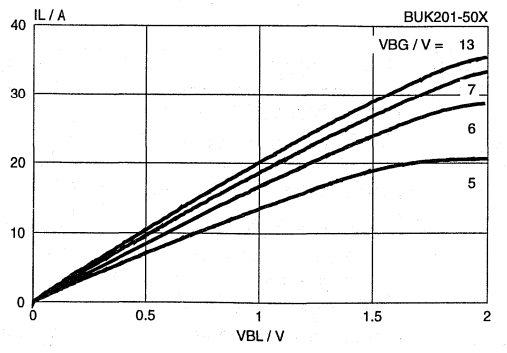


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

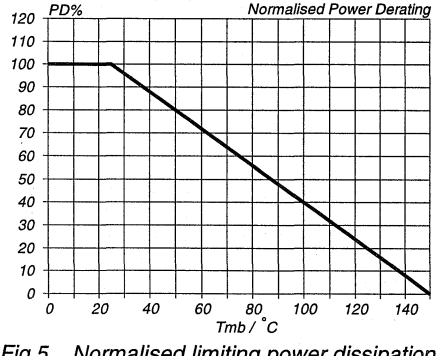


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

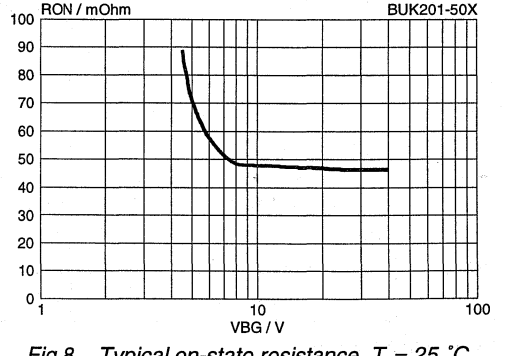


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 7.5 A; t_p = 300 µs

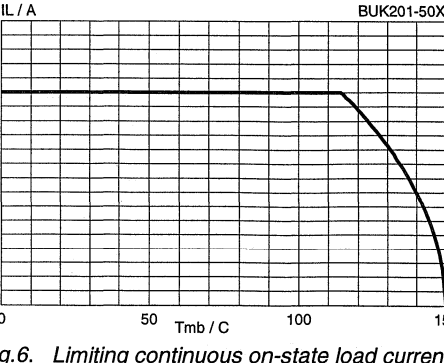


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

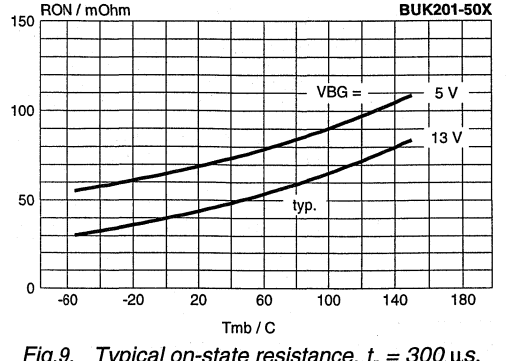


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1.5 A

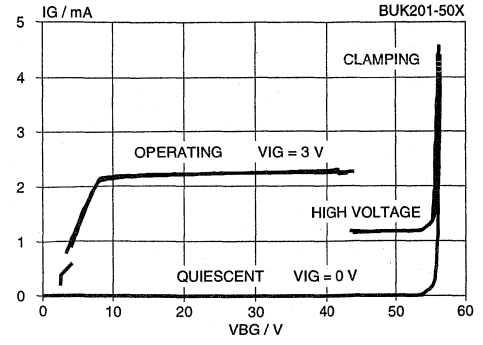


Fig.10. Typical supply characteristics, 25 °C.
$I_G = f(V_{BG})$; parameter V_{IG}

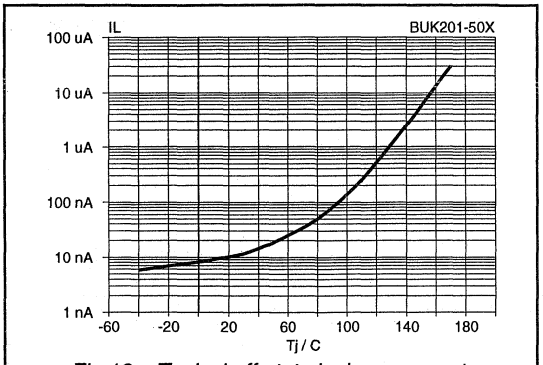


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

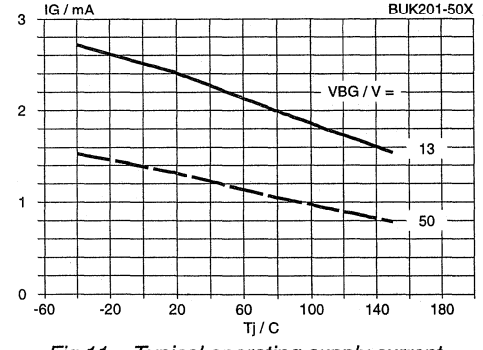


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

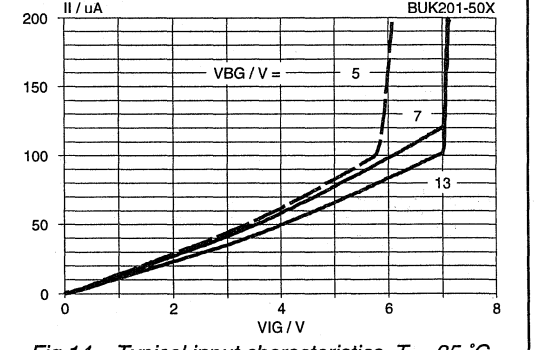


Fig.14. Typical input characteristics, T_j = 25 °C.
$I_I = f(V_{IG})$; parameter V_{BG}

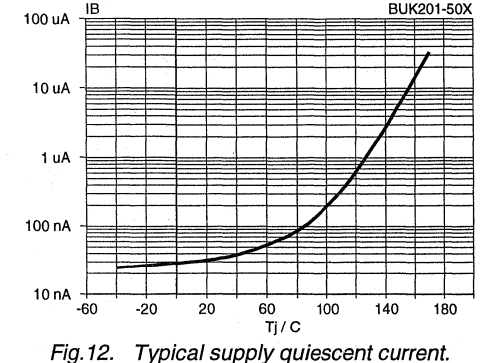


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

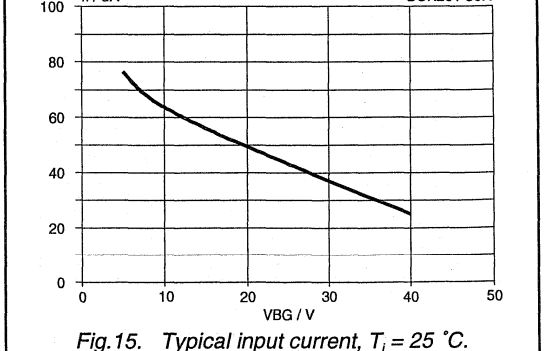


Fig.15. Typical input current, T_j = 25 °C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

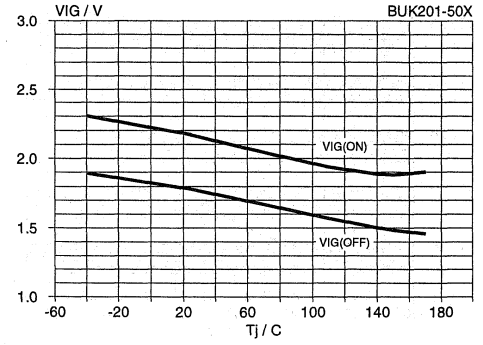


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 80 mA

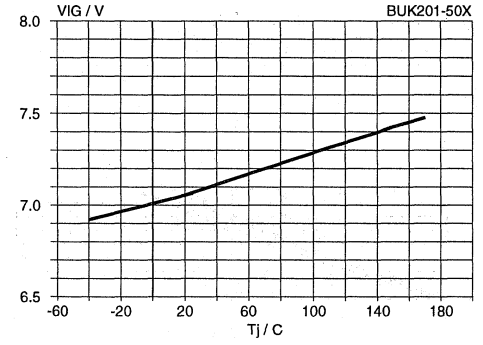


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

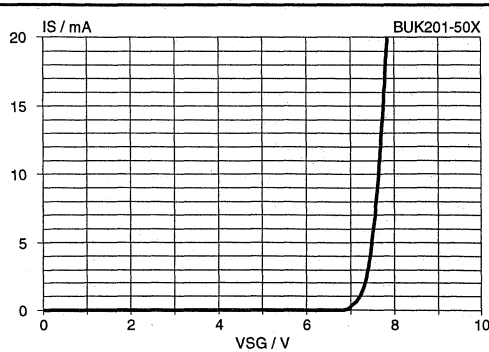


Fig.18. Typical status characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

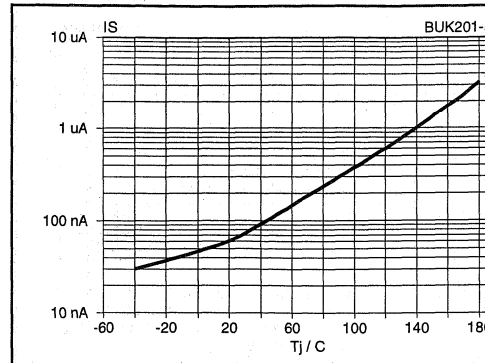


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

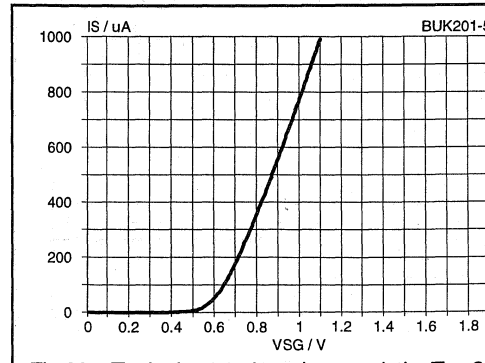


Fig.20. Typical status low characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

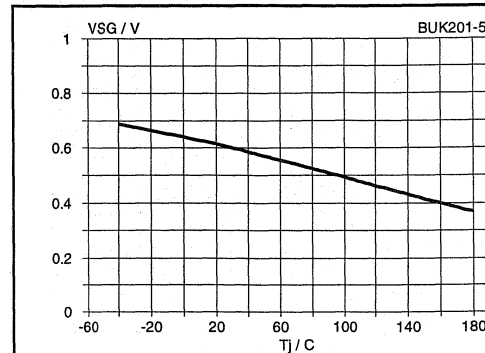


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

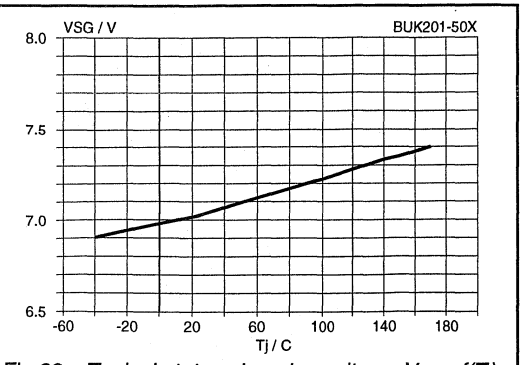


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

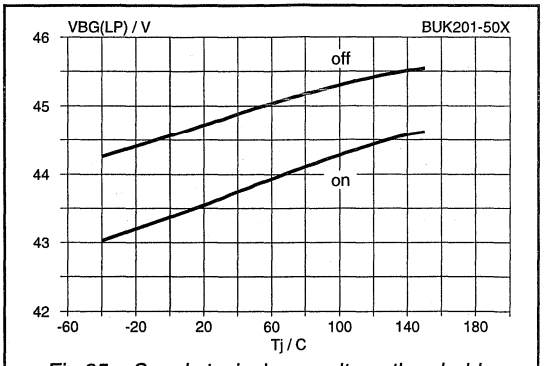


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 80\ mA$

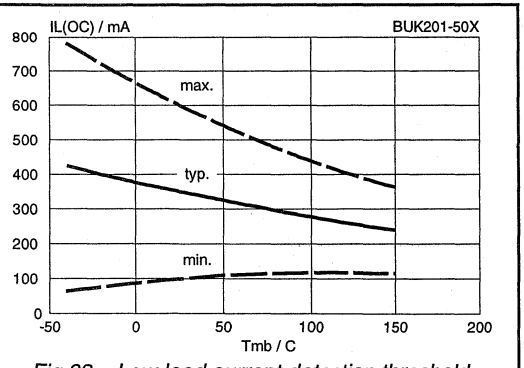


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

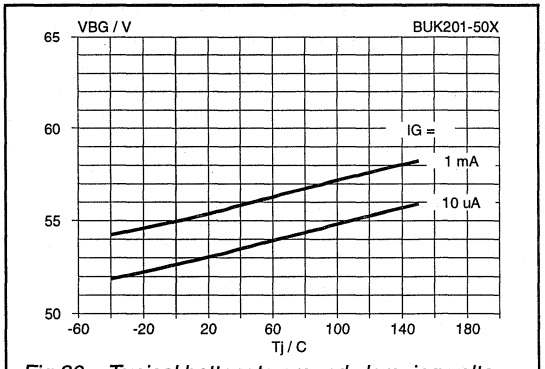


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

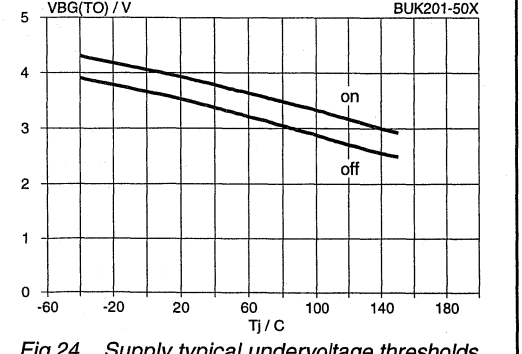


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 80\ mA$

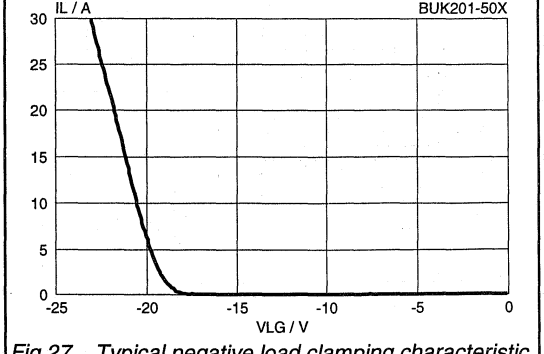


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 ˚C

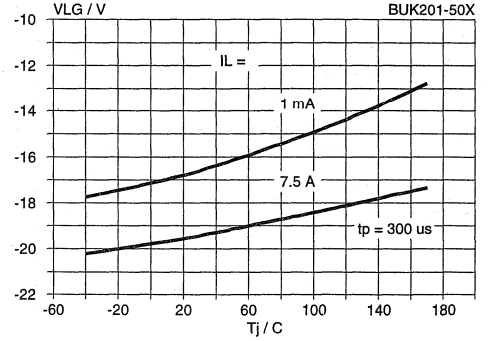


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

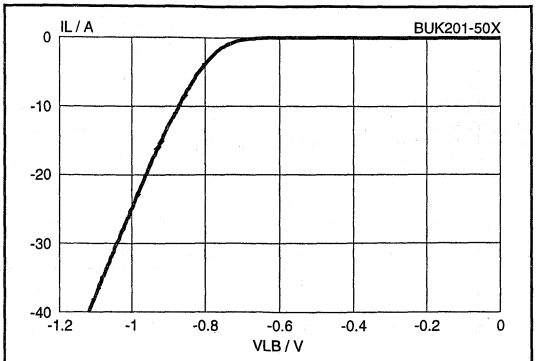


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

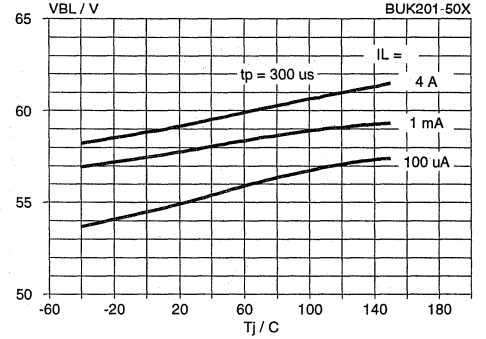


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

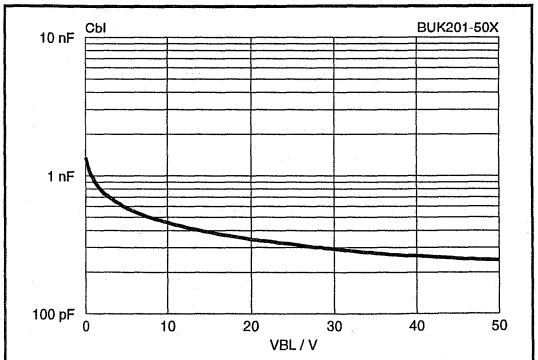


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

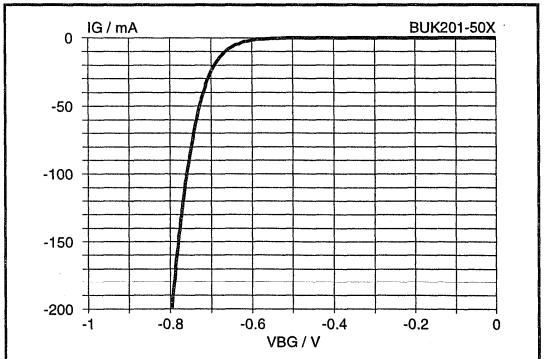


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

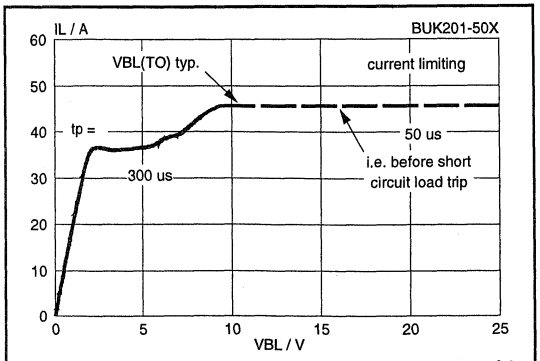


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

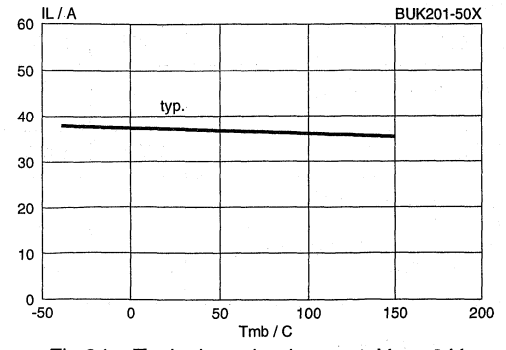


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

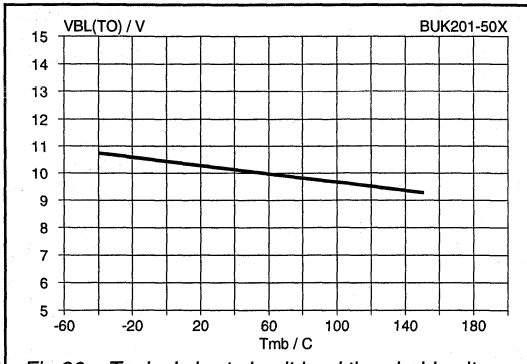


Fig.36. Typical short circuit threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

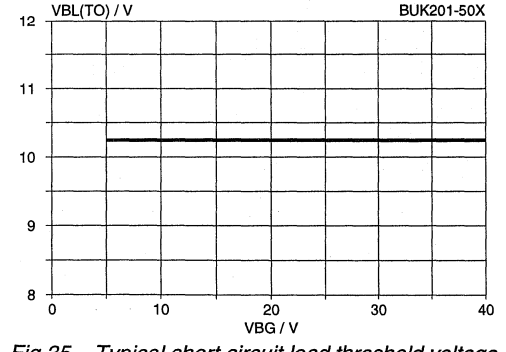


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

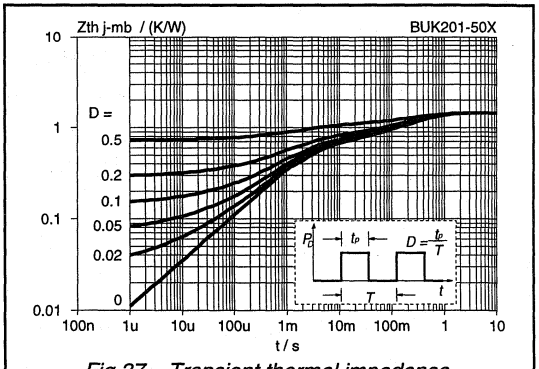


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK201-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	15	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	60	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

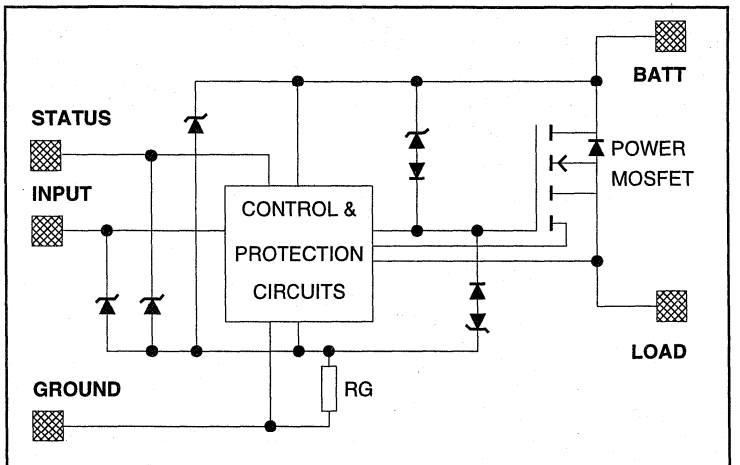


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

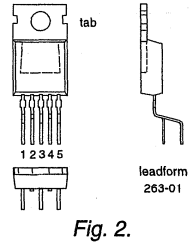


Fig. 2.

SYMBOL

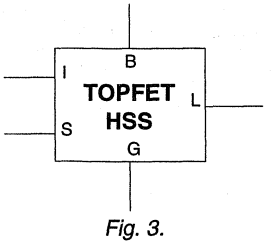


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115\ ^\circ C$	-	15	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	83.3	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.2	1.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 7.5 A; t_p = 300 µs	-	45	60	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1.5 A; t_p = 300 µs	-	70	90	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	100	350	600	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 140 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 7.5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	28	40	52	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	415	580	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

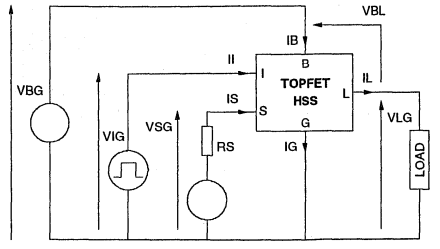


Fig.4. High side switch measurements schematic. (current and voltage conventions)

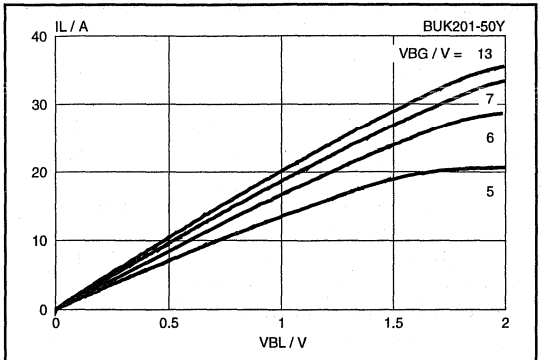


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

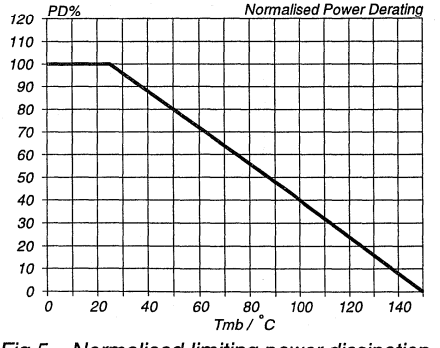


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

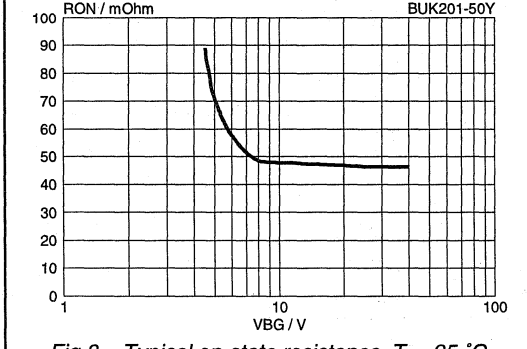


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 7.5 A; t_p = 300 µs

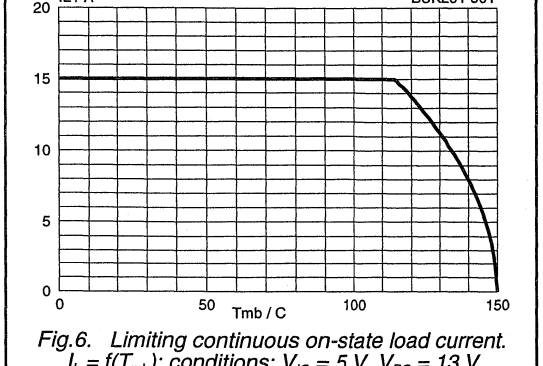


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

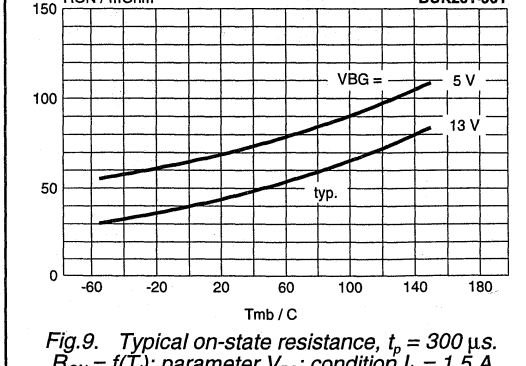


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1.5 A

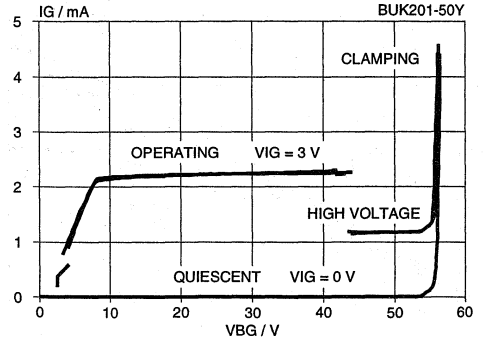


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

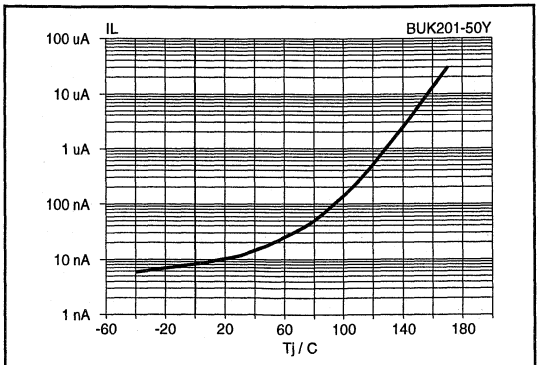


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

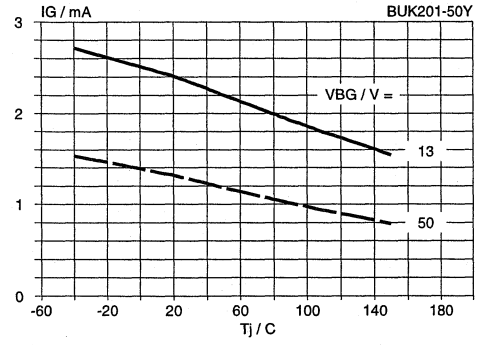


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

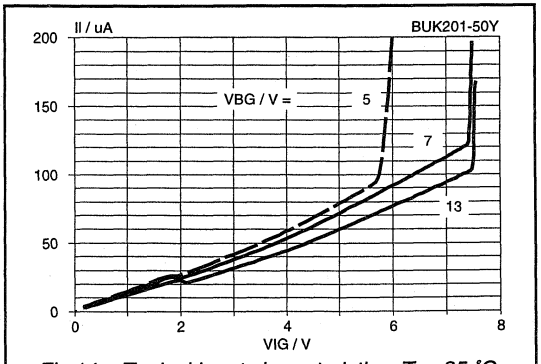


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

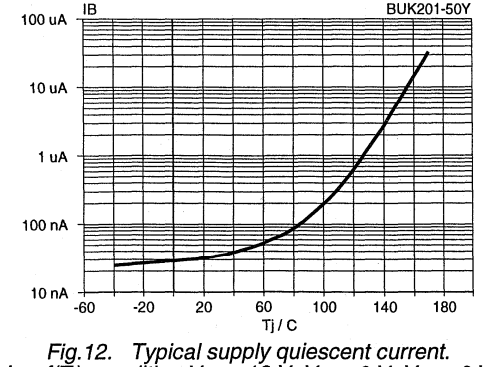


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

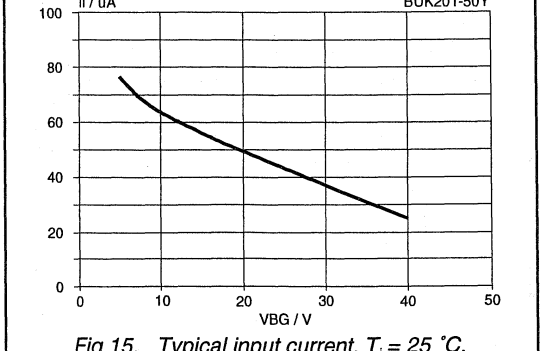


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

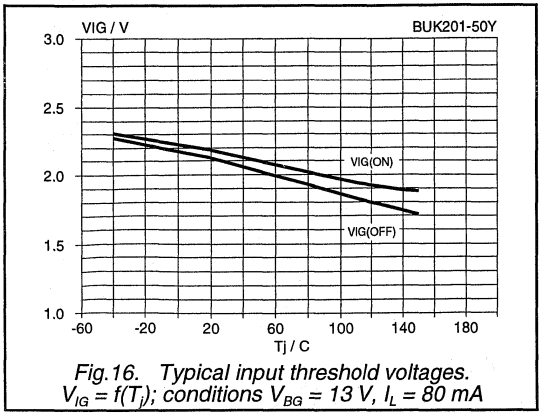


Fig.16. Typical input threshold voltages.
V_{IG} = f(T_j); conditions V_{BG} = 13 V, I_L = 80 mA

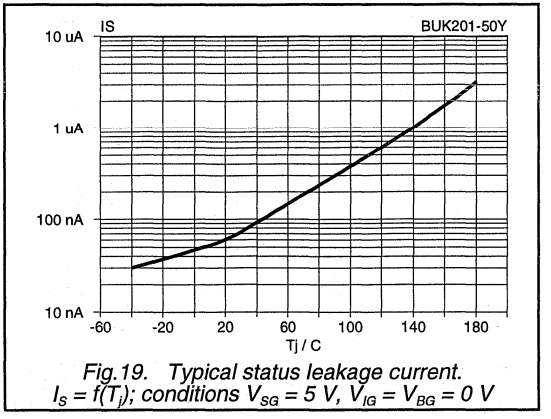


Fig.19. Typical status leakage current.
I_S = f(T_j); conditions V_{SG} = 5 V, V_{IG} = V_{BG} = 0 V

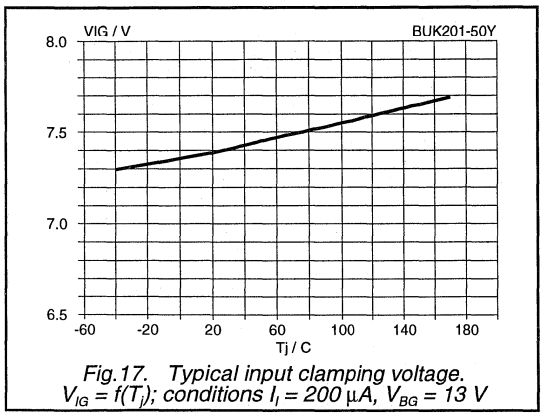


Fig.17. Typical input clamping voltage.
V_{IG} = f(T_j); conditions I_I = 200 µA, V_{BG} = 13 V

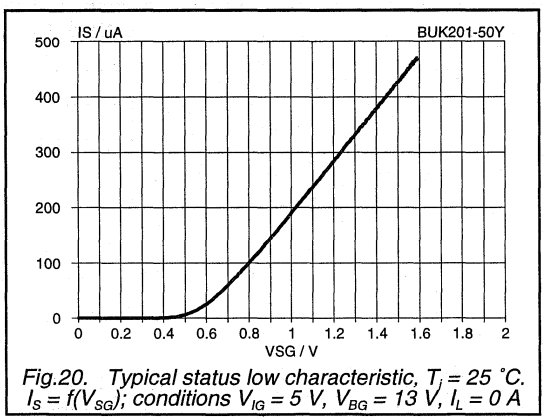


Fig.20. Typical status low characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

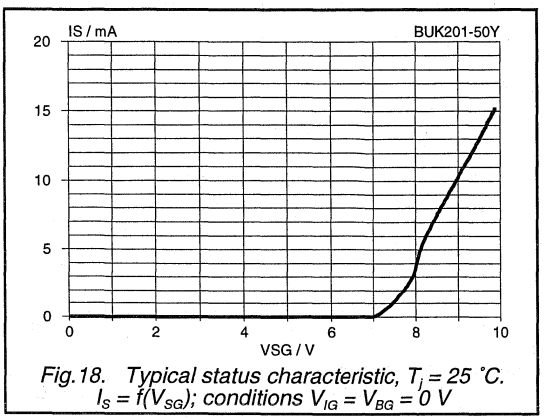


Fig.18. Typical status characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = V_{BG} = 0 V

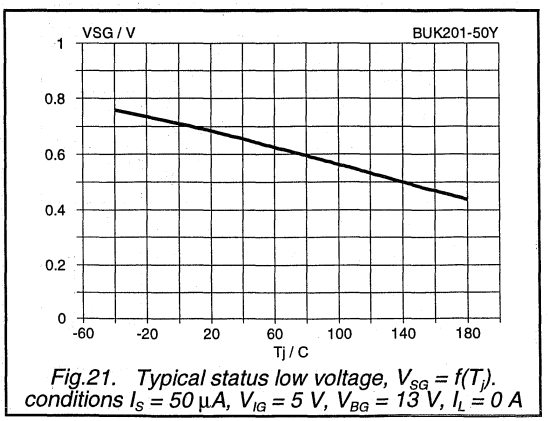


Fig.21. Typical status low voltage, V_{SG} = f(T_j).
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

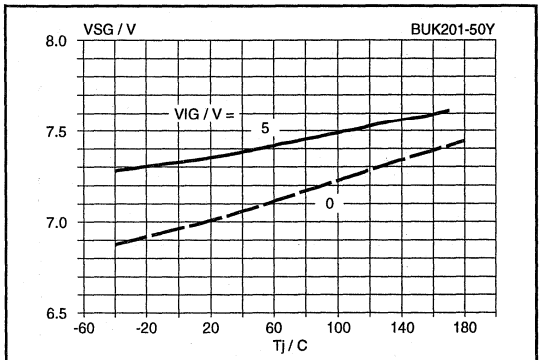


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

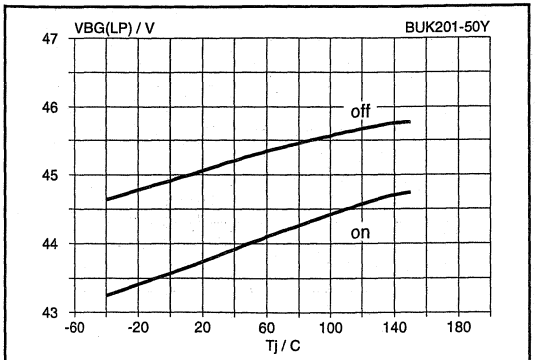


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 80\ mA$

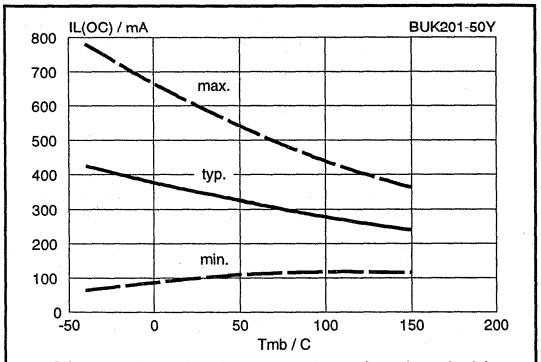


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

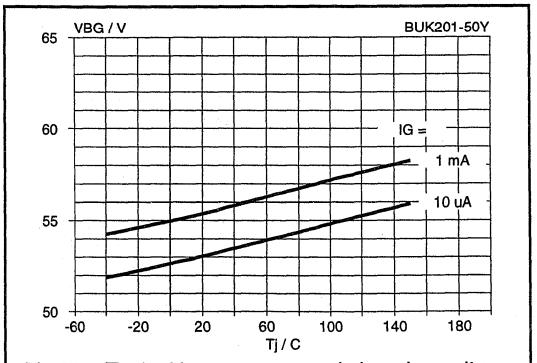


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

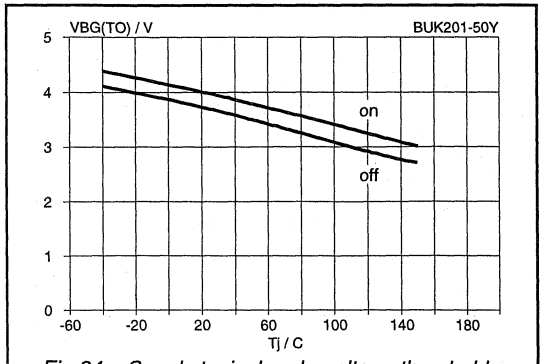


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 80\ mA$

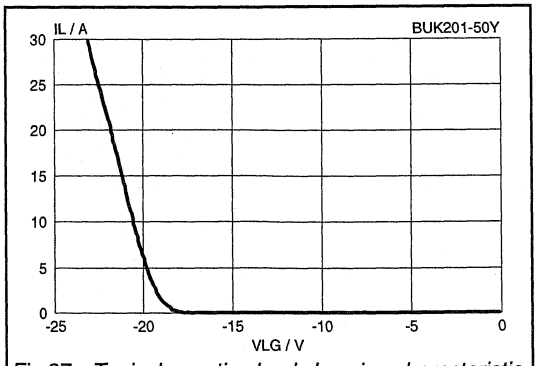


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

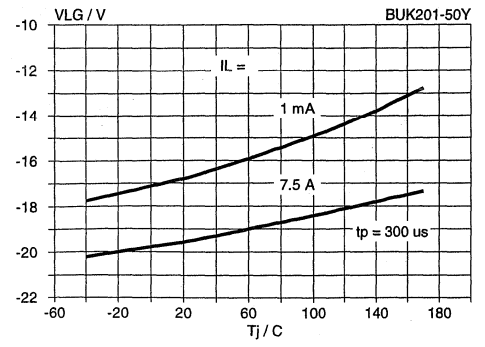


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

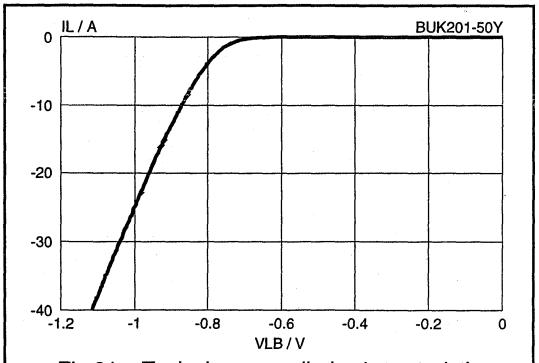


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

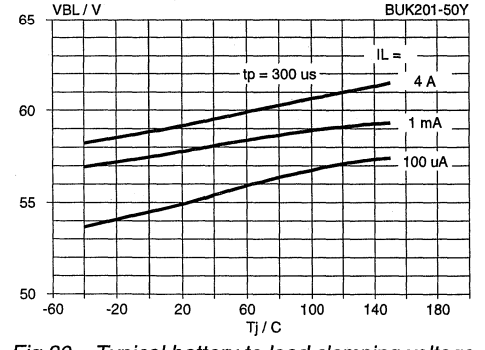


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

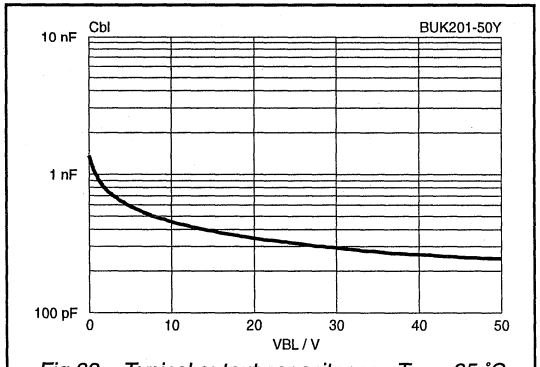


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

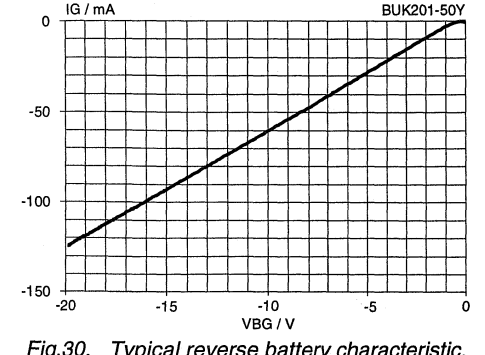


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

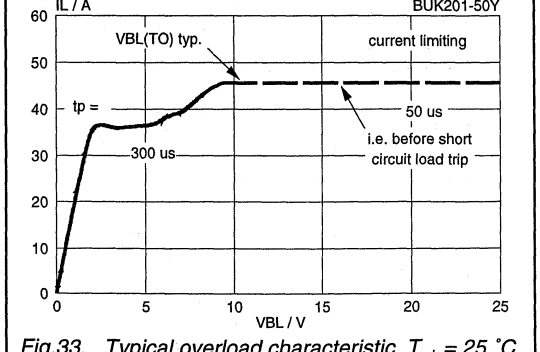


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

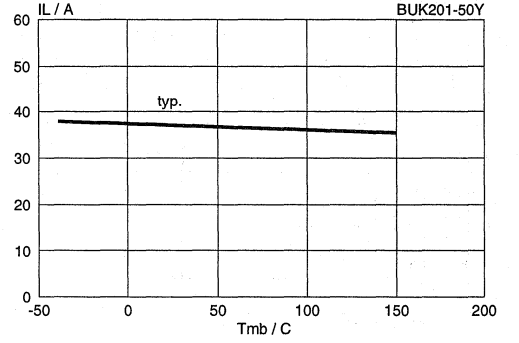


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

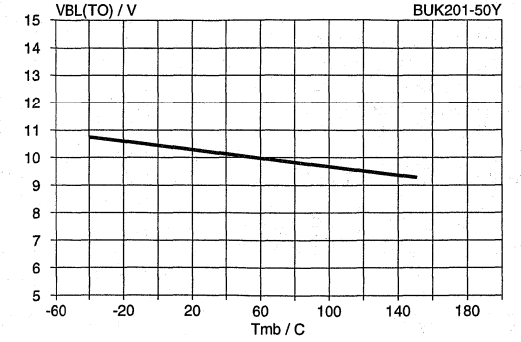


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

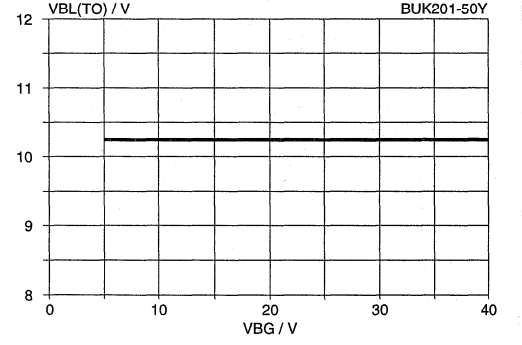


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

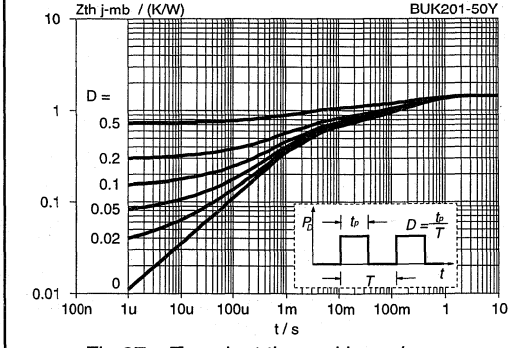


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK202-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FUNCTIONAL BLOCK DIAGRAM

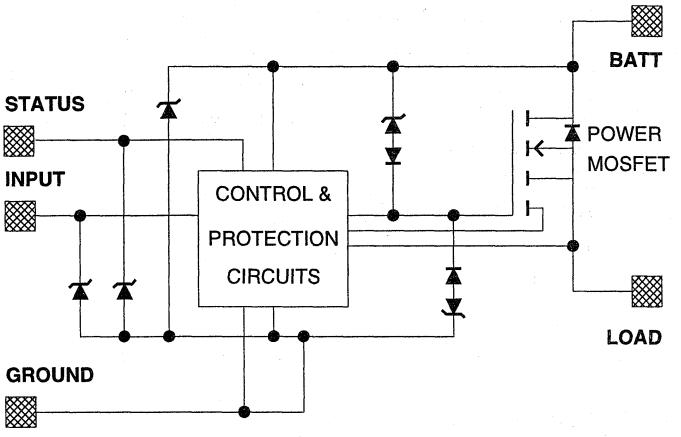


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

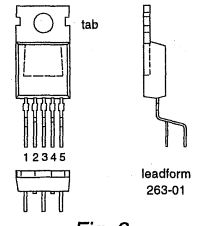


Fig. 2.

SYMBOL

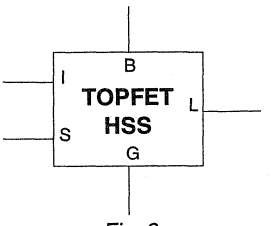


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external ground, input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	50	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	34	45	64	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

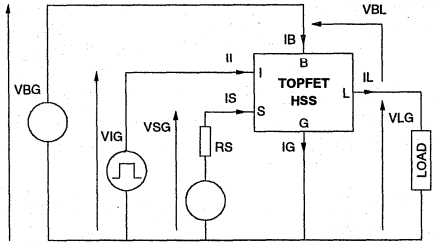


Fig.4. High side switch measurements schematic. (current and voltage conventions)

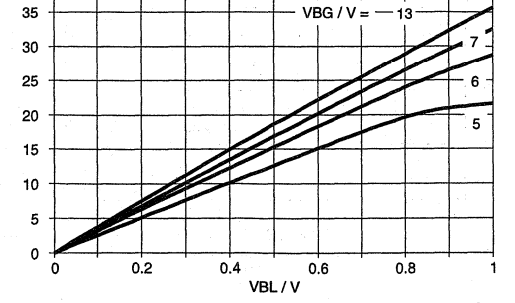


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

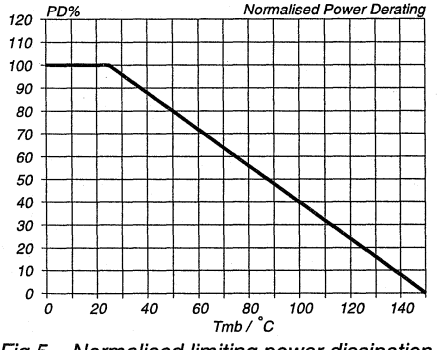


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

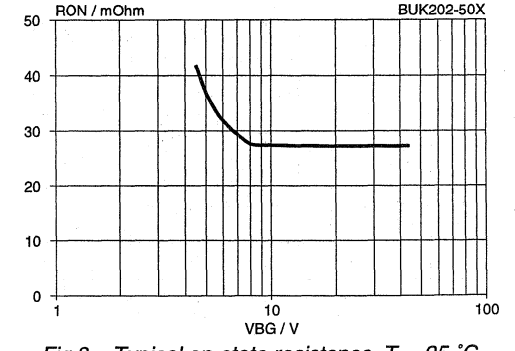


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

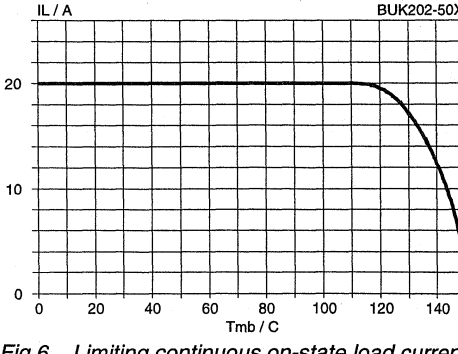


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

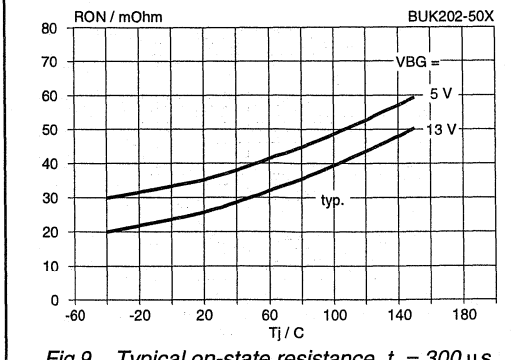


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

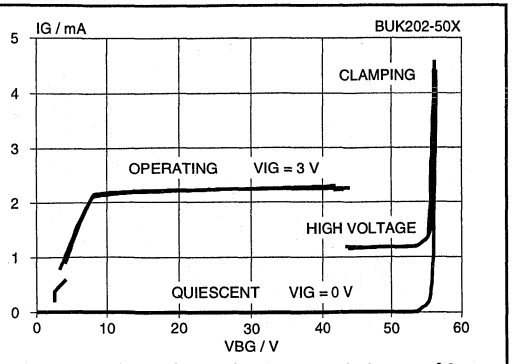


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

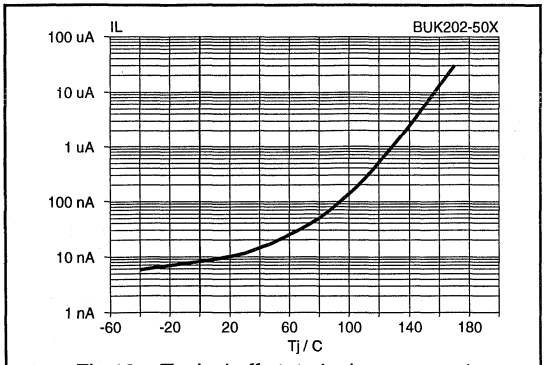


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

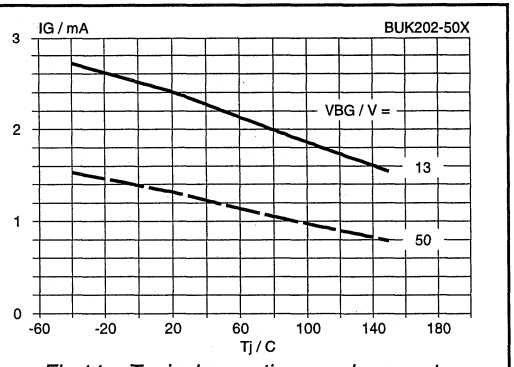


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

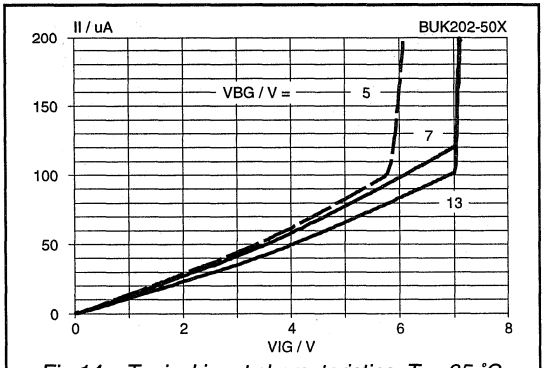


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

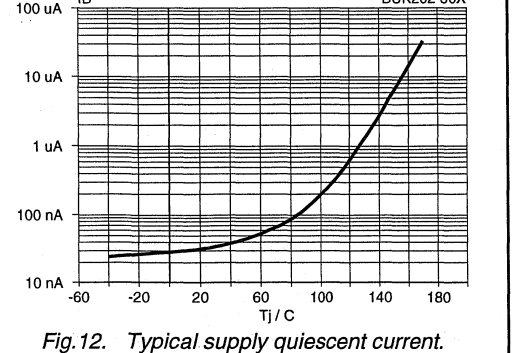


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

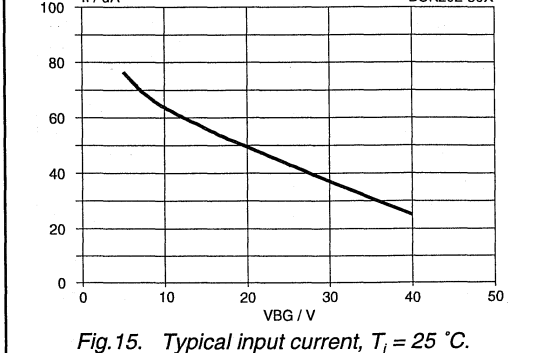


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

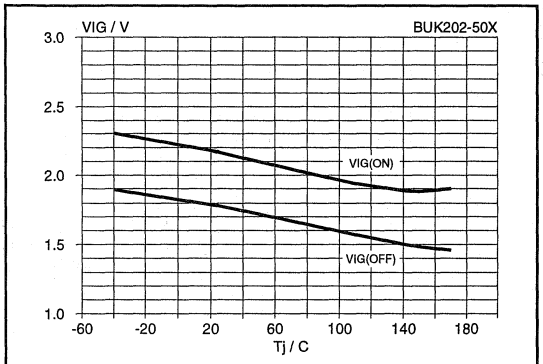


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

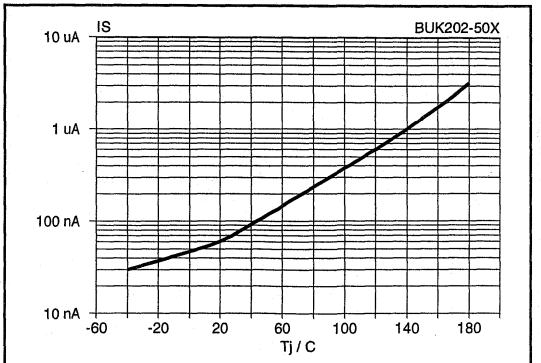


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

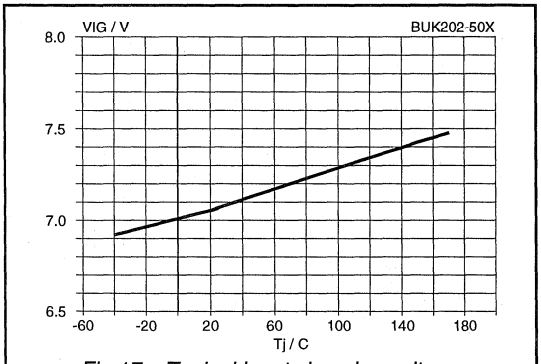


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

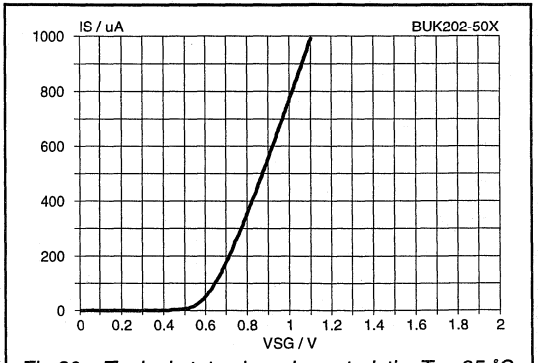


Fig.20. Typical status low characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

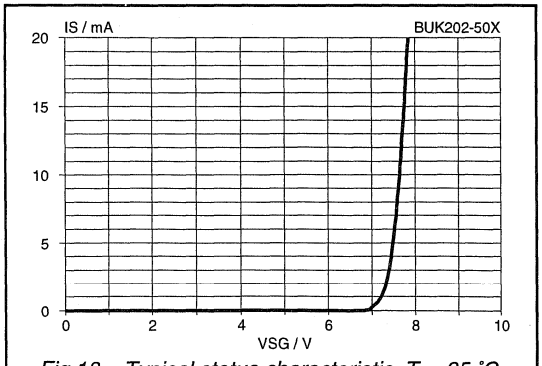


Fig.18. Typical status characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

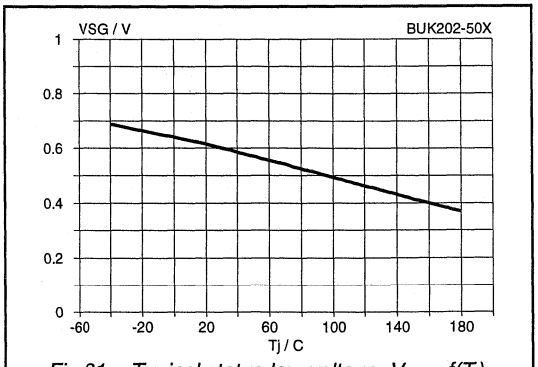


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

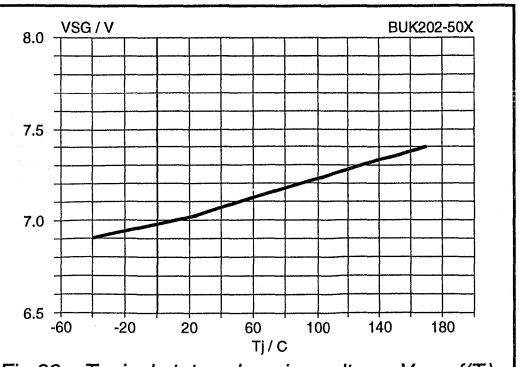


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

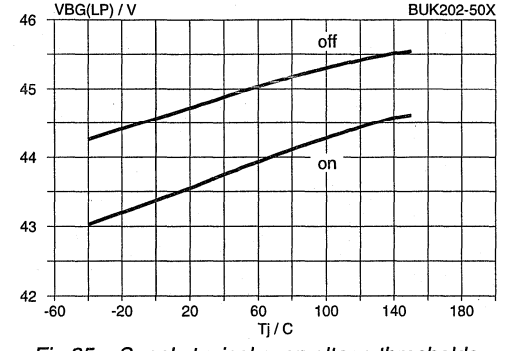


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

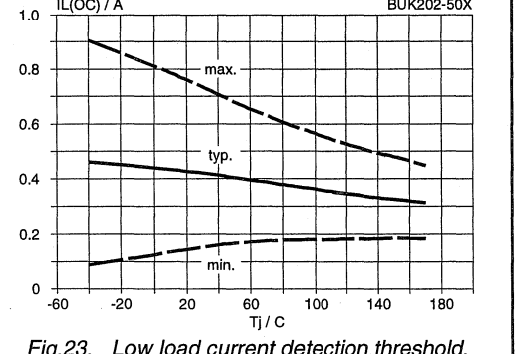


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

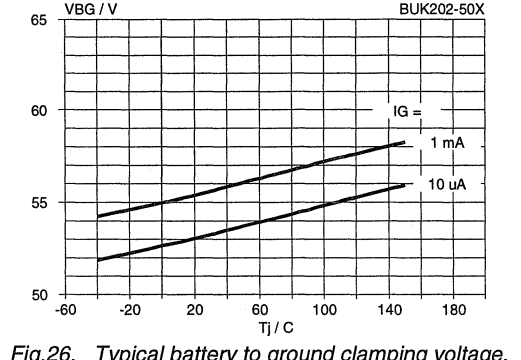


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

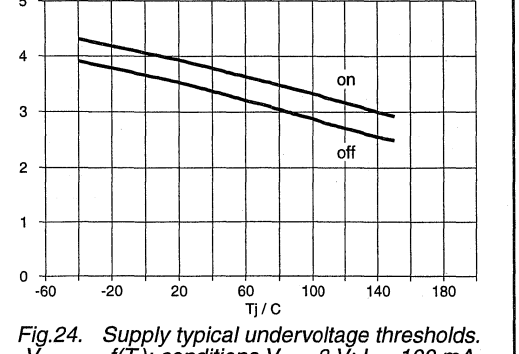


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

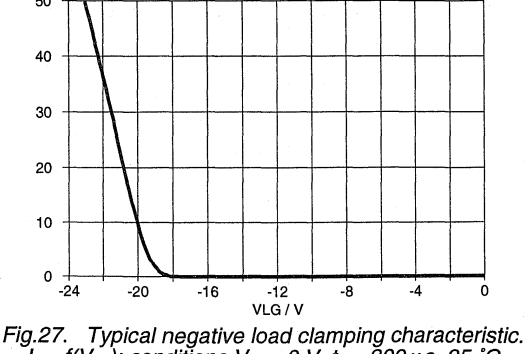


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

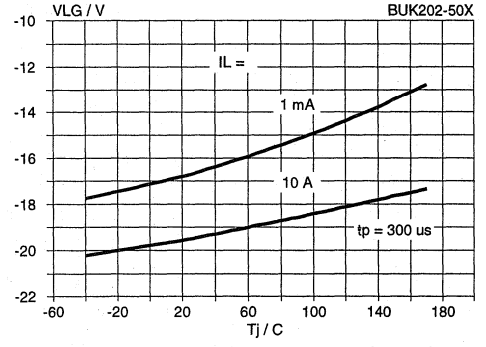


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

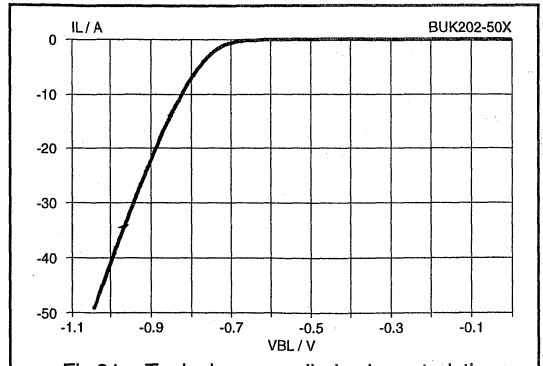


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

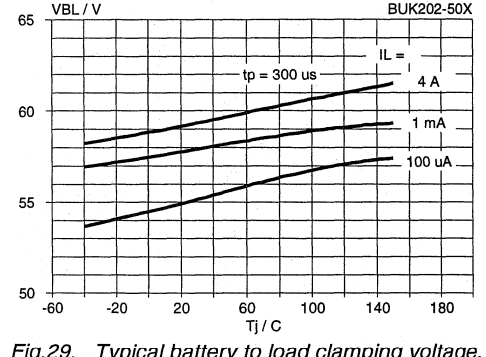


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

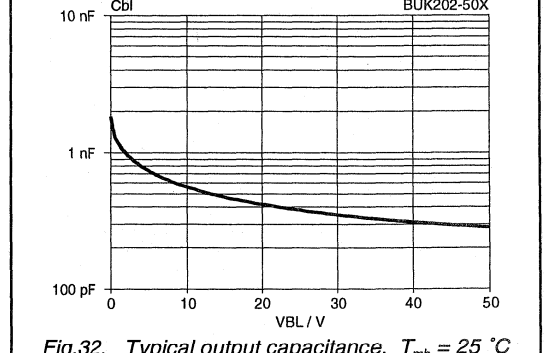


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

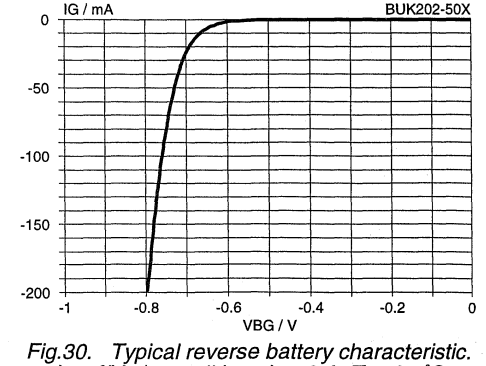


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

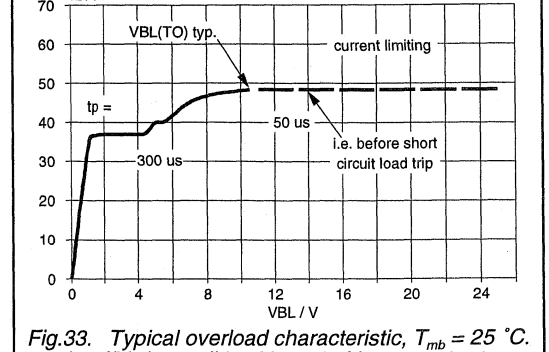


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

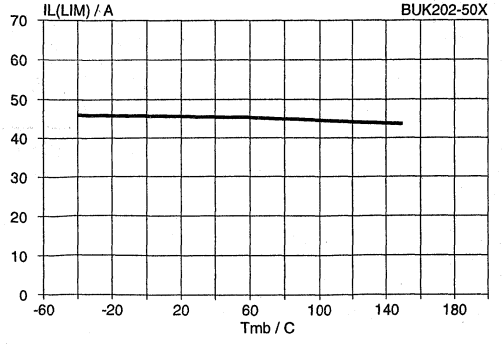


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

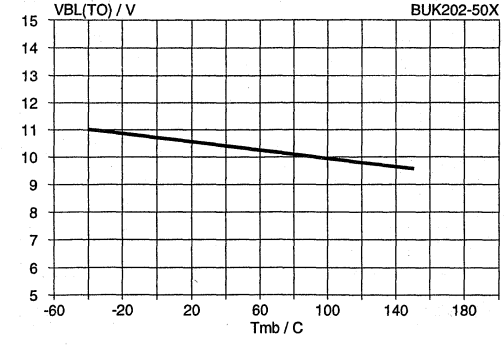


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

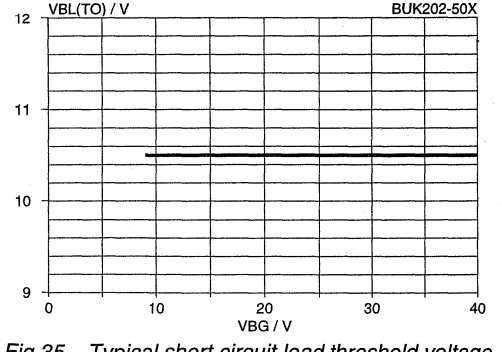


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 ˚C

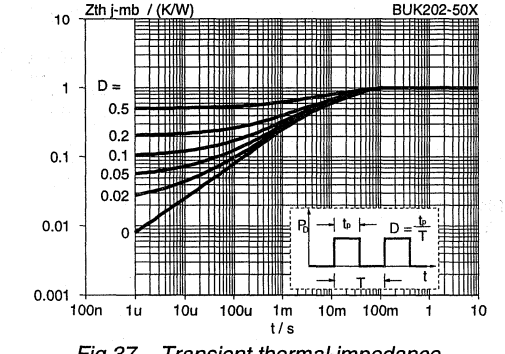


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK202-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

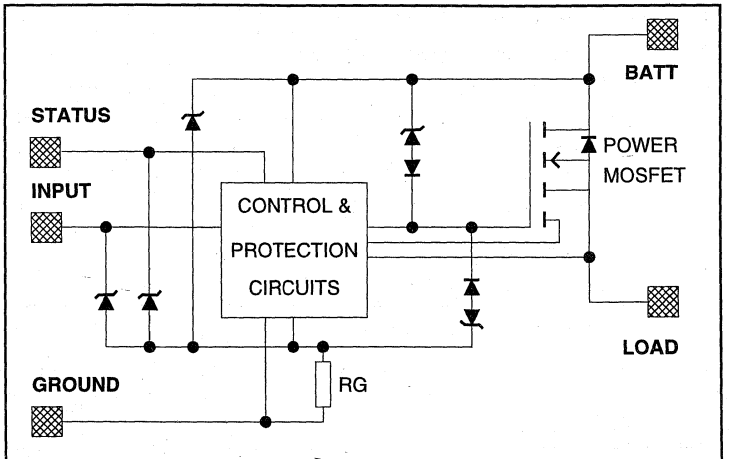


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

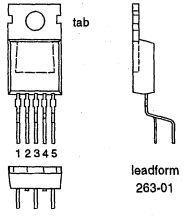


Fig. 2.

SYMBOL

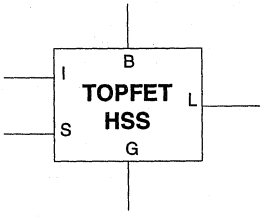


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the supply when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the supply with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	50	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	34	45	64	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

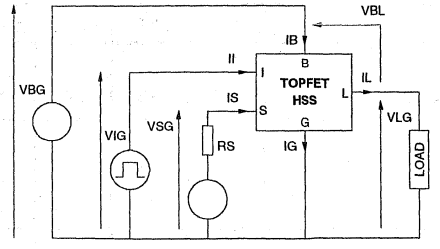


Fig.4. High side switch measurements schematic. (current and voltage conventions)

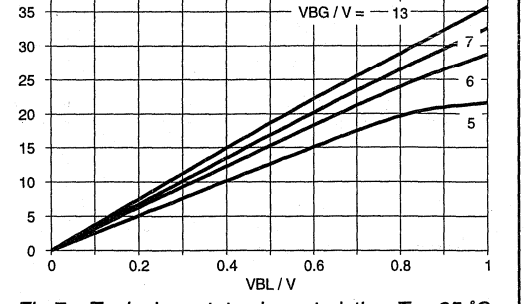


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

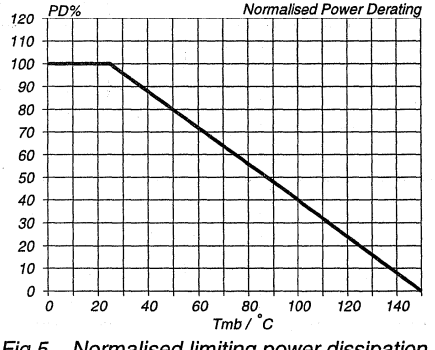


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

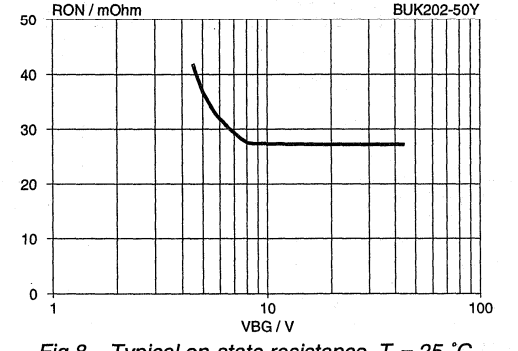


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

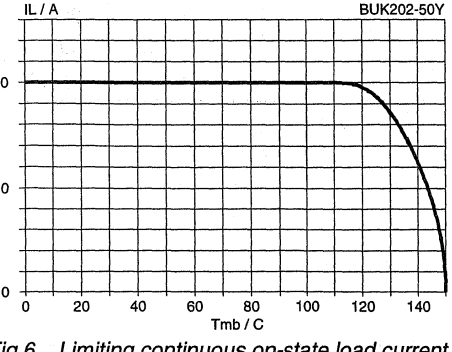


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

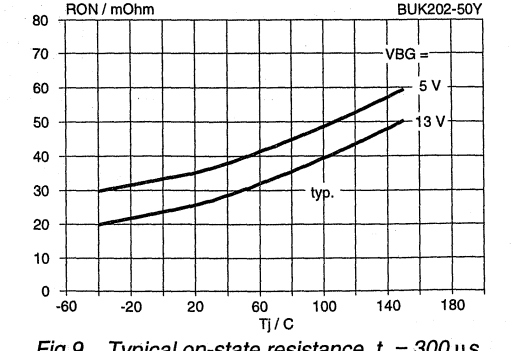


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

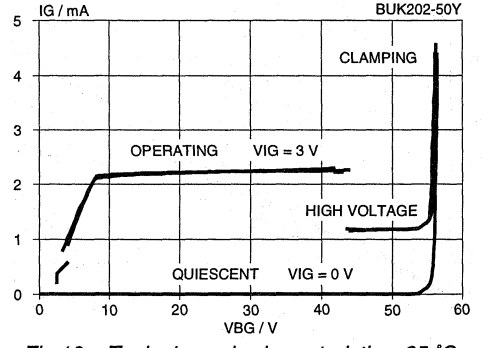


Fig.10. Typical supply characteristics, 25 °C. $I_G = f(V_{BG})$; parameter V_{IG}

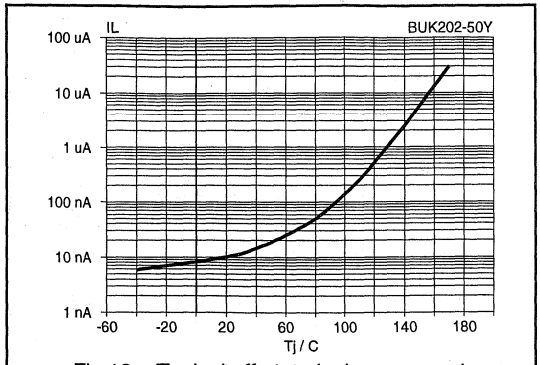


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

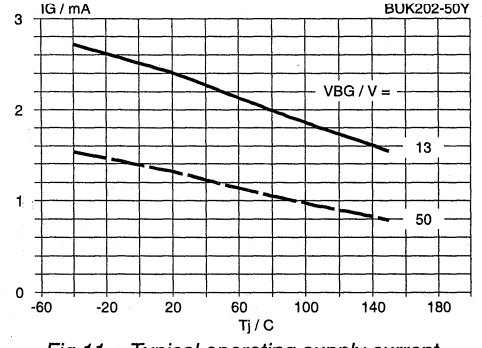


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

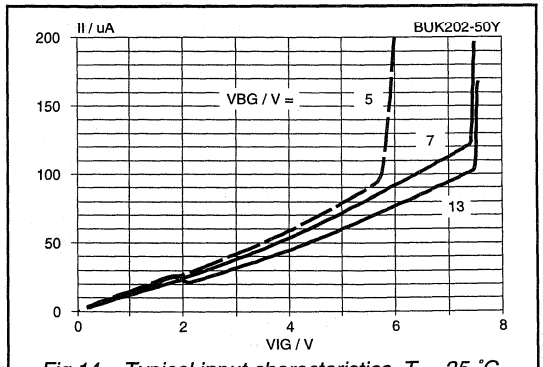


Fig.14. Typical input characteristics, T_j = 25 °C. $I_I = f(V_{IG})$; parameter V_{BG}

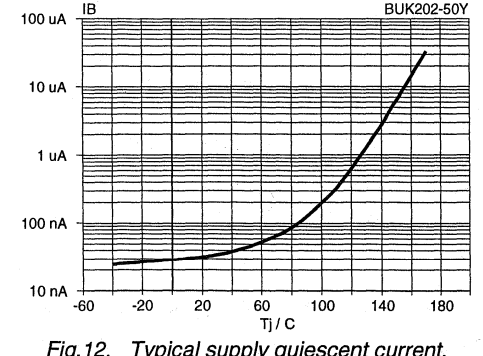


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

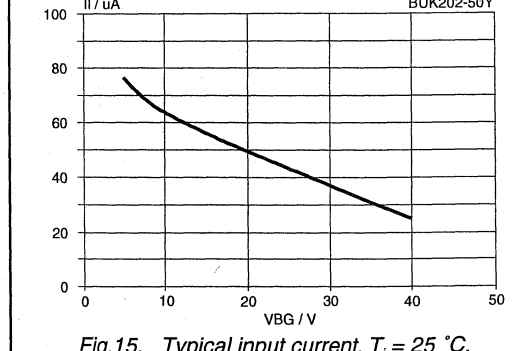


Fig.15. Typical input current, T_j = 25 °C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

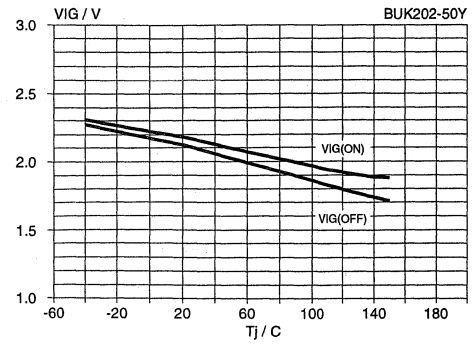


Fig.16. Typical input threshold voltages.
$V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

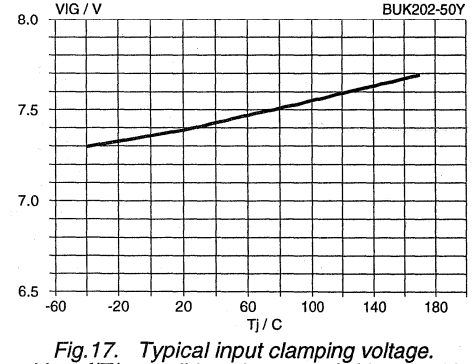


Fig.17. Typical input clamping voltage.
$V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

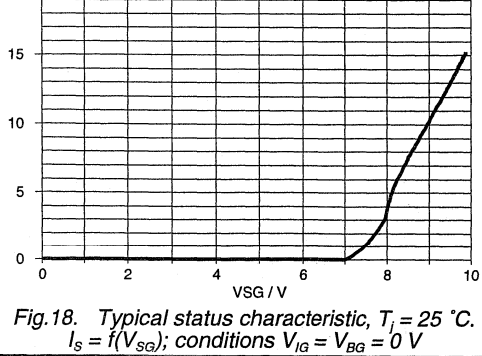


Fig.18. Typical status characteristic, T_j = 25 °C.
$I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

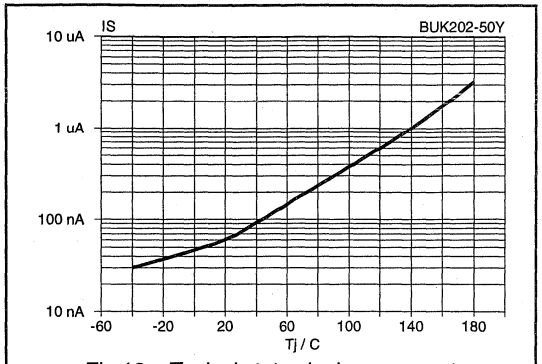


Fig.19. Typical status leakage current.
$I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

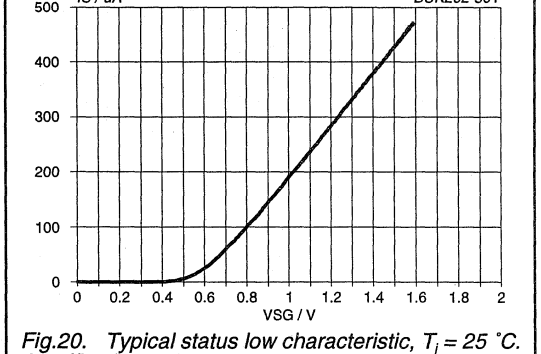


Fig.20. Typical status low characteristic, T_j = 25 °C.
$I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

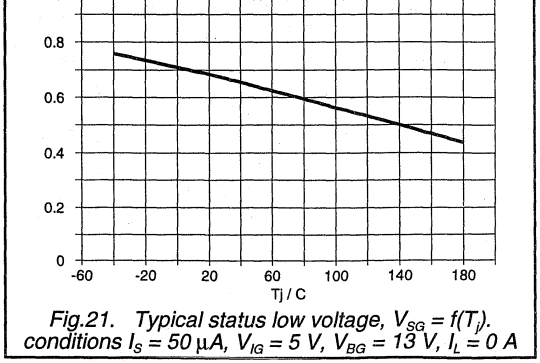


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$.
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

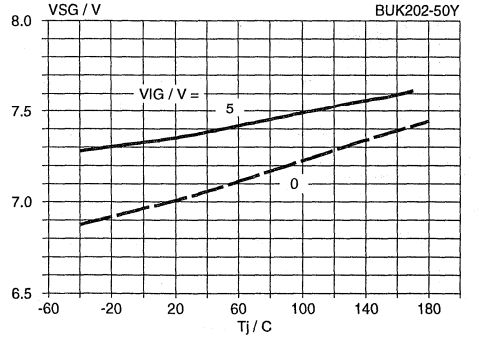


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

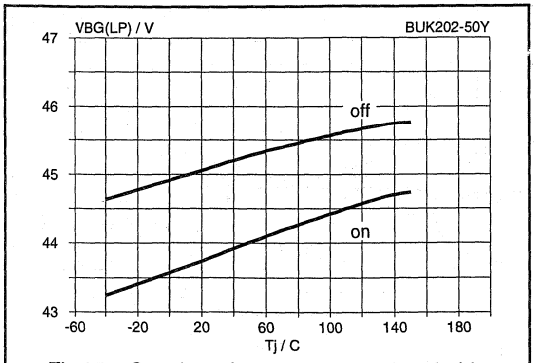


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

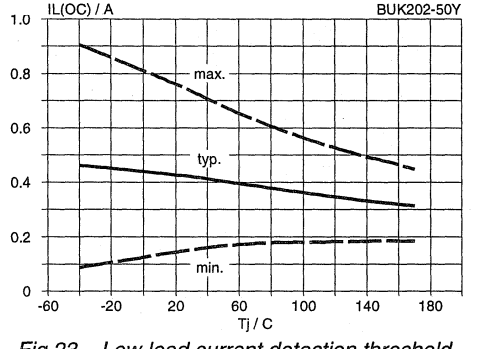


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

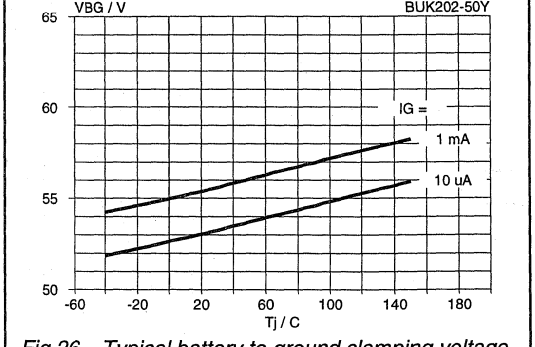


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

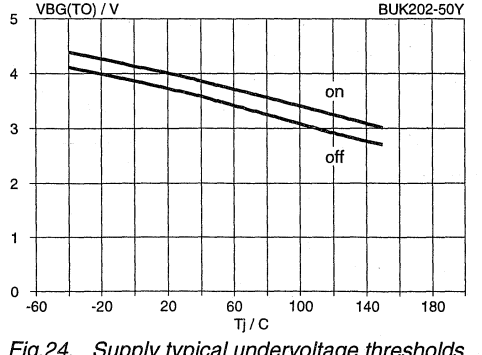


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

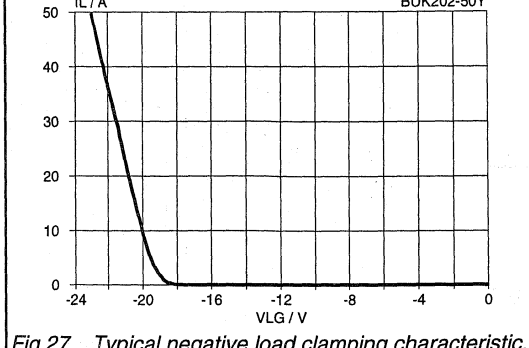


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

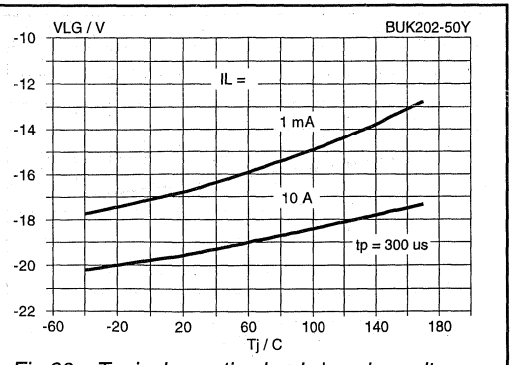


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

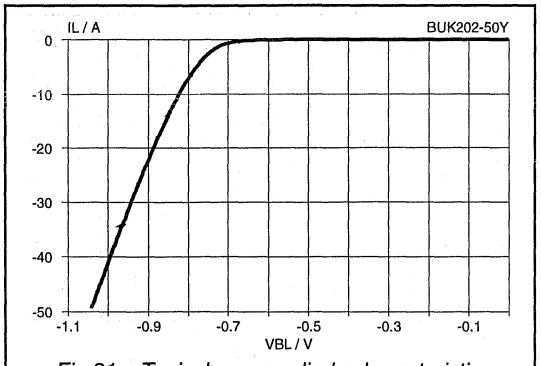


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

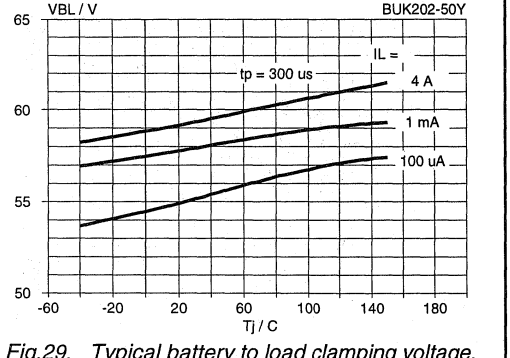


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

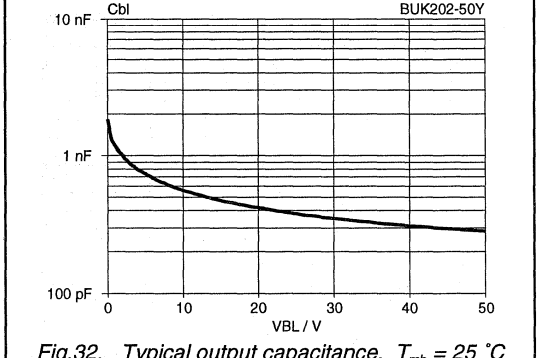


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

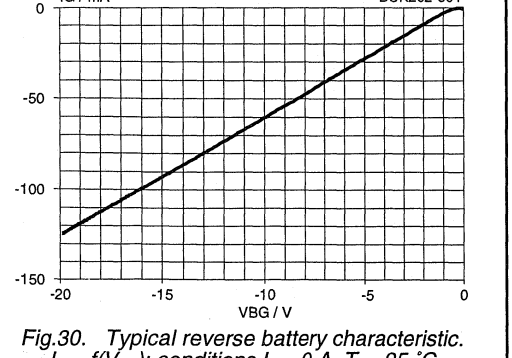


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

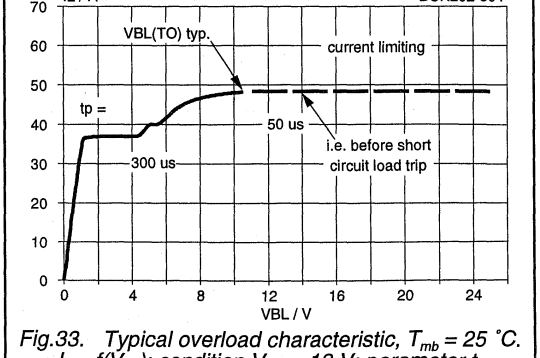


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

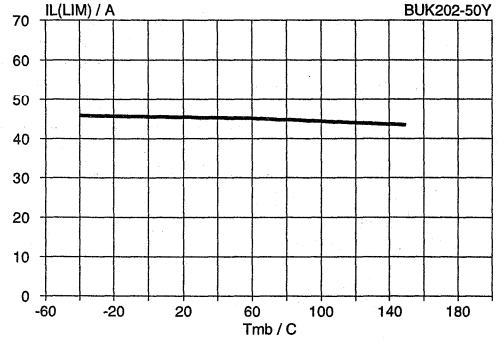


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

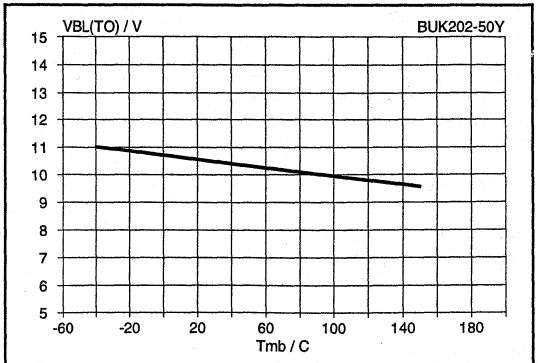


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

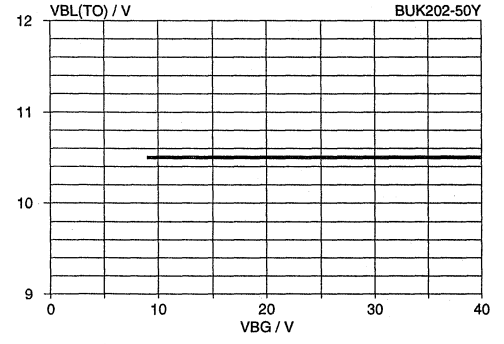


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

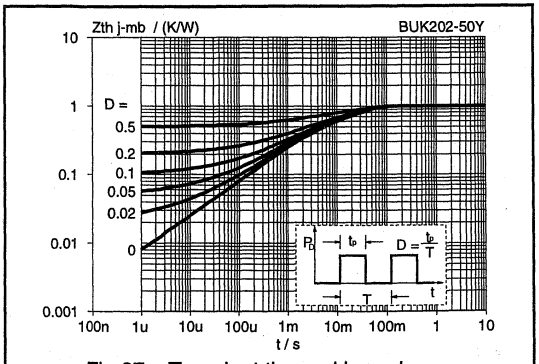


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK203-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

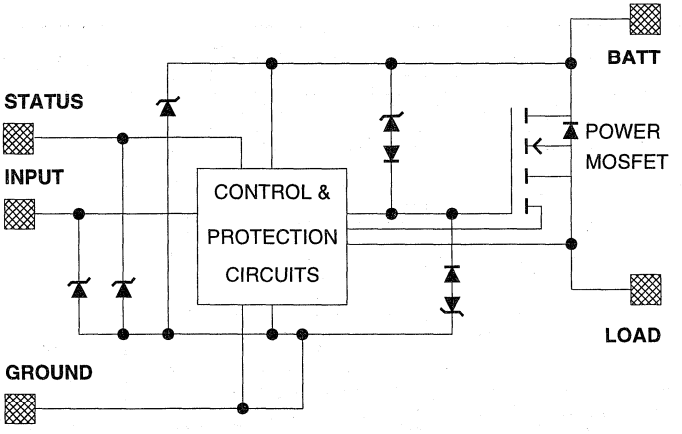


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

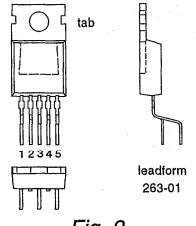


Fig. 2.

SYMBOL

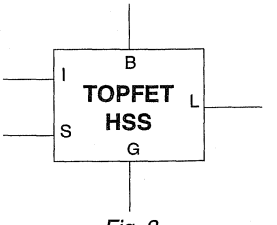


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	17	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	12	15	22	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

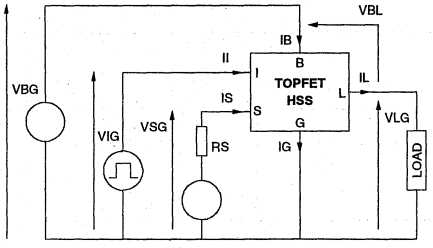


Fig.4. High side switch measurements schematic. (current and voltage conventions)

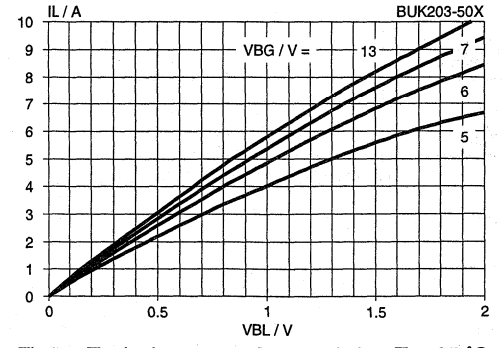


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

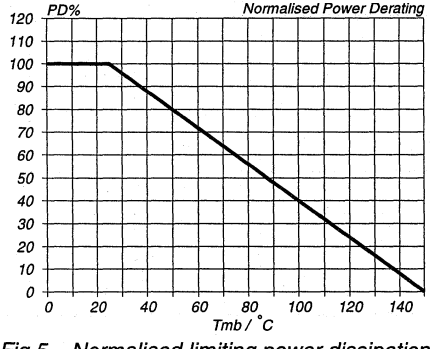


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

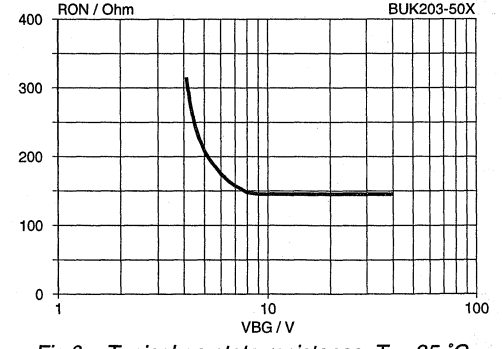


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

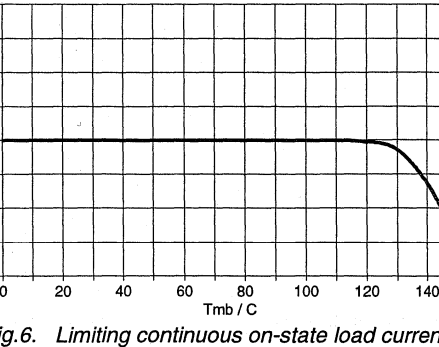


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

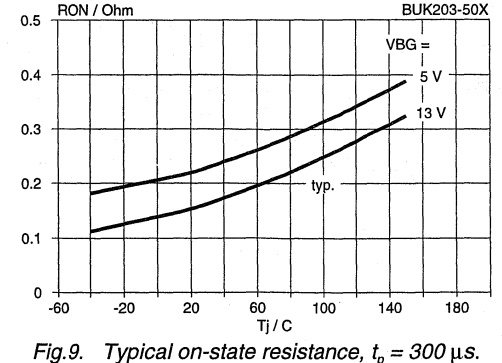


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

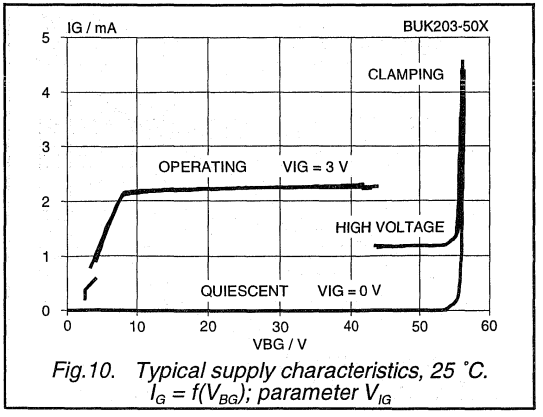


Fig.10. Typical supply characteristics, 25 °C.
$I_G = f(V_{BG})$; parameter V_{IG}

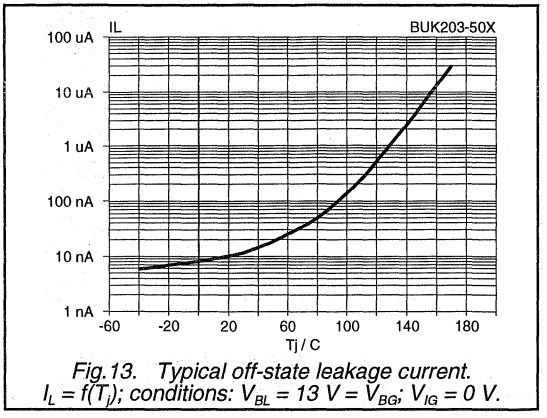


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

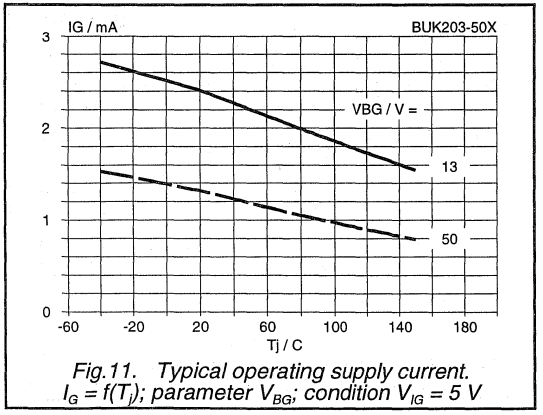


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

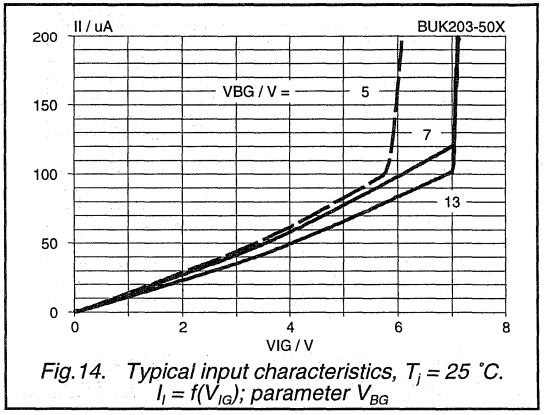


Fig.14. Typical input characteristics, T_j = 25 °C.
$I_I = f(V_{IG})$; parameter V_{BG}

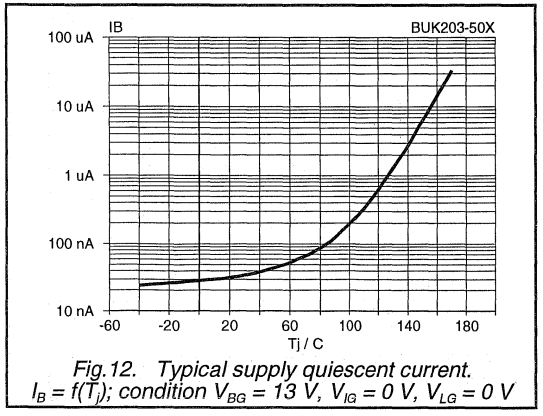


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

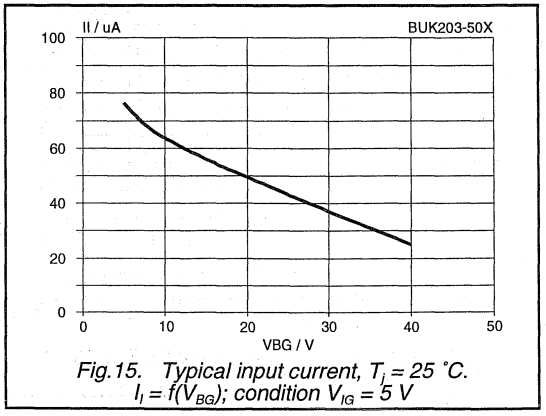


Fig.15. Typical input current, T_j = 25 °C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

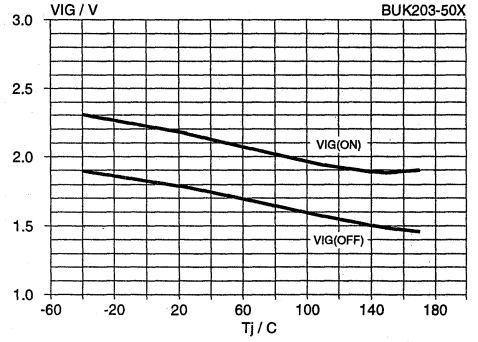


Fig.16. Typical input threshold voltages.
V_{IG} = f(T_j); conditions V_{BG} = 13 V, I_L = 100 mA

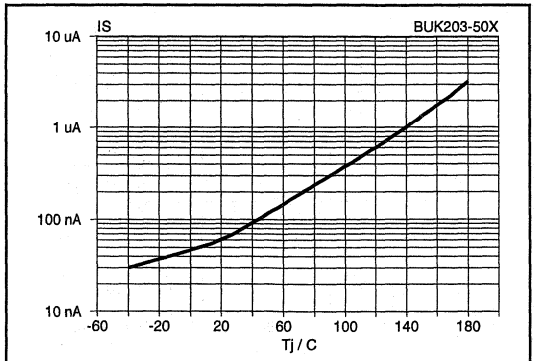


Fig.19. Typical status leakage current.
I_S = f(T_j); conditions V_{SG} = 5 V, V_{IG} = V_{BG} = 0 V

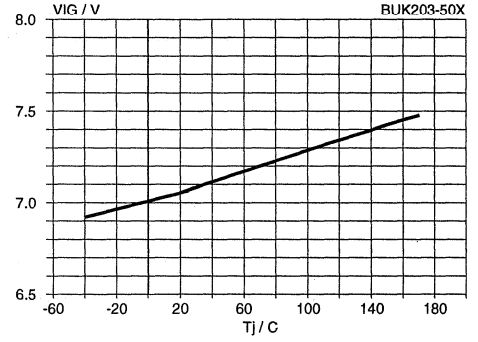


Fig.17. Typical input clamping voltage.
V_{IG} = f(T_j); conditions I_I = 200 µA, V_{BG} = 13 V

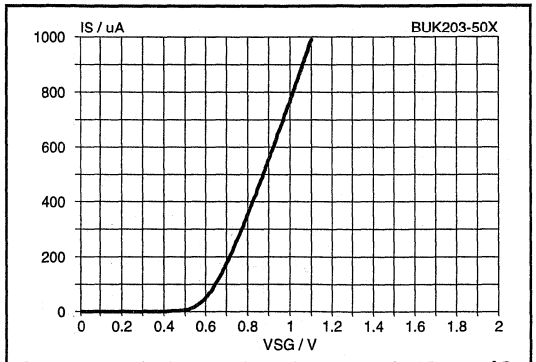


Fig.20. Typical status low characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

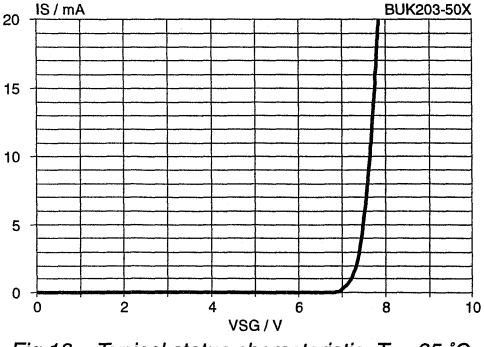


Fig.18. Typical status characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = V_{BG} = 0 V

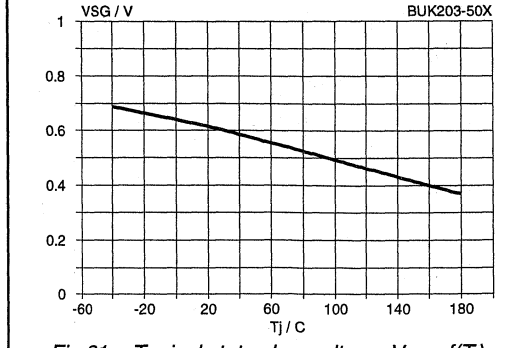


Fig.21. Typical status low voltage, V_{SG} = f(T_j).
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

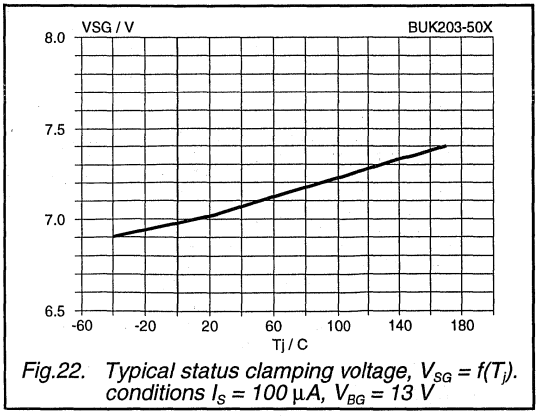


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

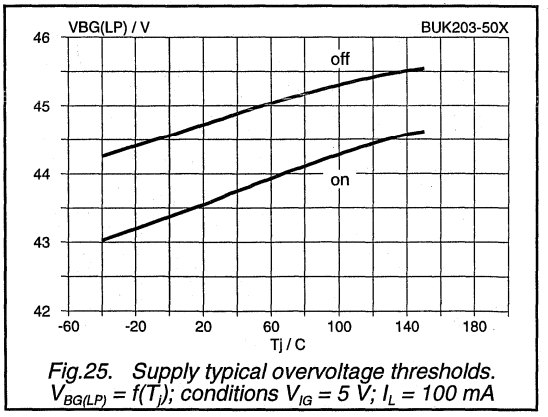


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

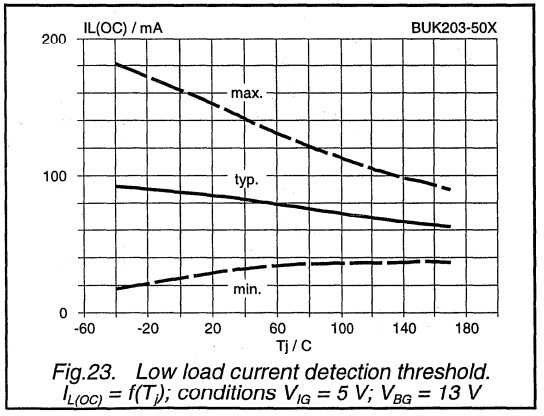


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

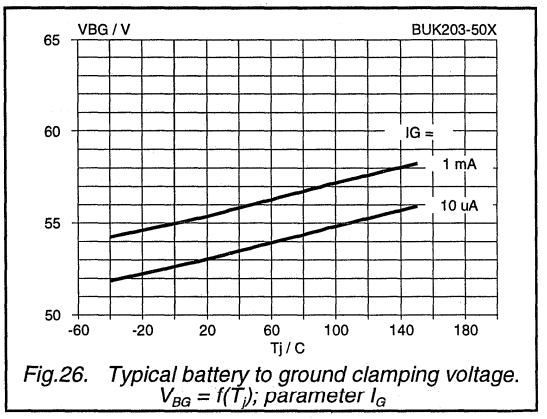


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

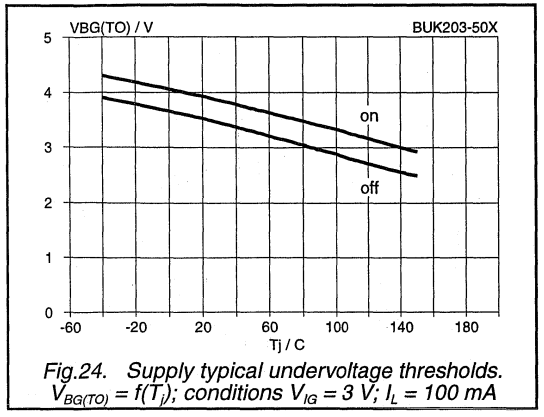


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

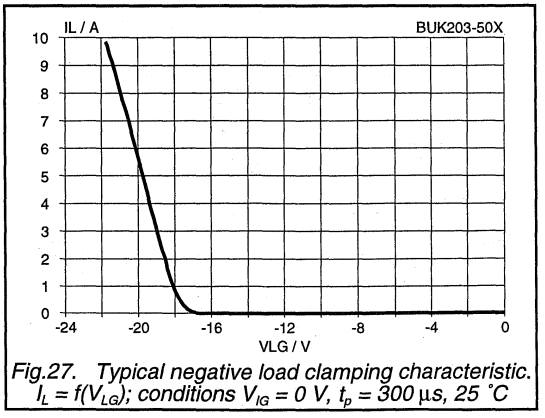


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

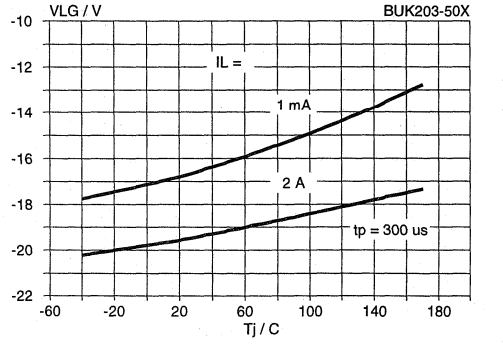


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

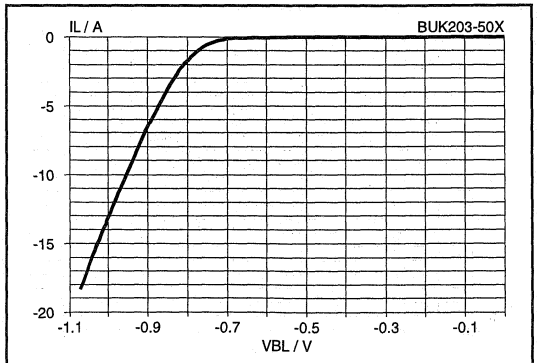


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

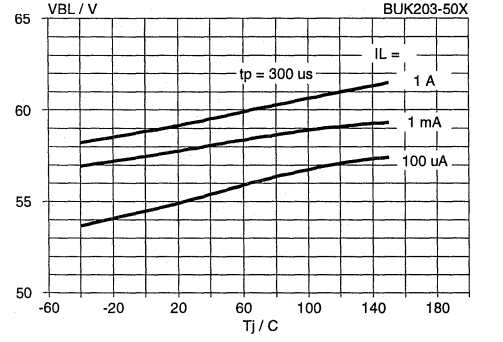


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

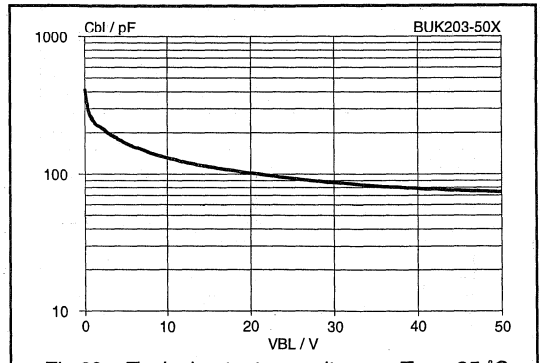


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

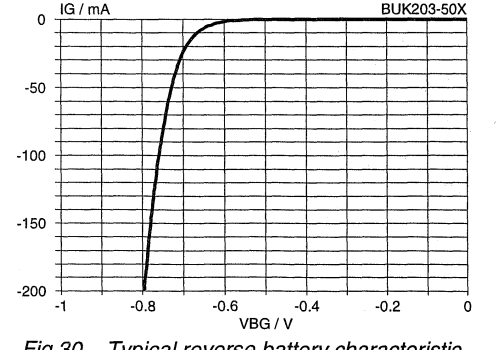


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

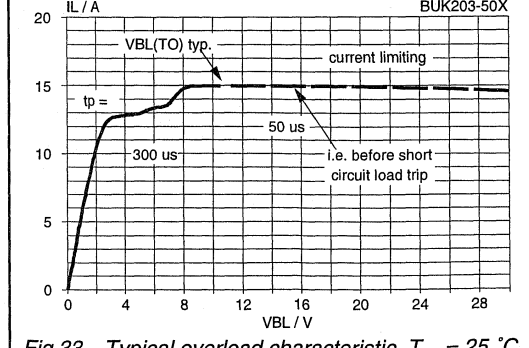


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

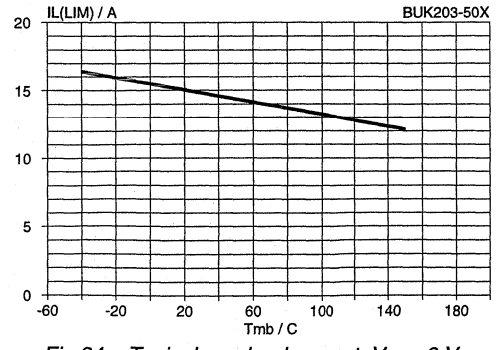


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

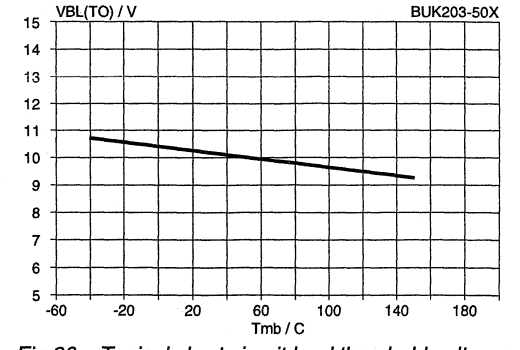


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

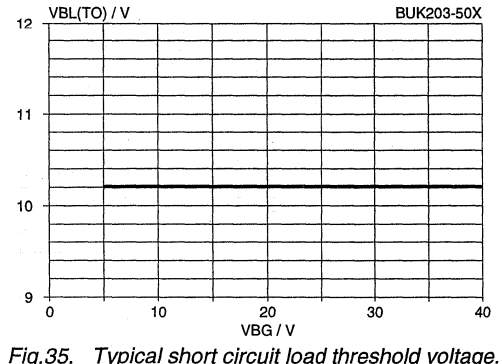


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

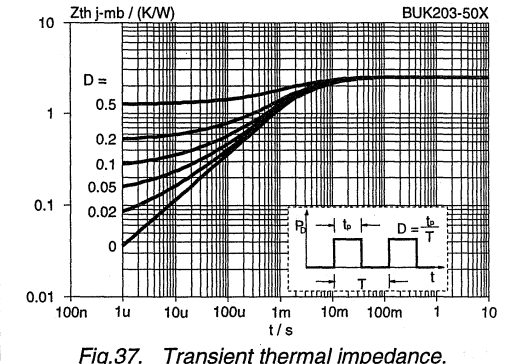


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

PowerMOS transistor TOPFET high side switch

BUK203-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

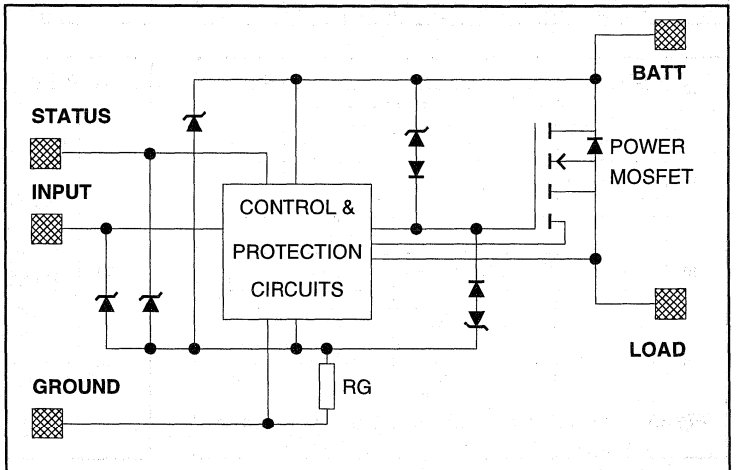


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT263

PIN	DESCRIPTION
1	Ground
2	Input
3	Battery (+ve supply)
4	Status
5	Load
tab	connected to pin 3

PIN CONFIGURATION

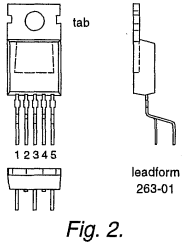


Fig. 2.

SYMBOL

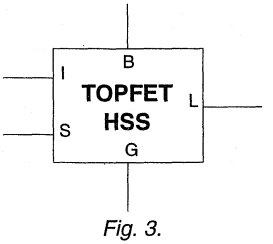


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	-	60	75	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	17	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	12	15	22	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

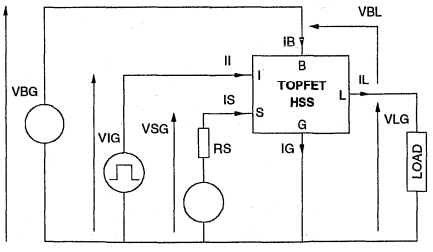


Fig.4. High side switch measurements schematic. (current and voltage conventions)

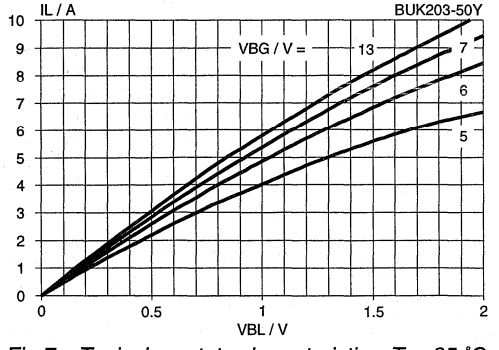


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

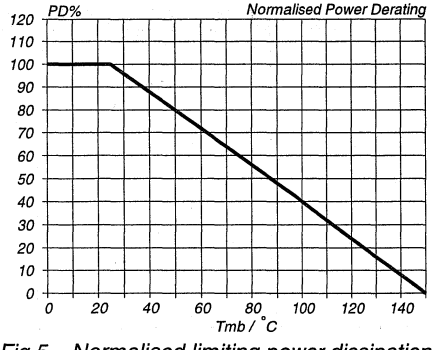


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

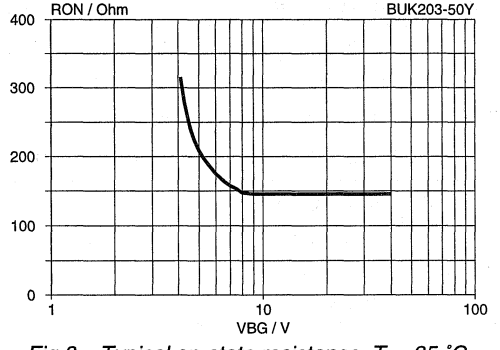


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

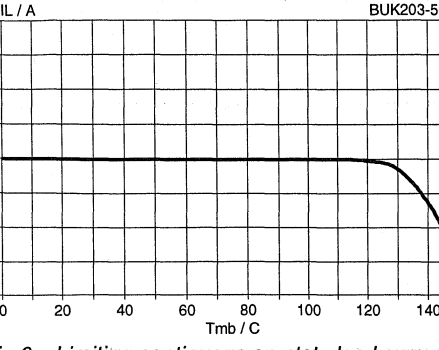


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

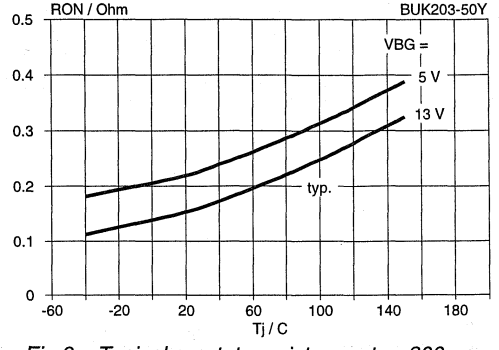


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

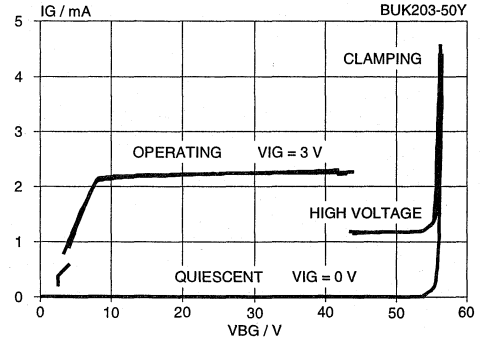


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

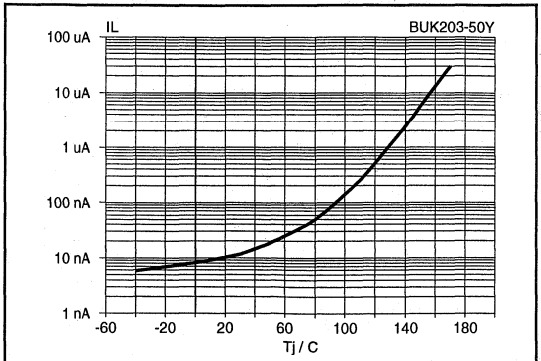


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

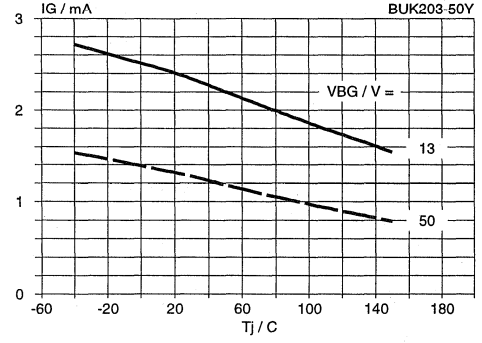


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

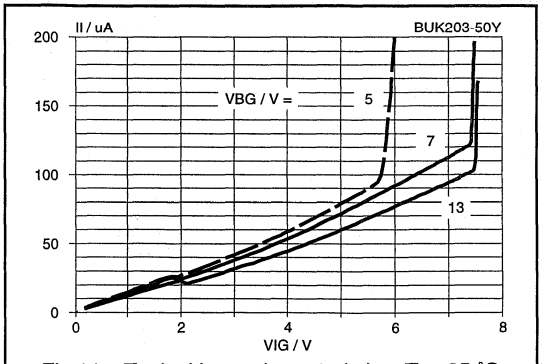


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

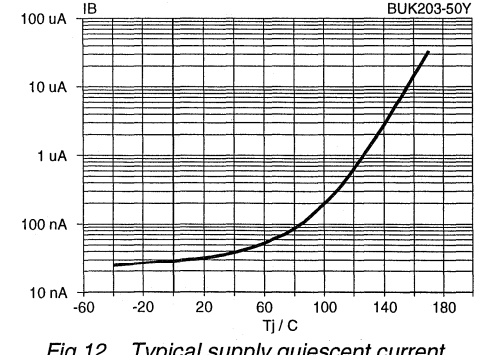


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

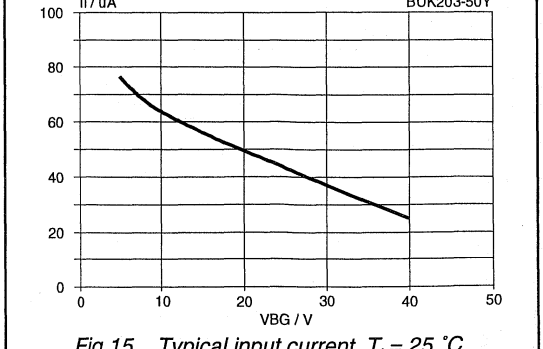


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

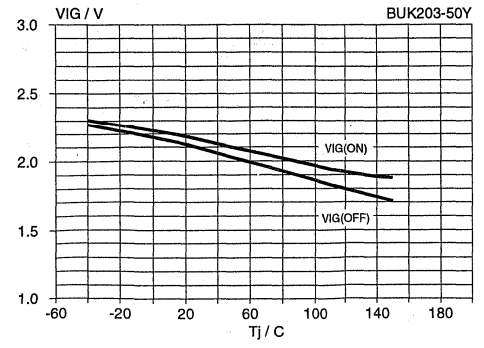


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

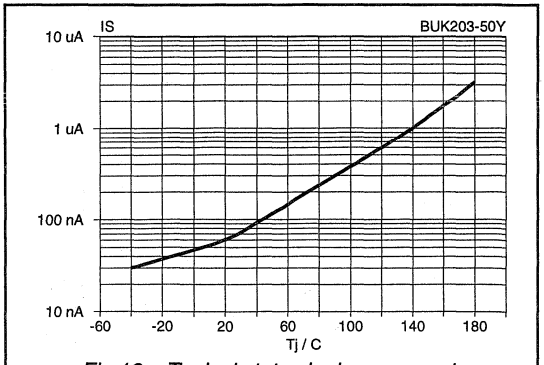


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

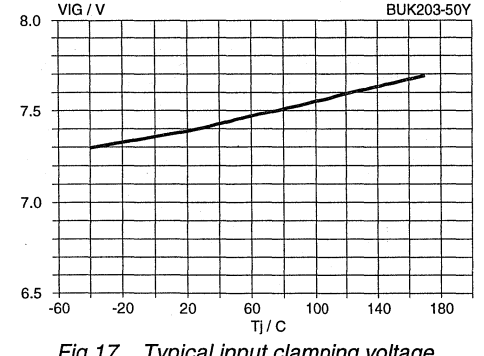


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

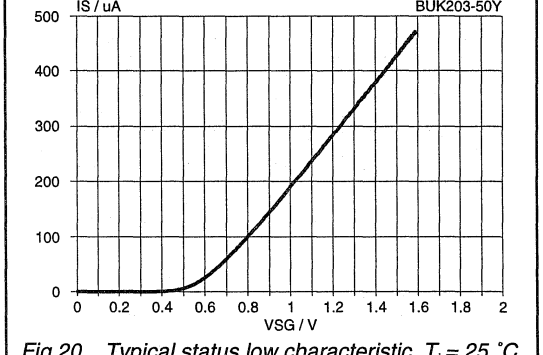


Fig.20. Typical status low characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

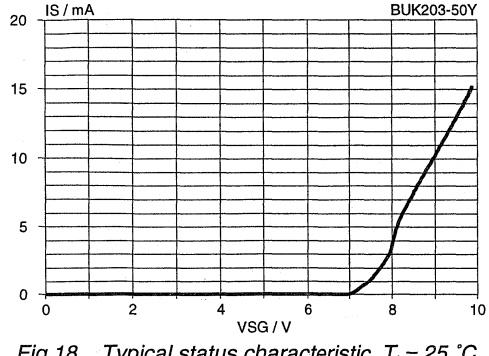


Fig.18. Typical status characteristic, T_j = 25 °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

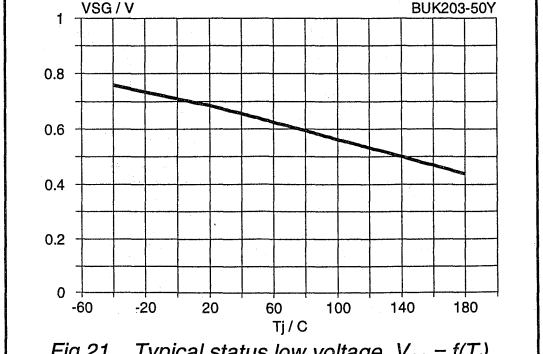


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

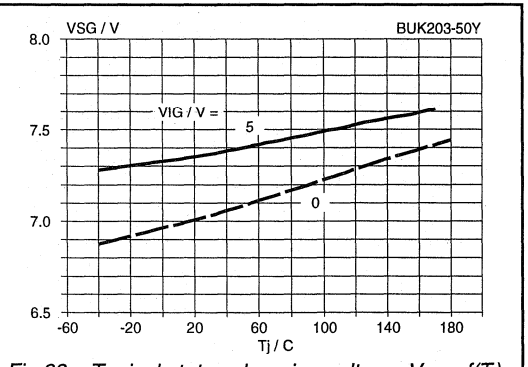


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

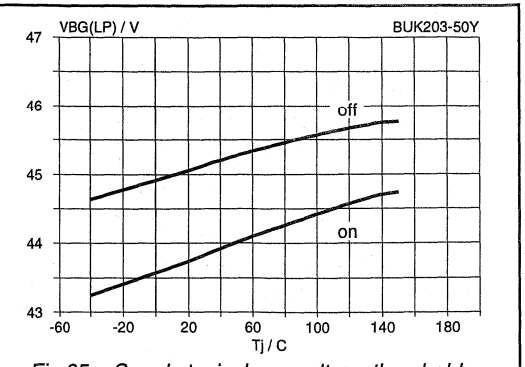


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

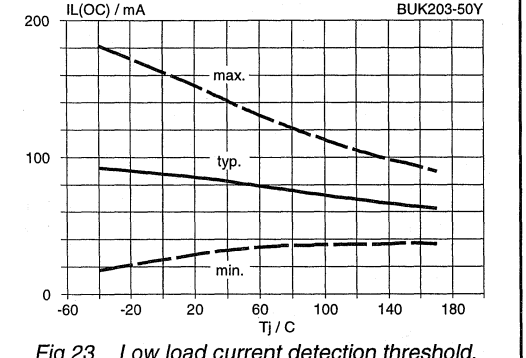


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

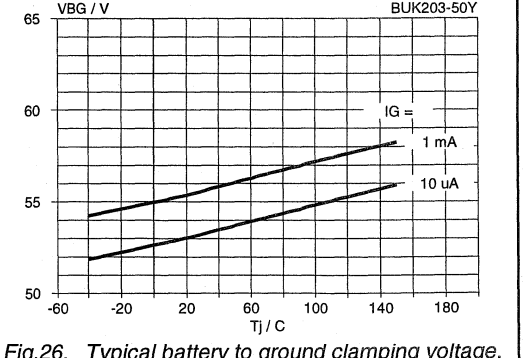


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

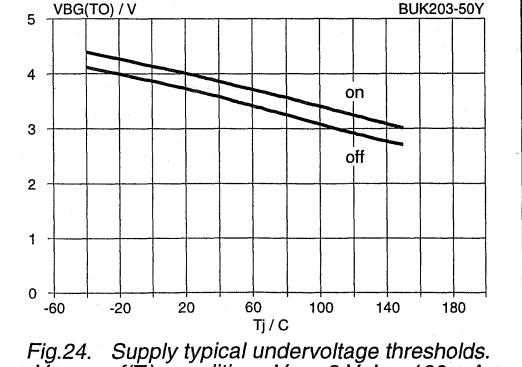


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

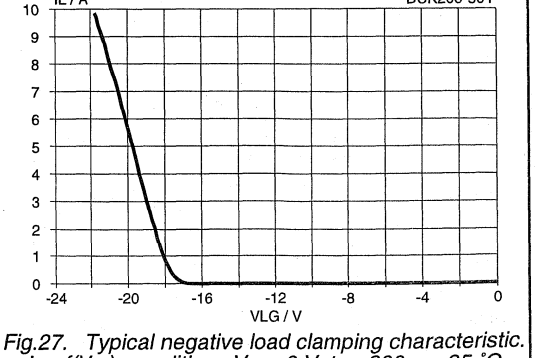


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

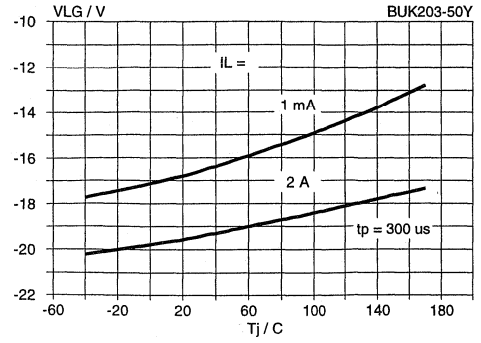


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

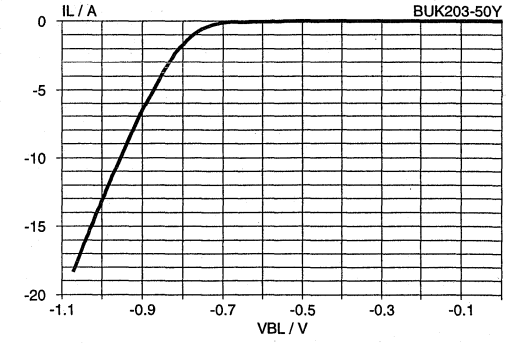


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

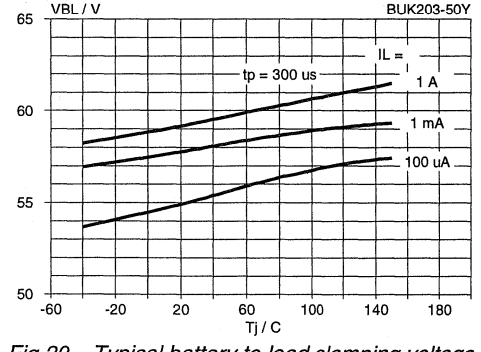


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

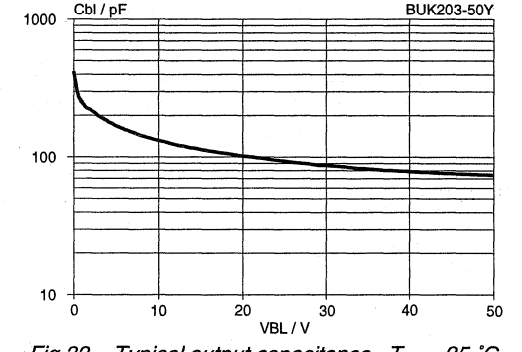


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

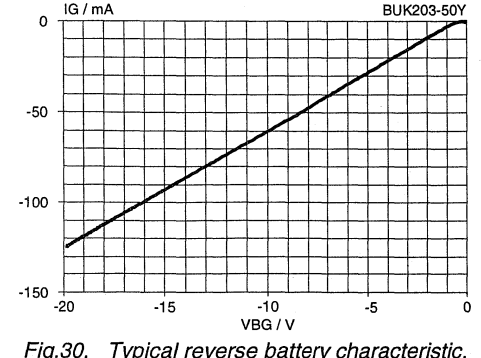


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

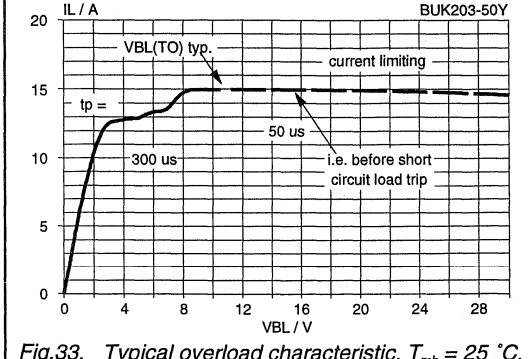


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

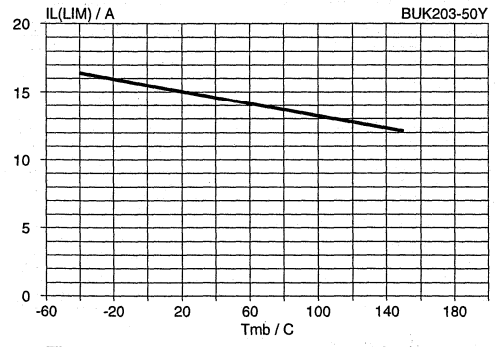


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

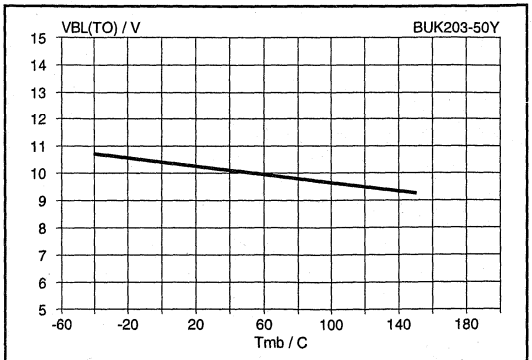


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

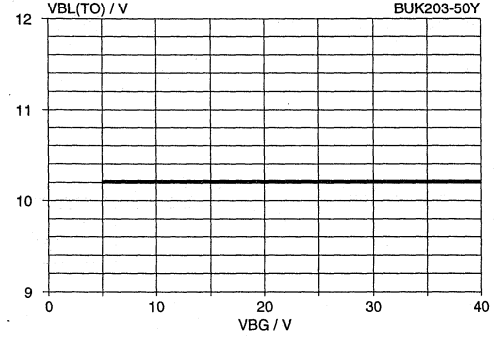


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

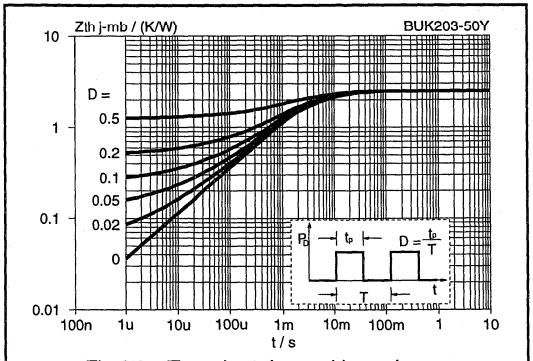


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch
SMD version of BUK200-50X

BUK204-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	3.5	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	10	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	100	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

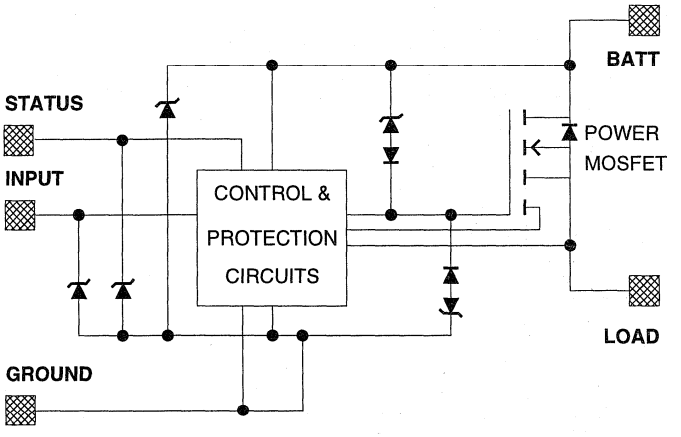


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

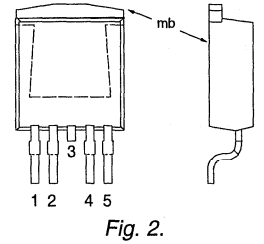


Fig. 2.

SYMBOL

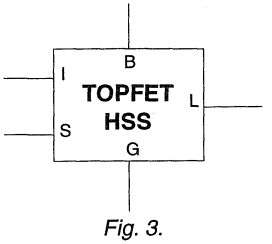


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115$ °C	-	10	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	62.5	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	T_{mb} = 150 °C prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.5	2	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	3.5	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 5 A; t_p = 300 µs	-	77	100	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1 A; t_p = 300 µs	-	116	150	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	50	200	350	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	8.5	10.3	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 80 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	35	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 8.5 V; t_p = 300 µs	23	33	43	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	330	460	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

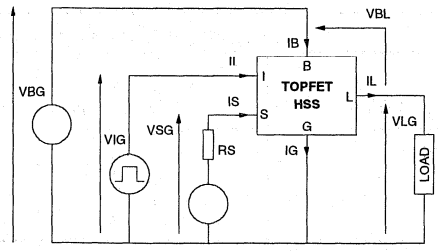


Fig.4. High side switch measurements schematic. (current and voltage conventions)

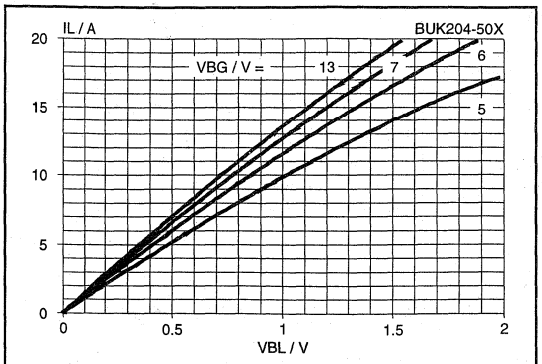


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

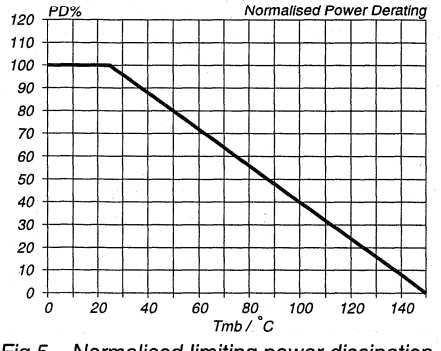


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

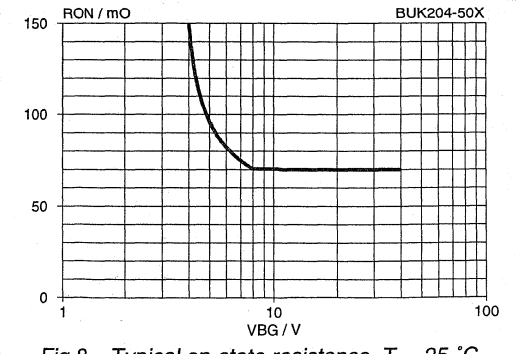


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 5 A; t_p = 300 µs

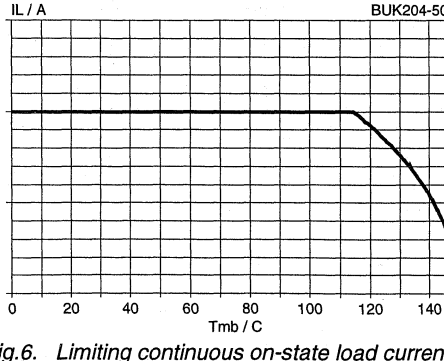


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

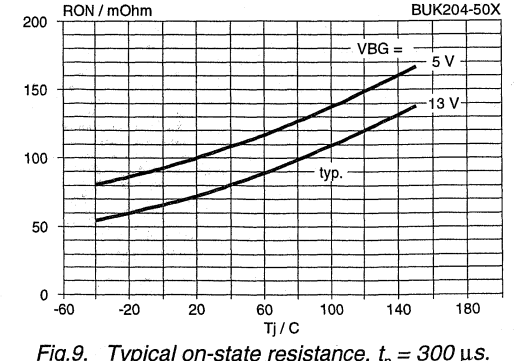


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1 A

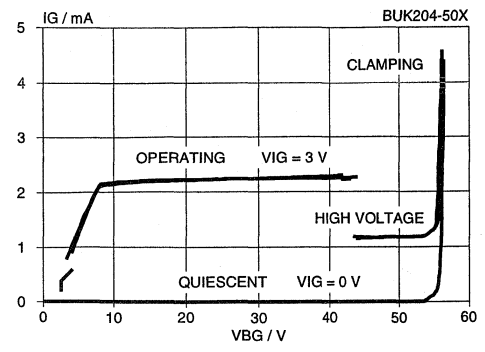


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

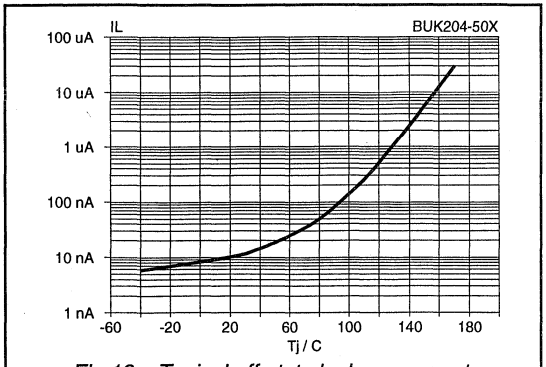


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

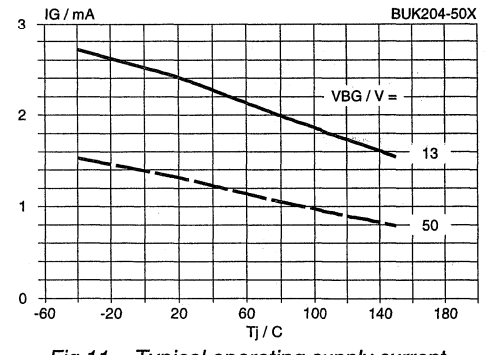


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

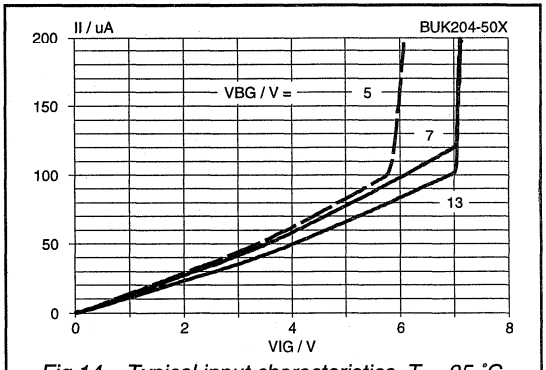


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

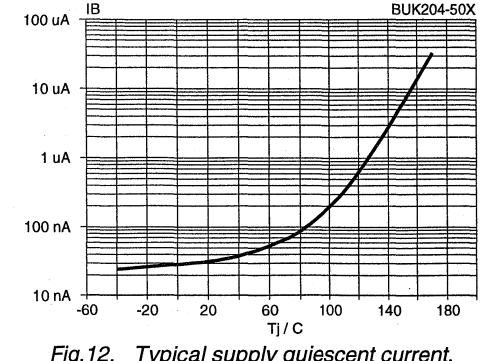


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

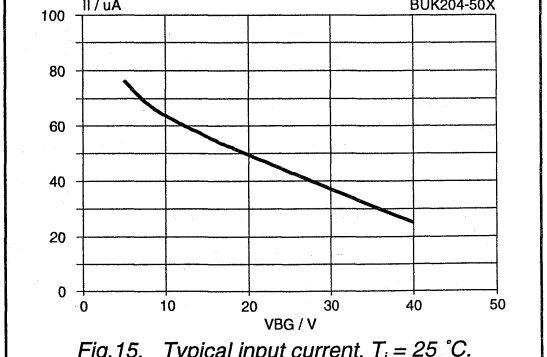


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

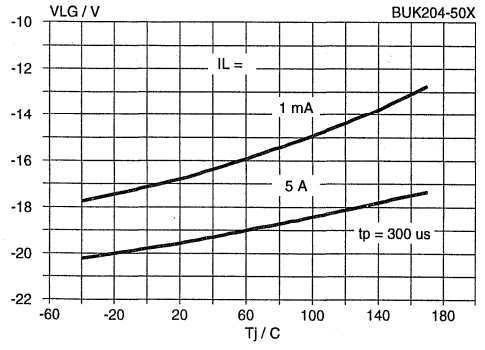


Fig.16. Typical input threshold voltages.
V_{IG} = f(T_j); conditions V_{BG} = 13 V, I_L = 50 mA

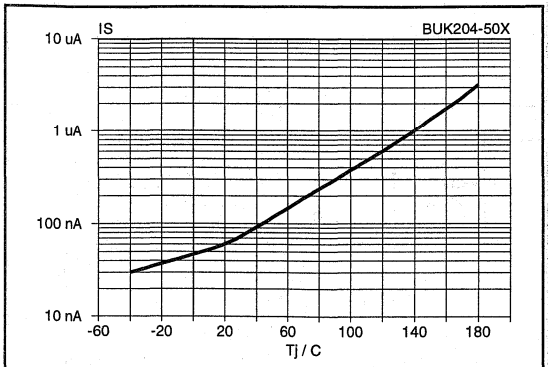


Fig.19. Typical status leakage current.
I_S = f(T_j); conditions V_{SG} = 5 V, V_{IG} = V_{BG} = 0 V

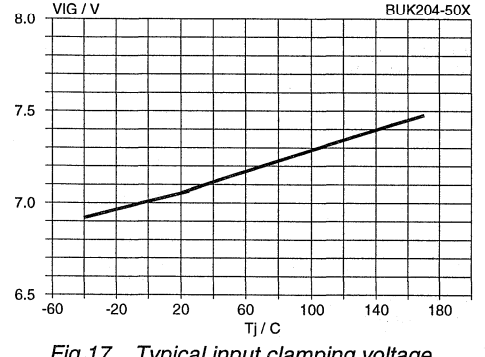


Fig.17. Typical input clamping voltage.
V_{IG} = f(T_j); conditions I_I = 200 µA, V_{BG} = 13 V

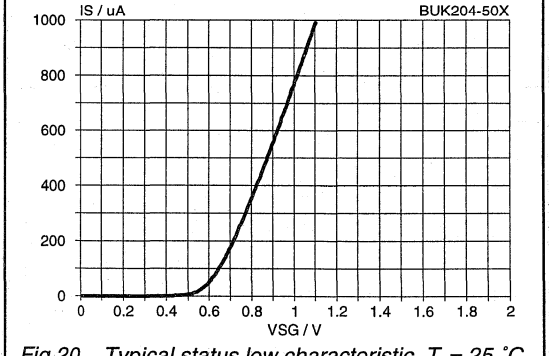


Fig.20. Typical status low characteristic, T_j = 25 ˚C.
I_S = f(V_{SG}); conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

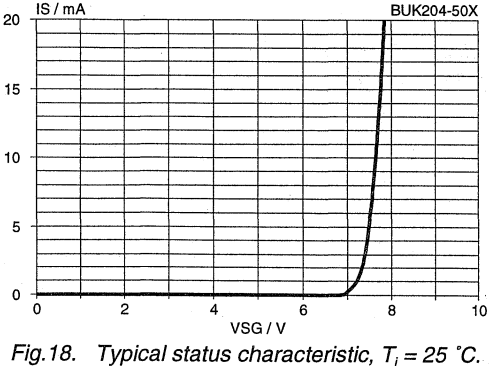


Fig.18. Typical status characteristic, T_j = 25 ˚C.
I_S = f(V_{SG}); conditions V_{IG} = V_{BG} = 0 V

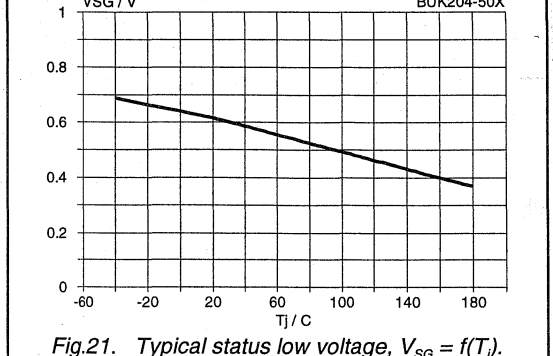


Fig.21. Typical status low voltage, V_{SG} = f(T_j).
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

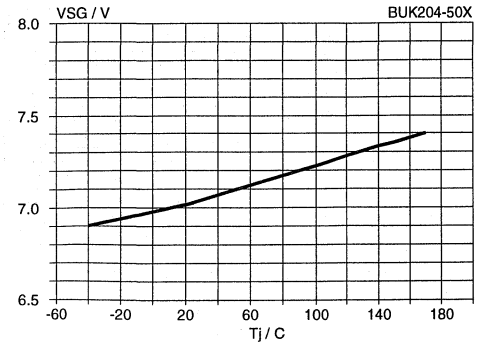


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

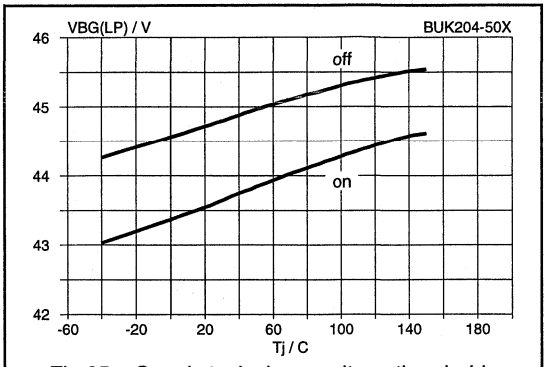


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 50\ mA$

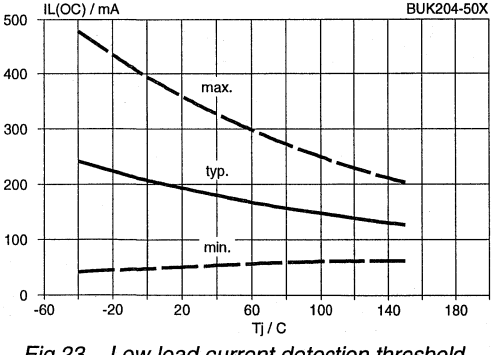


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

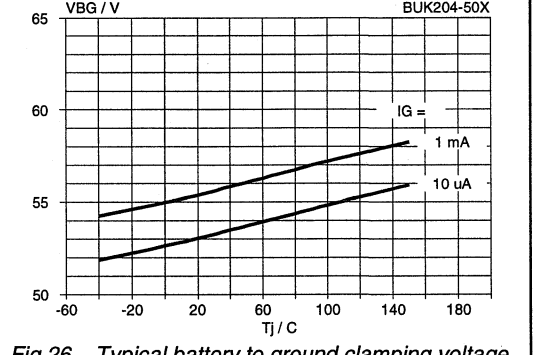


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

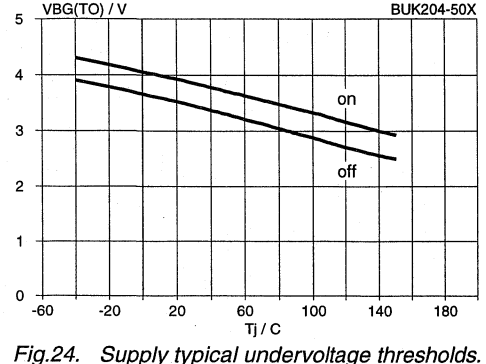


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 50\ mA$

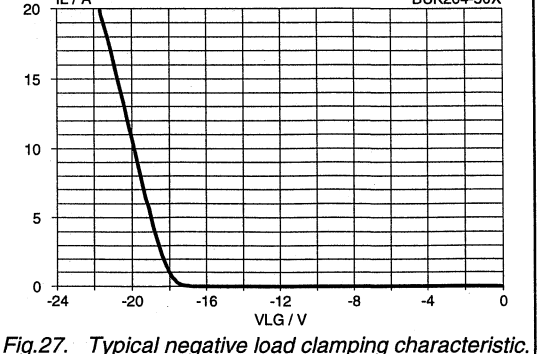


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 ˚C

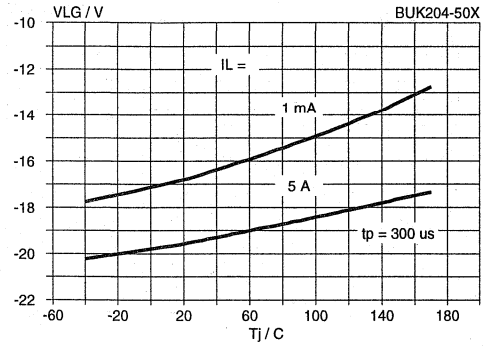


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

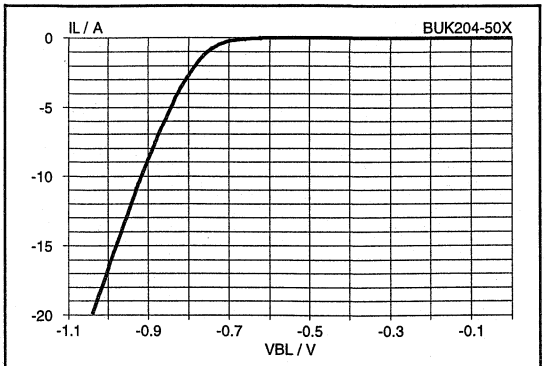


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

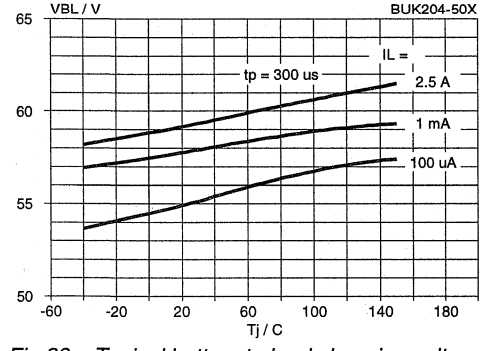


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

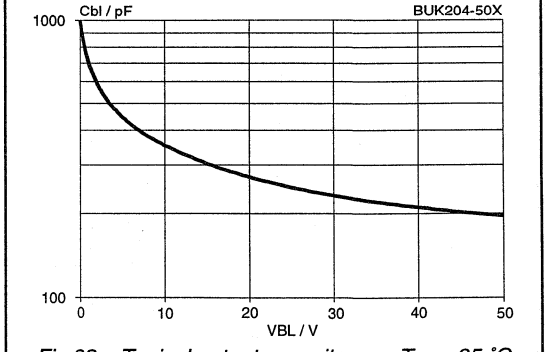


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

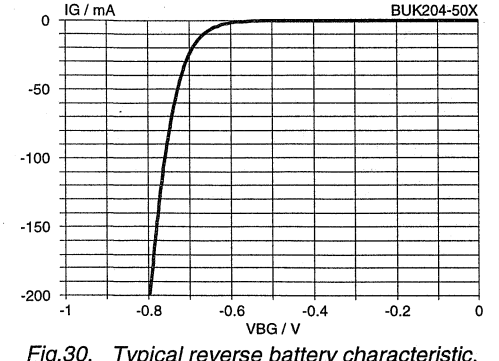


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

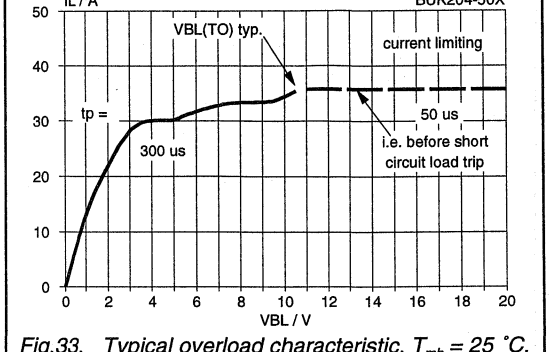


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

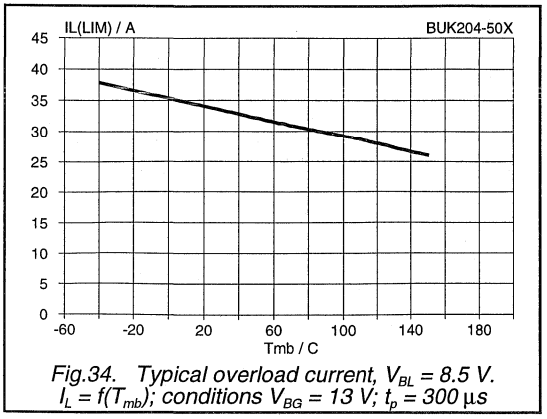


Fig.34. Typical overload current, V_{BL} = 8.5 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

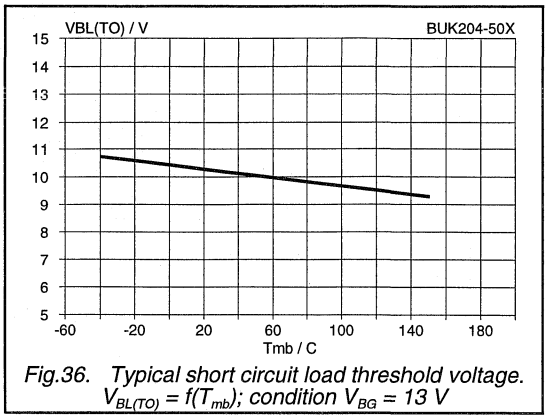


Fig.36. Typical short circuit threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

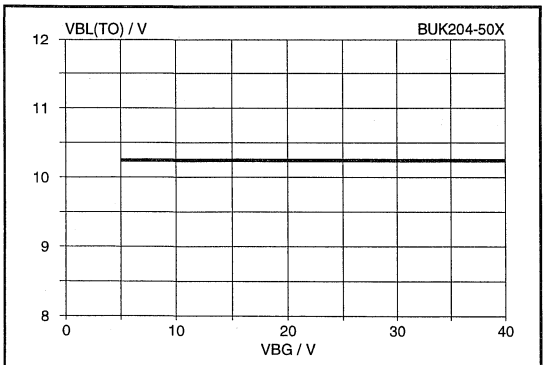


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 ˚C

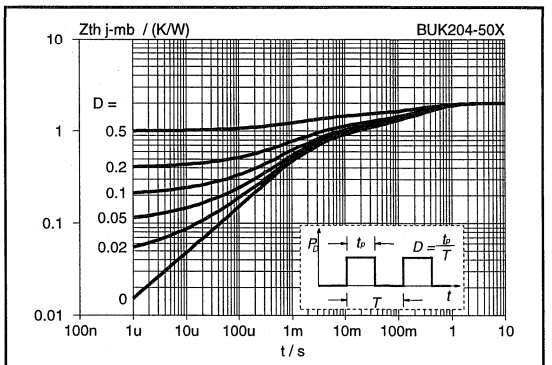


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch
SMD version of BUK200-50Y

BUK204-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	3.5	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	10	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	100	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

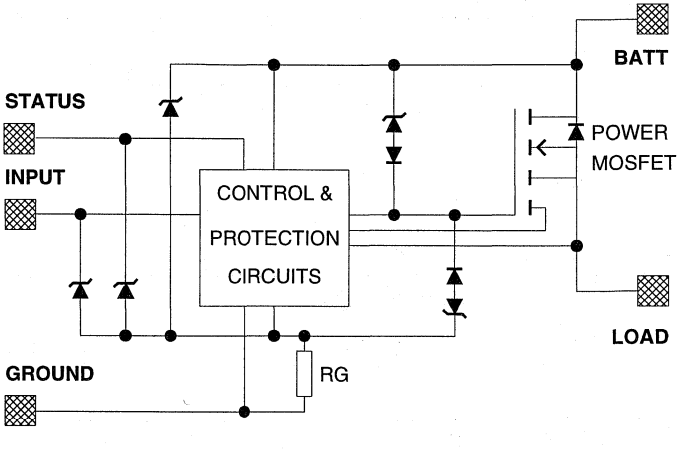


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

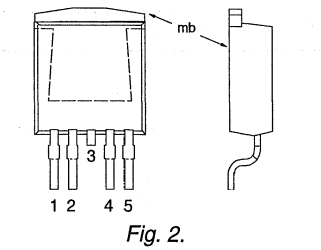


Fig. 2.

SYMBOL

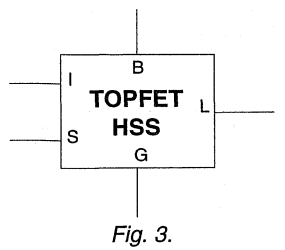


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115$ °C	-	10	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	62.5	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	T_{mb} = 150 °C prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.5	2	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	3.5	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 5 A; t_p = 300 µs	-	77	100	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1 A; t_p = 300 µs	-	116	150	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	50	200	350	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	8.5	10.3	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 80 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	35	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 8.5 V; t_p = 300 µs	23	33	43	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	V_{BL} = V_{BG} = 13 V	-	330	460	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

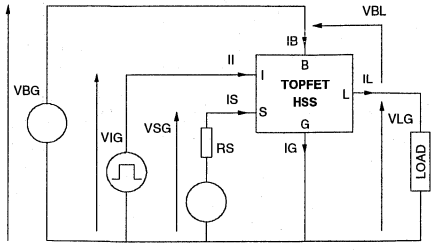


Fig.4. High side switch measurements schematic. (current and voltage conventions)

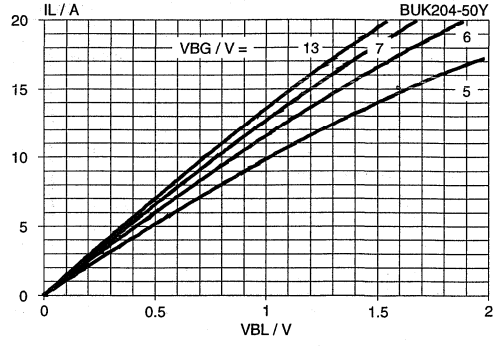


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

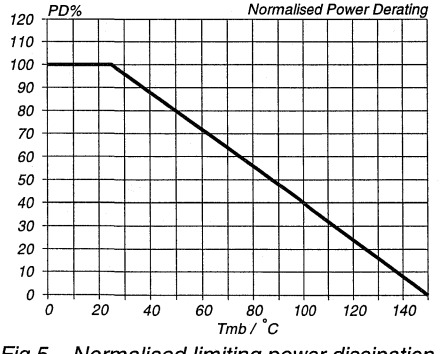


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

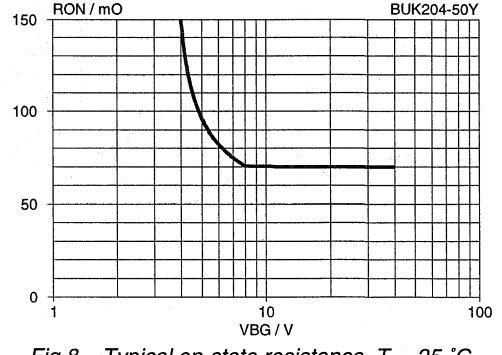


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 5 A; t_p = 300 µs

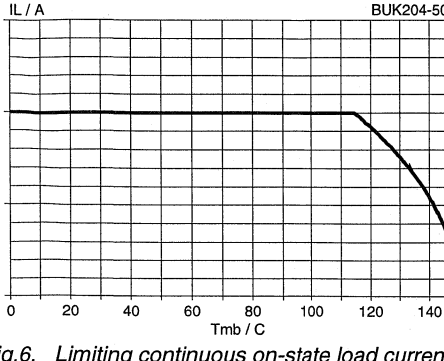


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

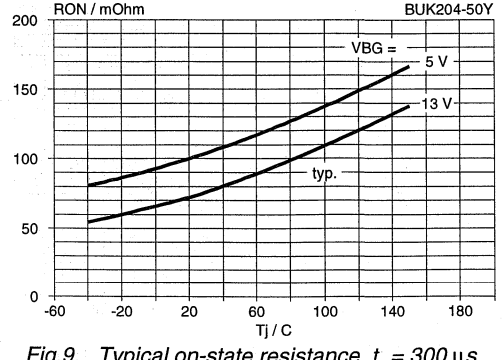


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1 A

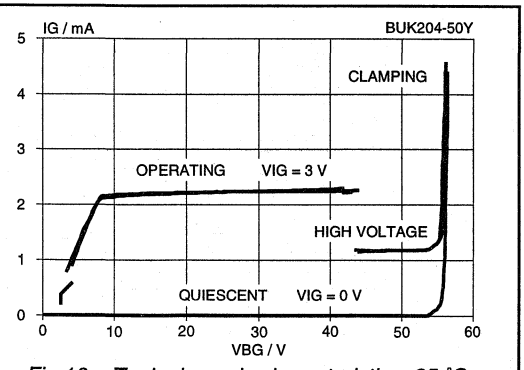


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

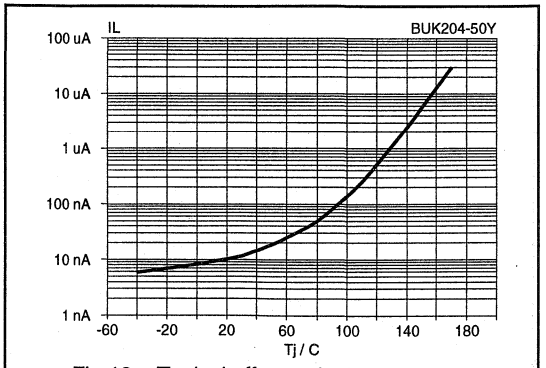


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

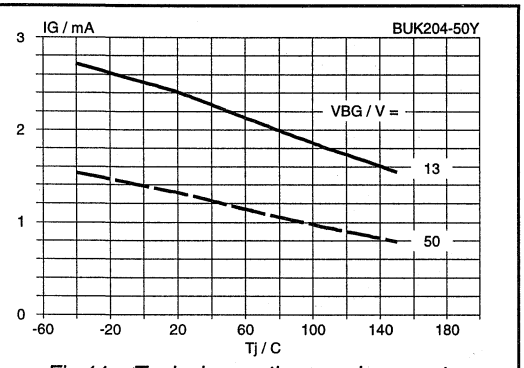


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

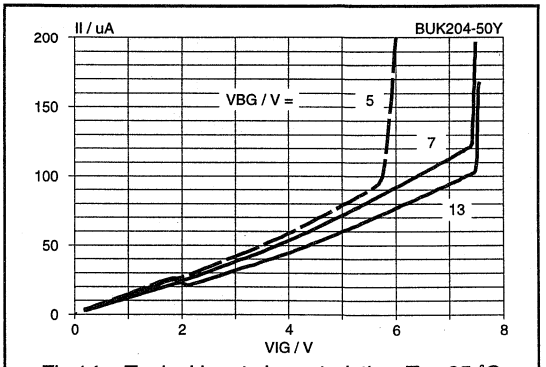


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

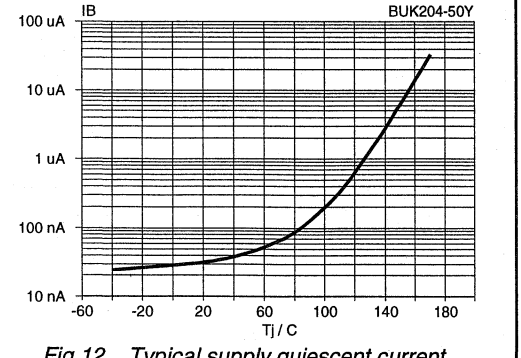


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

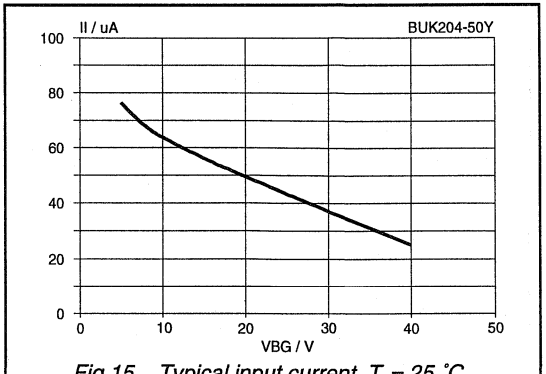


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

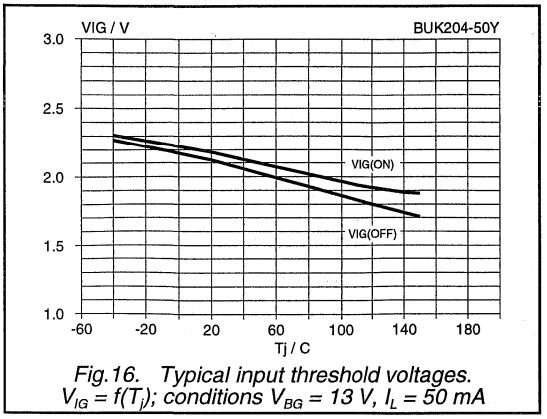


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions $V_{BG} = 13$ V, $I_L = 50$ mA

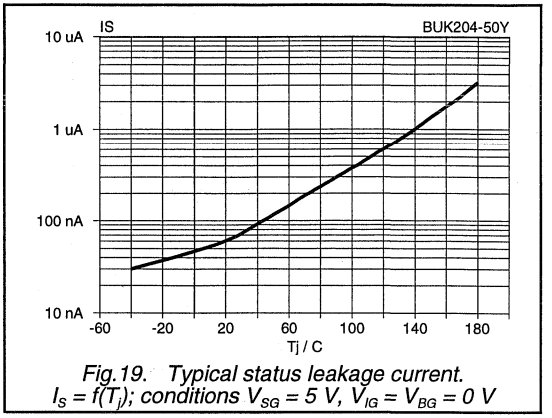


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions $V_{SG} = 5$ V, $V_{IG} = V_{BG} = 0$ V

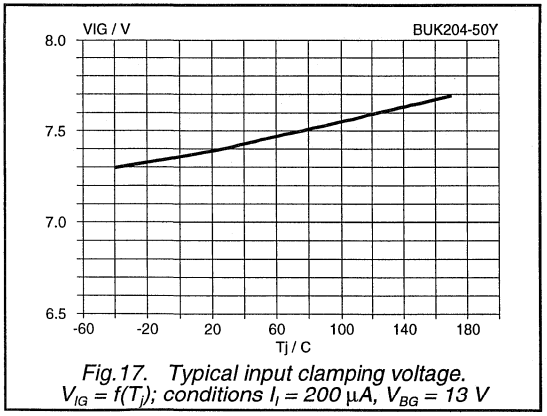


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions $I_I = 200$ µA, $V_{BG} = 13$ V

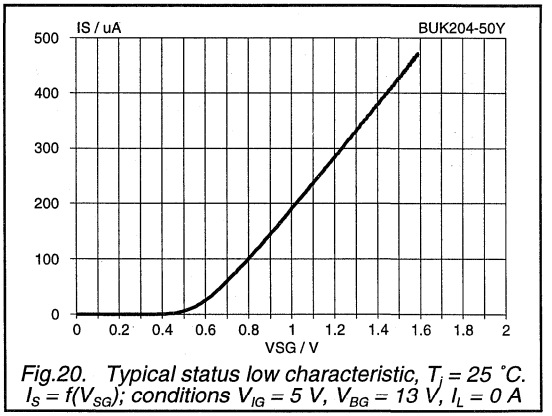


Fig.20. Typical status low characteristic, $T_j = 25$ ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

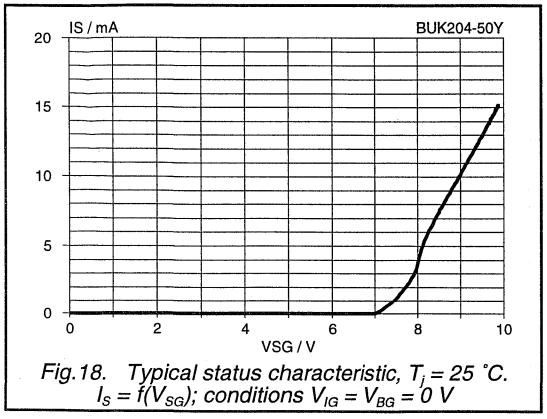


Fig.18. Typical status characteristic, $T_j = 25$ ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG} = 0$ V

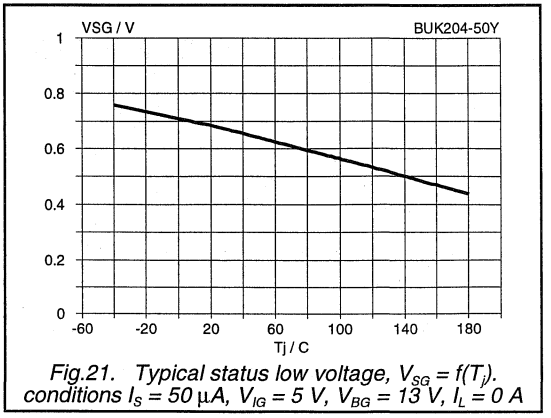


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions $I_S = 50$ µA, $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

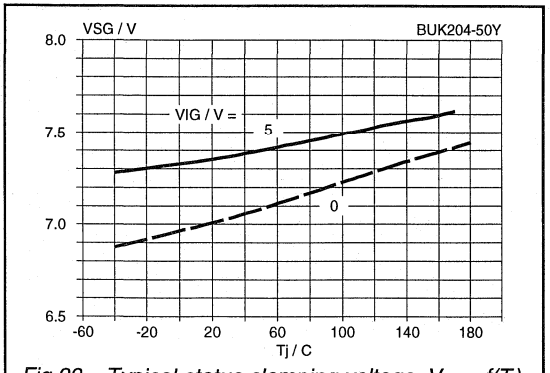


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

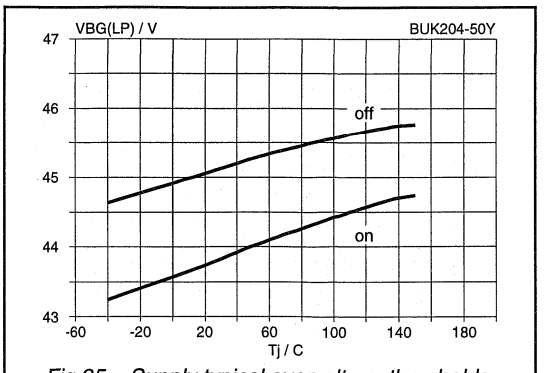


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 50\ mA$

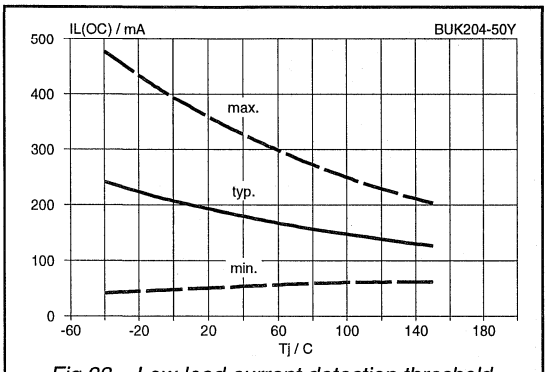


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

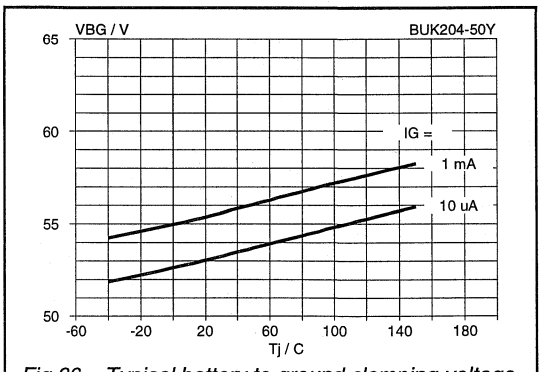


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

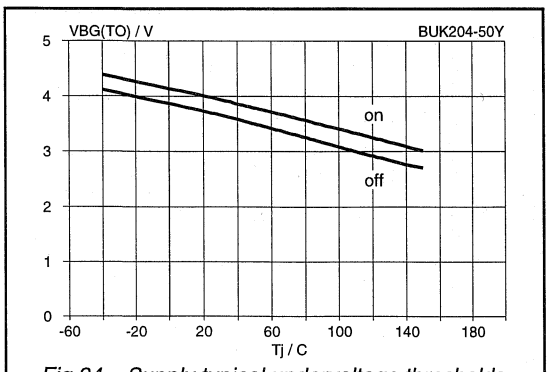


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 50\ mA$

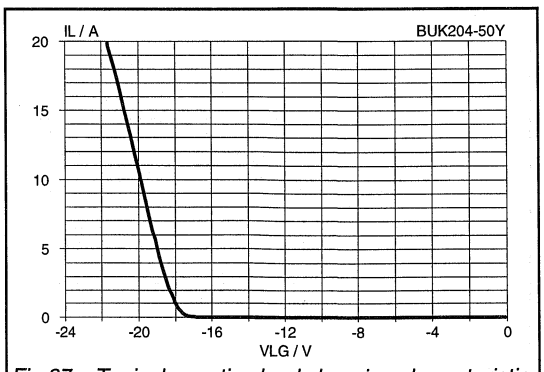


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

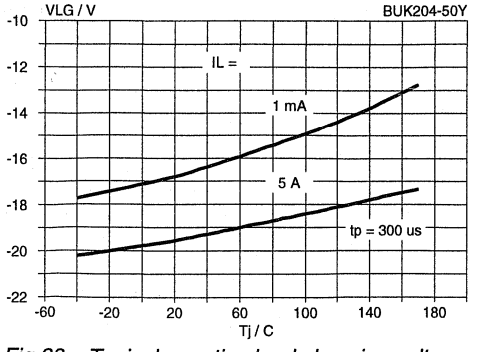


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

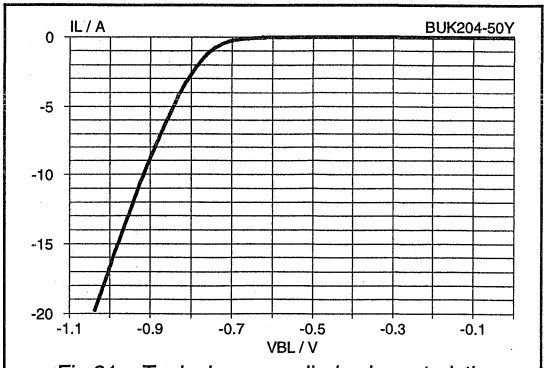


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

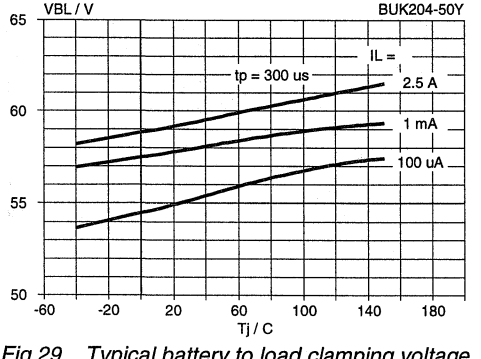


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

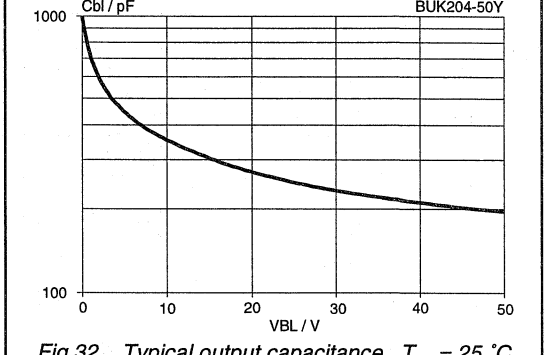


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

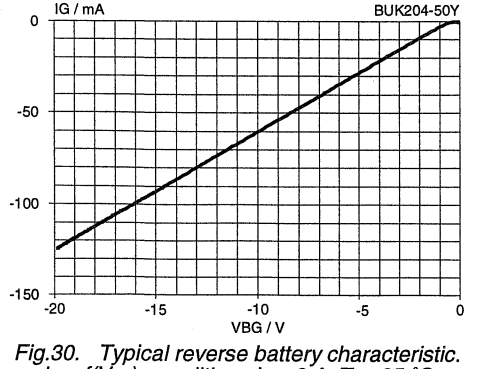


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

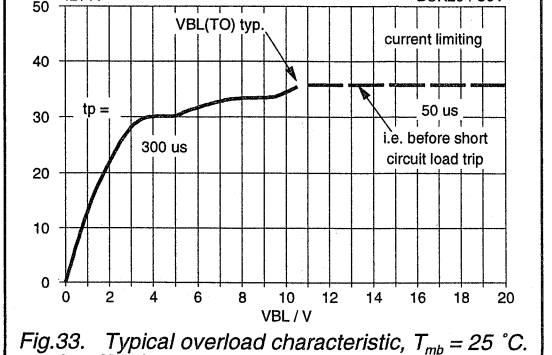


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

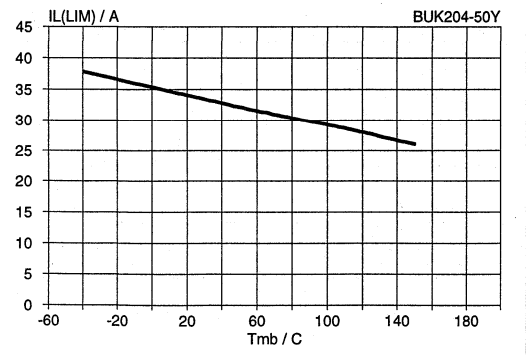


Fig.34. Typical overload current, V_{BL} = 8.5 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

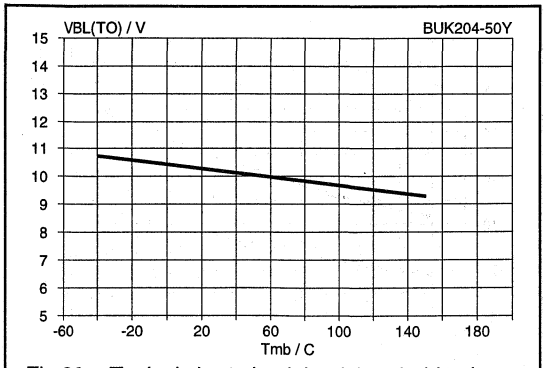


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

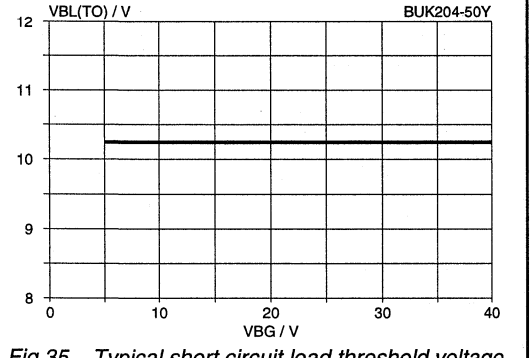


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 ˚C

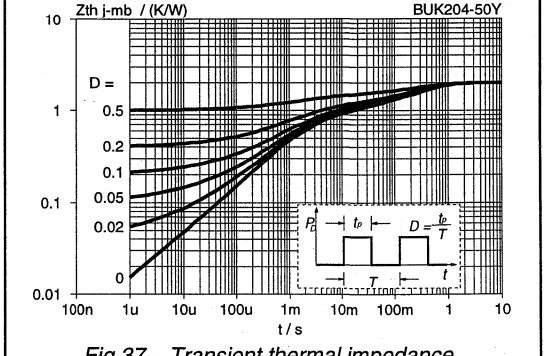


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch
SMD version of BUK201-50X

BUK205-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	15	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	60	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

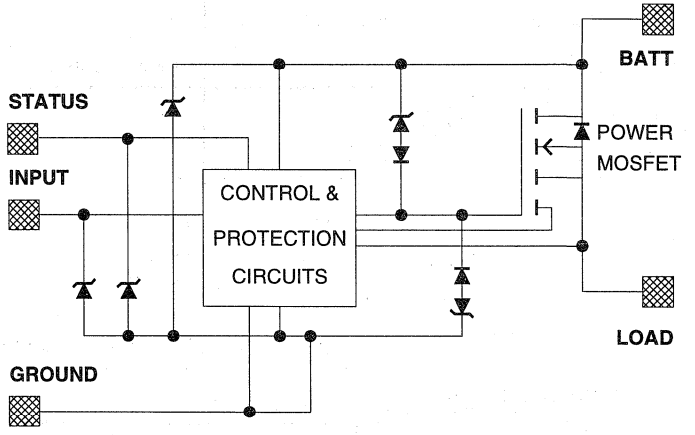


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

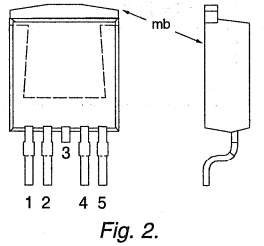


Fig. 2.

SYMBOL

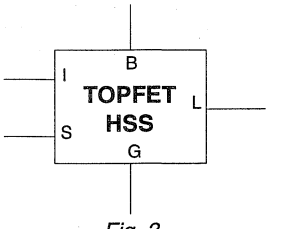


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115$ °C	-	15	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	83.3	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	T_{mb} = 150 °C prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.2	1.5	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 7.5 A; t_p = 300 µs	-	45	60	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1.5 A; t_p = 300 µs	-	70	90	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	100	350	600	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 140 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 7.5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	28	40	52	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	415	580	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

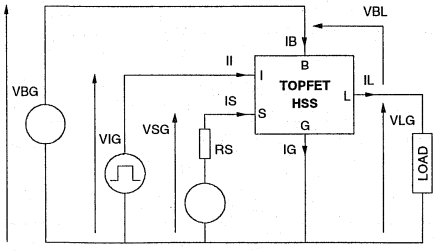


Fig.4. High side switch measurements schematic. (current and voltage conventions)

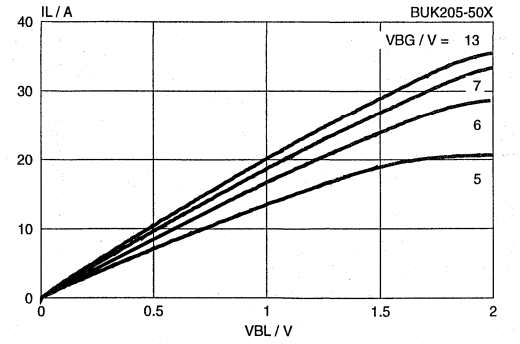


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

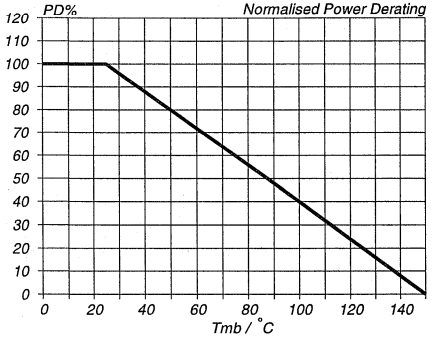


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\,^{\circ}C) = f(T_{mb})$

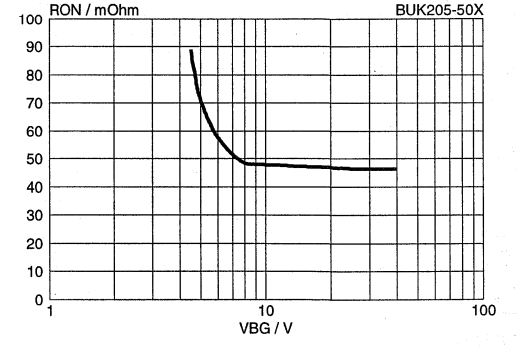


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 7.5 A; t_p = 300 µs

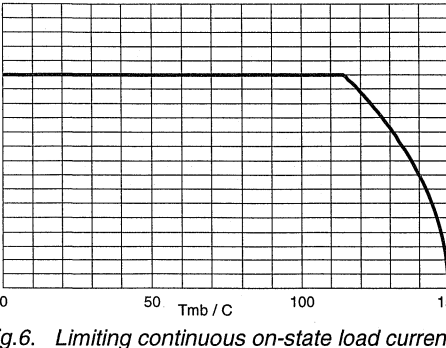


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

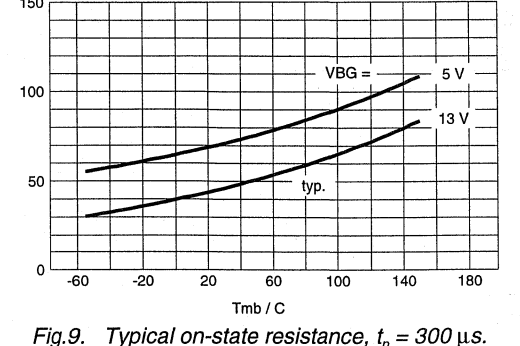


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1.5 A

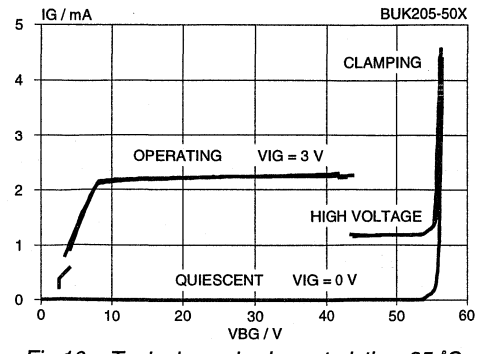


Fig.10. Typical supply characteristics, 25 °C. $I_G = f(V_{BG})$; parameter V_{IG}

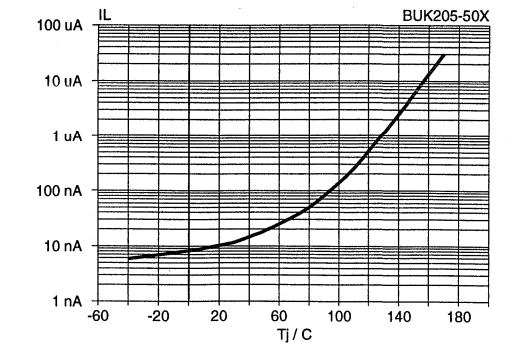


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: $V_{BL} = 13\ V = V_{BG}$; $V_{IG} = 0\ V$.

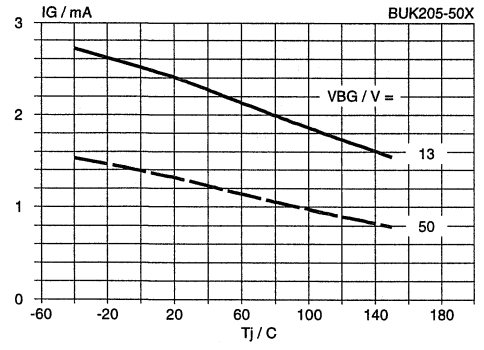


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition $V_{IG} = 5\ V$

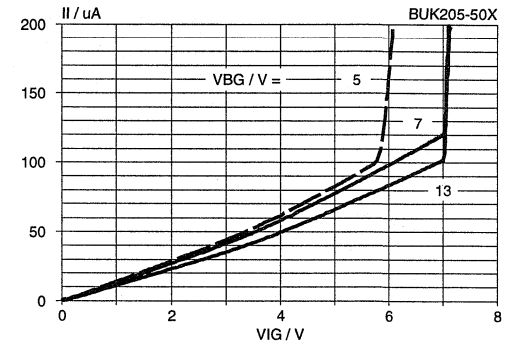


Fig.14. Typical input characteristics, $T_j = 25$ °C. $I_I = f(V_{IG})$; parameter V_{BG}

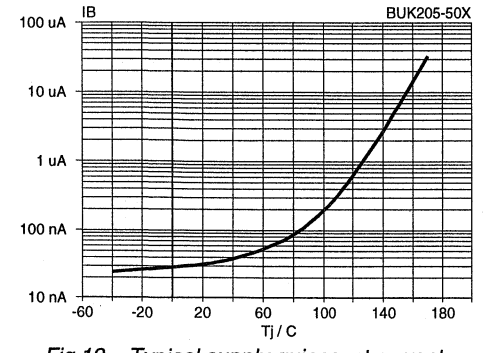


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition $V_{BG} = 13\ V$, $V_{IG} = 0\ V$, $V_{LG} = 0\ V$

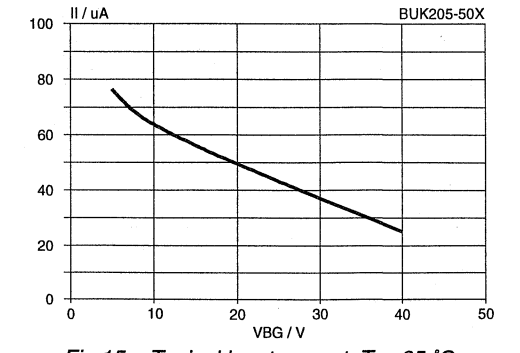


Fig.15. Typical input current, $T_j = 25$ °C. $I_I = f(V_{BG})$; condition $V_{IG} = 5\ V$

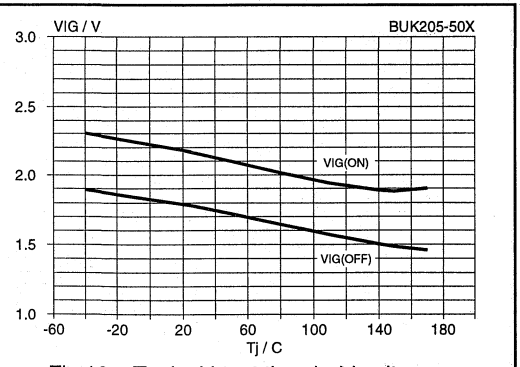


Fig.16. Typical input threshold voltages.
V_{IG} = f(T_j); conditions V_{BG} = 13 V, I_L = 80 mA

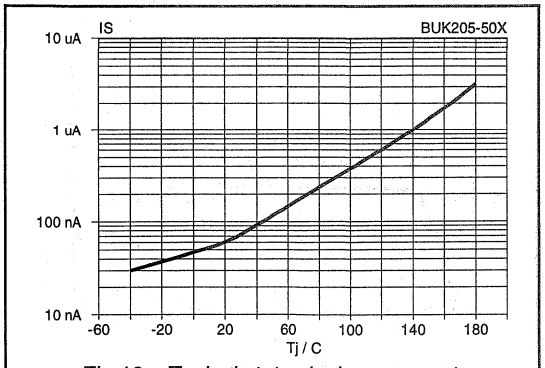


Fig.19. Typical status leakage current.
I_S = f(T_j); conditions V_{SG} = 5 V, V_{IG} = V_{BG} = 0 V

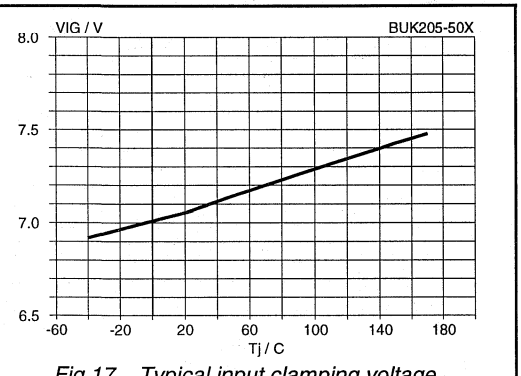


Fig.17. Typical input clamping voltage.
V_{IG} = f(T_j); conditions I_I = 200 µA, V_{BG} = 13 V

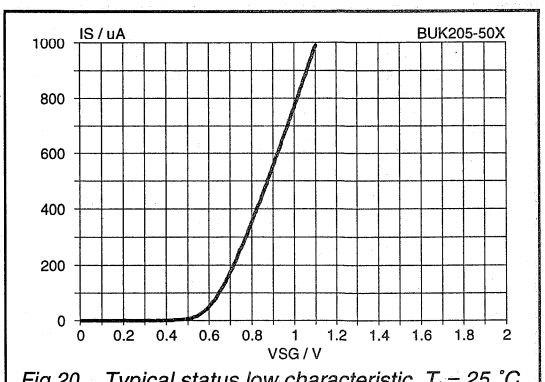


Fig.20. Typical status low characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

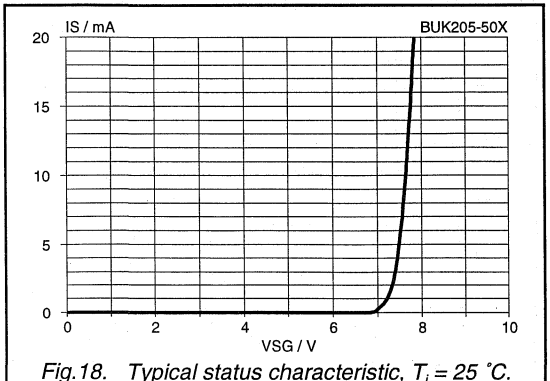


Fig.18. Typical status characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = V_{BG} = 0 V

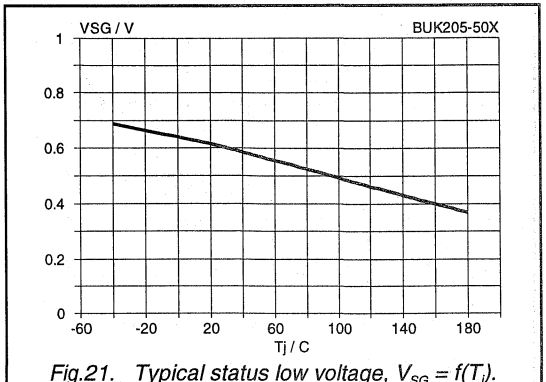


Fig.21. Typical status low voltage, V_{SG} = f(T_j).
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

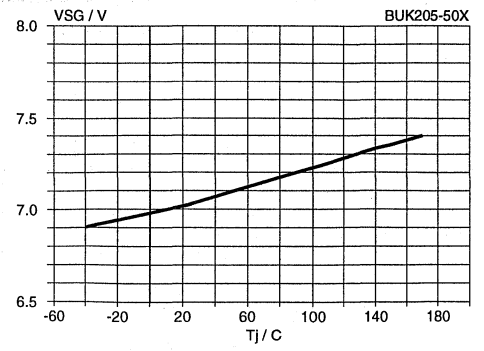


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

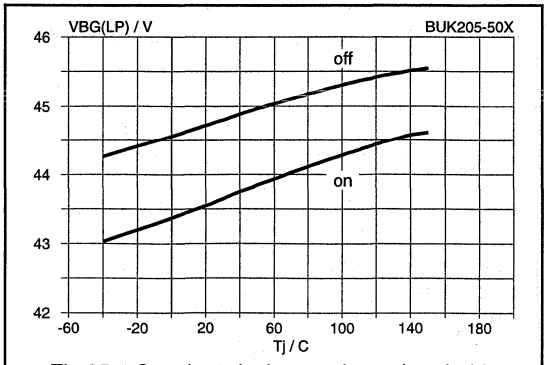


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 80\ mA$

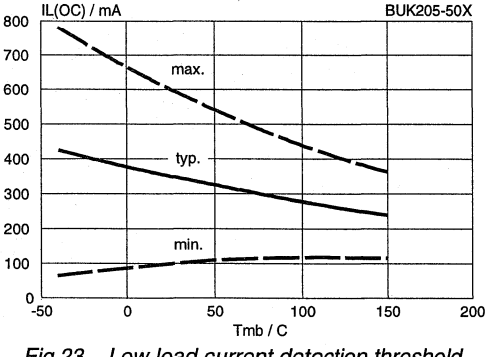


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

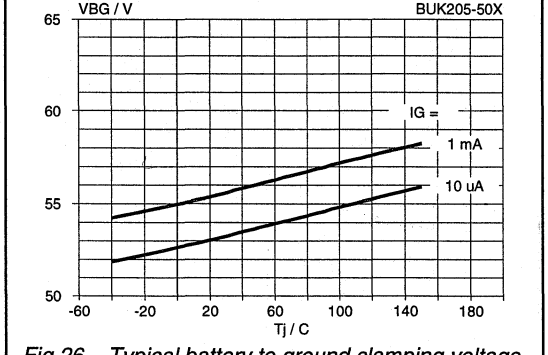


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

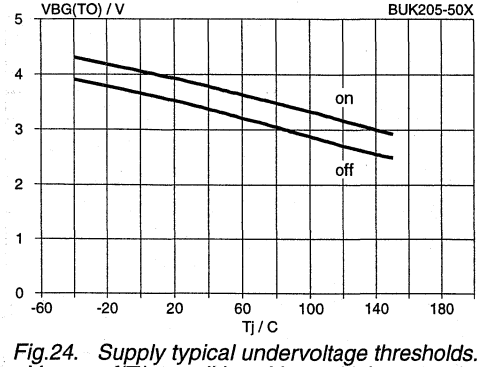


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 80\ mA$

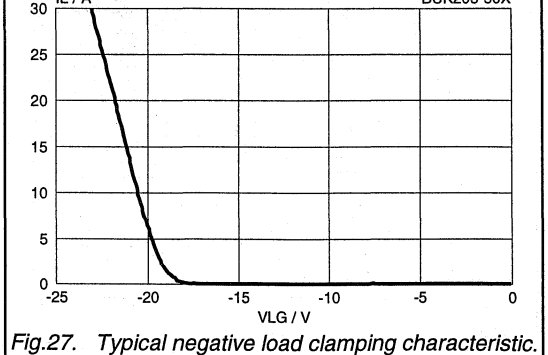


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

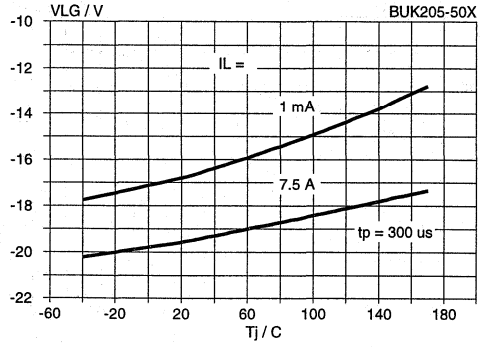


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

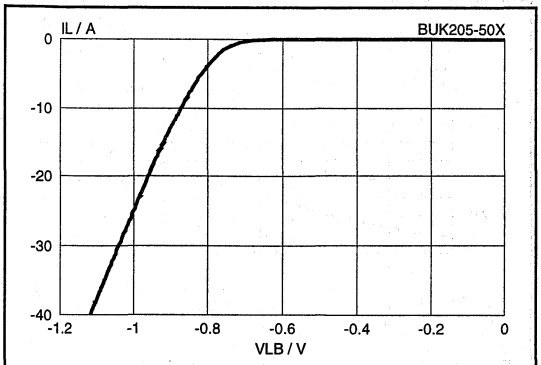


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

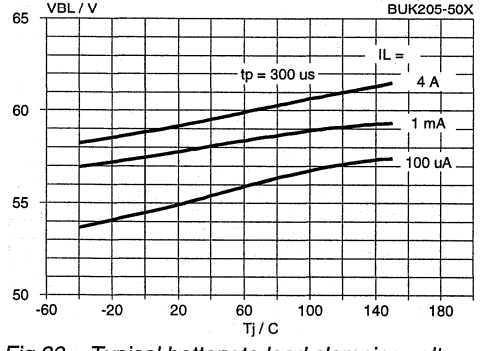


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

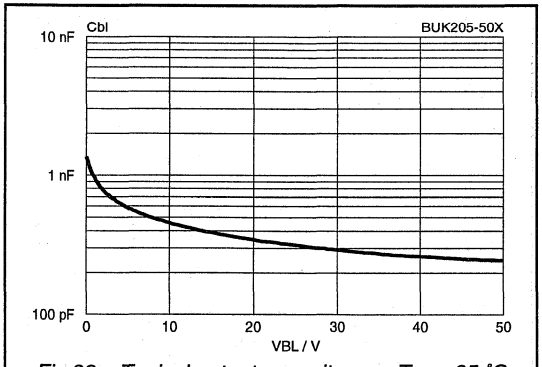


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

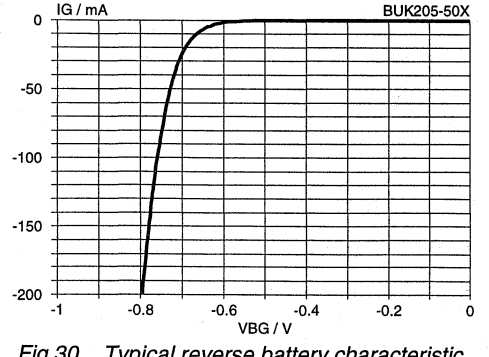


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

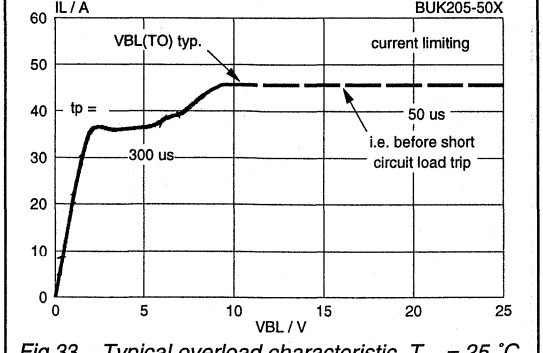


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

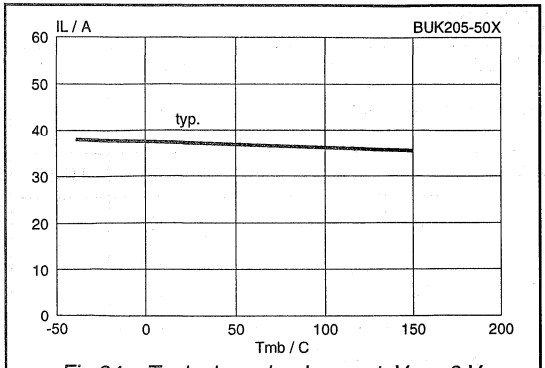


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

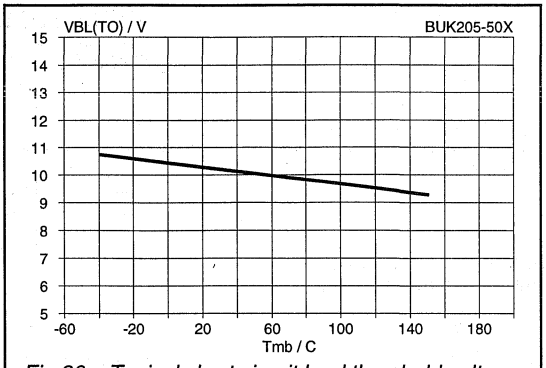


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

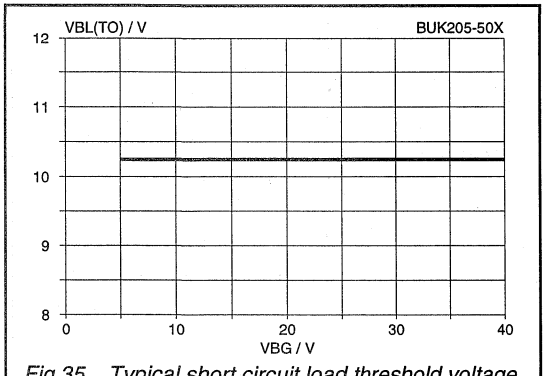


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

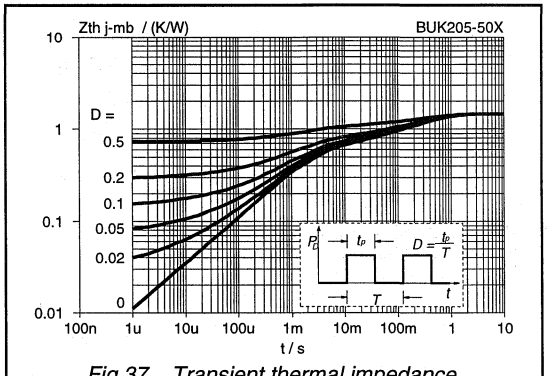


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch
SMD version of BUK201-50Y

BUK205-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	15	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	60	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

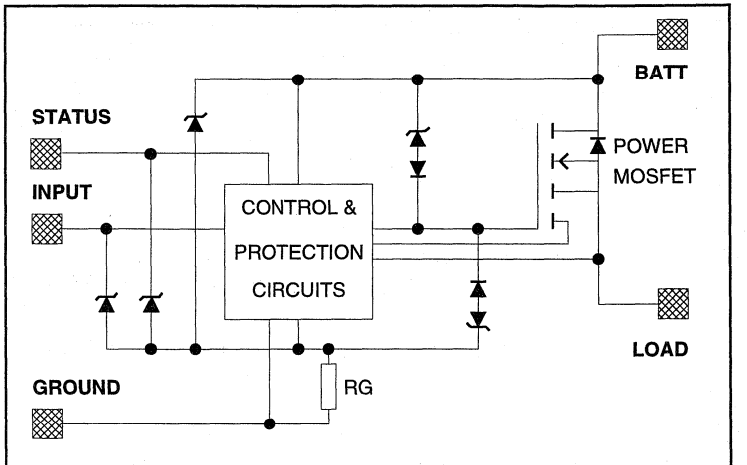


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

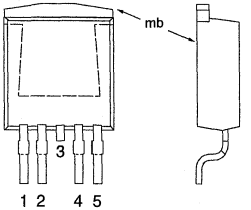


Fig. 2.

SYMBOL

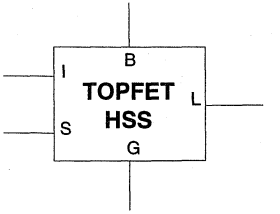


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 115\ ^\circ C$	-	15	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	83.3	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.2	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.2	1.5	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 7.5 A; t_p = 300 µs	-	45	60	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 1.5 A; t_p = 300 µs	-	70	90	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	100	350	600	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 140 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 7.5 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	90	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	42	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	28	40	52	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1	2.5	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	30	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.2	2.5	V/µs
t_{off}	Total switching time	to 10% V_L	-	50	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	415	580	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

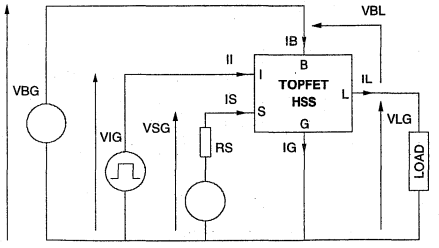


Fig.4. High side switch measurements schematic. (current and voltage conventions)

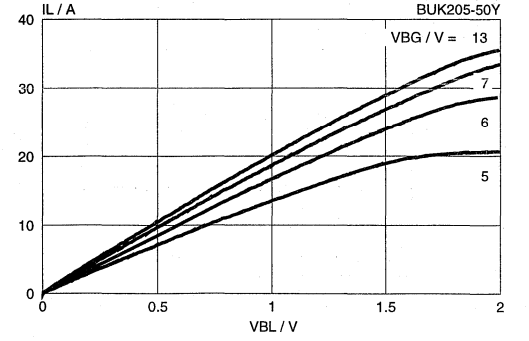


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

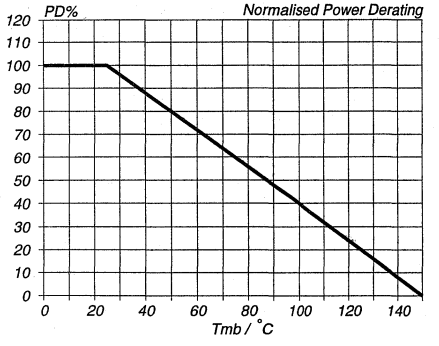


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

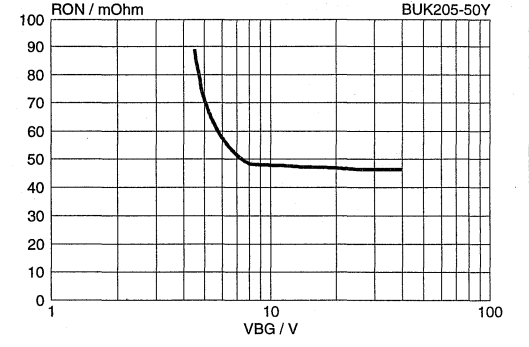


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 7.5 A; t_p = 300 µs

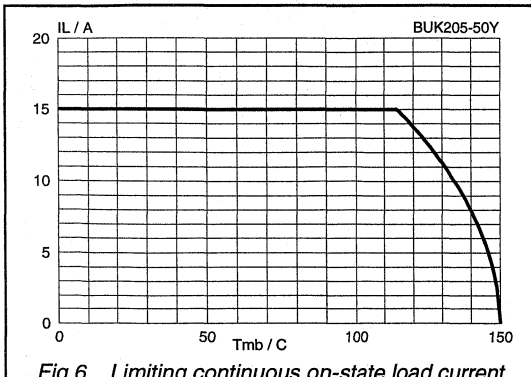


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

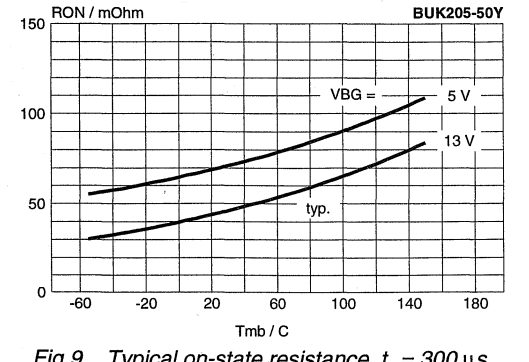


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 1.5 A

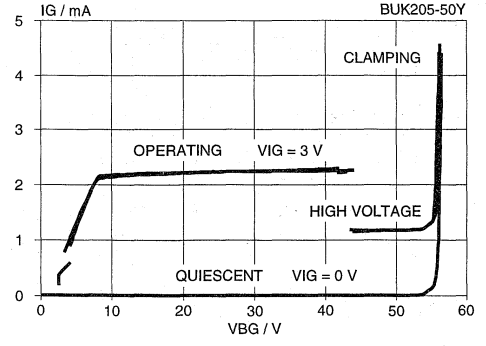


Fig.10. Typical supply characteristics, 25 ˚C.
$I_G = f(V_{BG})$; parameter V_{IG}

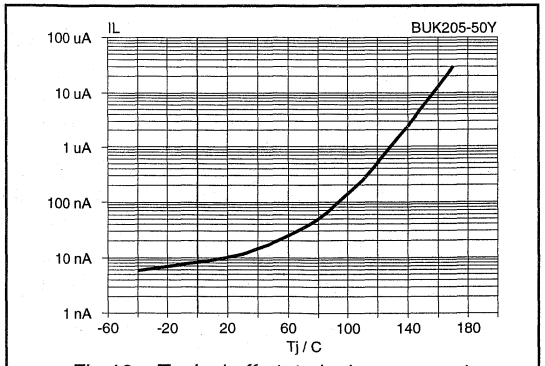


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

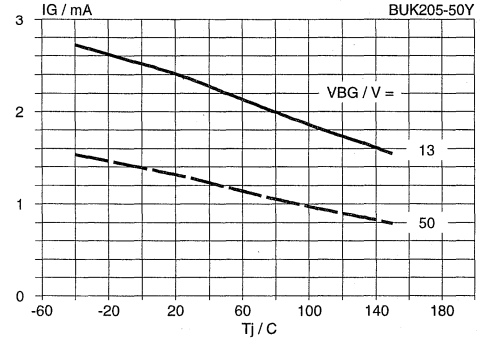


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

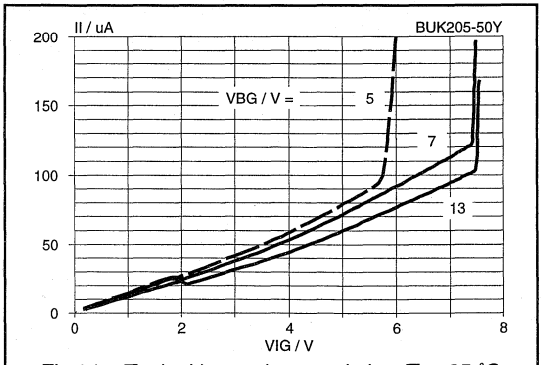


Fig.14. Typical input characteristics, T_j = 25 ˚C.
$I_I = f(V_{IG})$; parameter V_{BG}

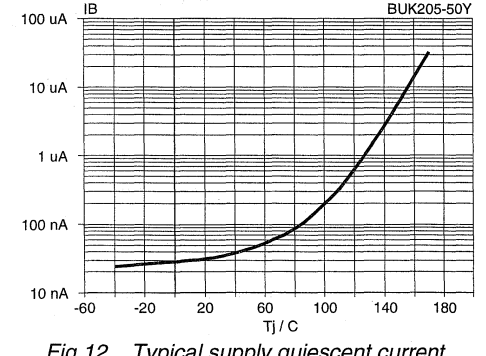


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

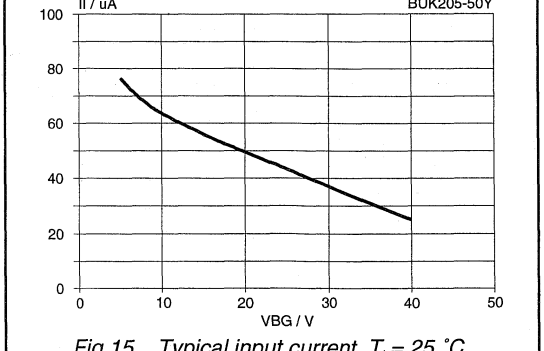


Fig.15. Typical input current, T_j = 25 ˚C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

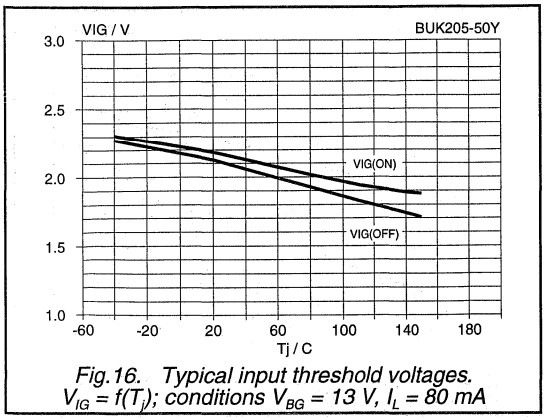


Fig.16. Typical input threshold voltages.
V_{IG} = f(T_j); conditions V_{BG} = 13 V, I_L = 80 mA

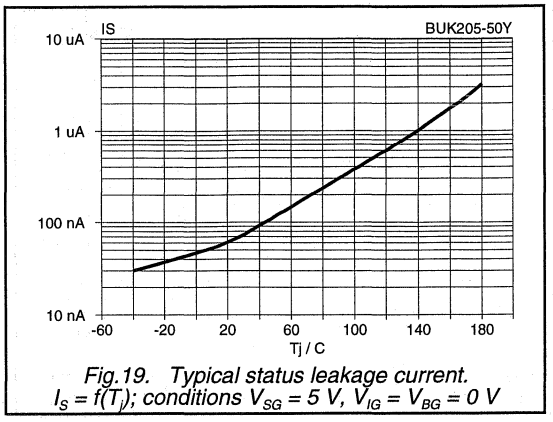


Fig.19. Typical status leakage current.
I_S = f(T_j); conditions V_{SG} = 5 V, V_{IG} = V_{BG} = 0 V

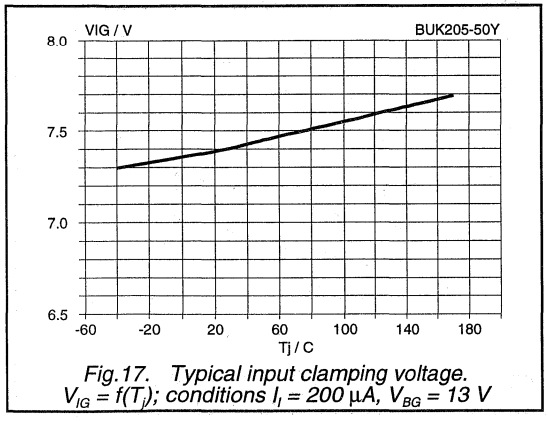


Fig.17. Typical input clamping voltage.
V_{IG} = f(T_j); conditions I_I = 200 µA, V_{BG} = 13 V

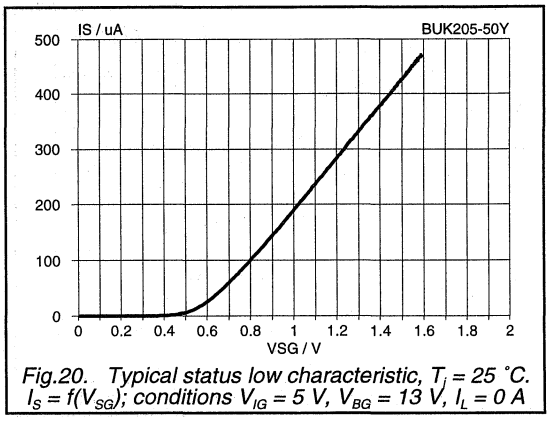


Fig.20. Typical status low characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

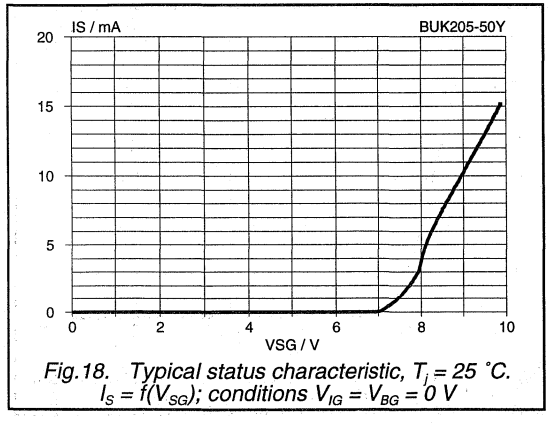


Fig.18. Typical status characteristic, T_j = 25 °C.
I_S = f(V_{SG}); conditions V_{IG} = V_{BG} = 0 V

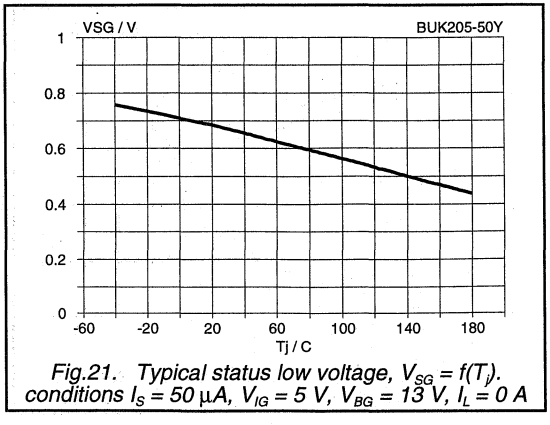


Fig.21. Typical status low voltage, V_{SG} = f(T_j).
conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

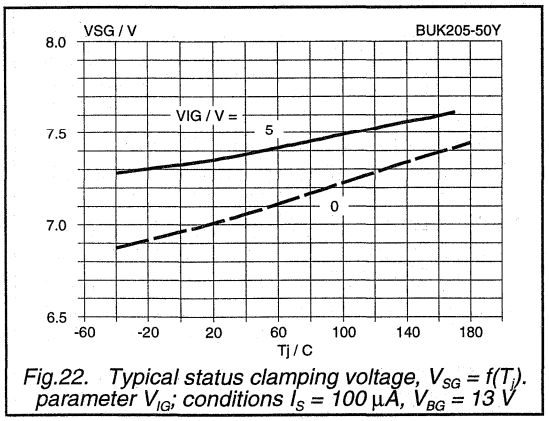


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

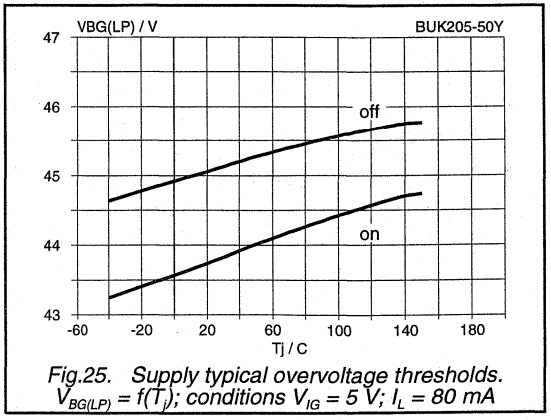


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 80\ mA$

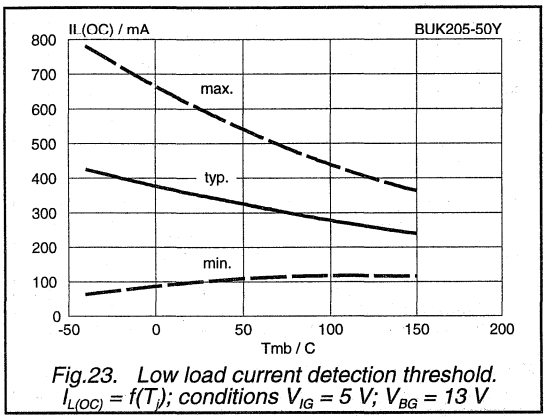


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

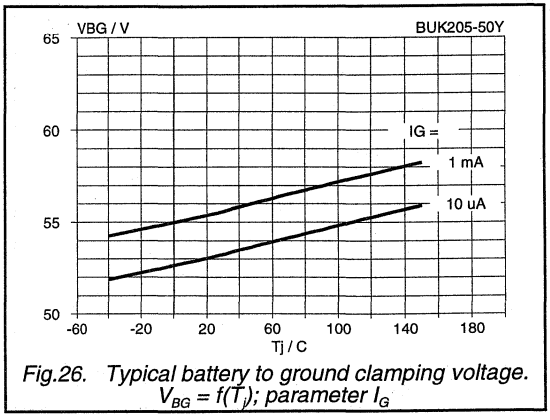


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

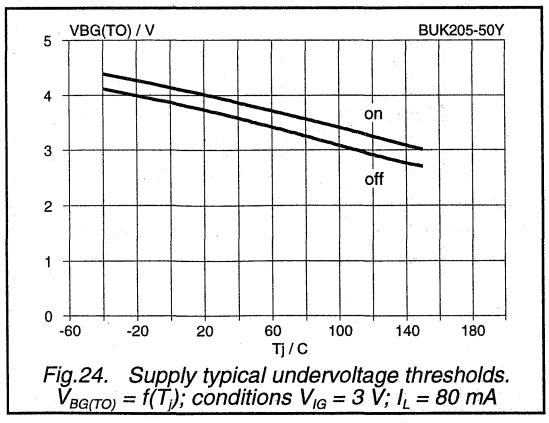


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 80\ mA$

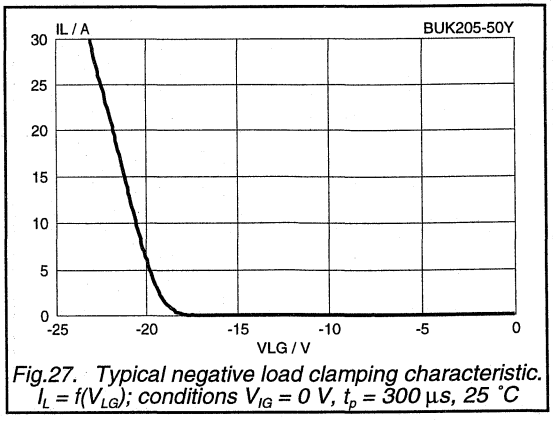


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

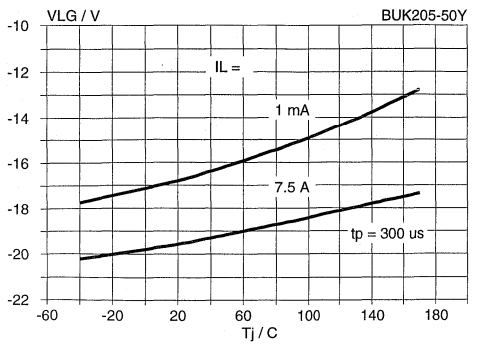


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

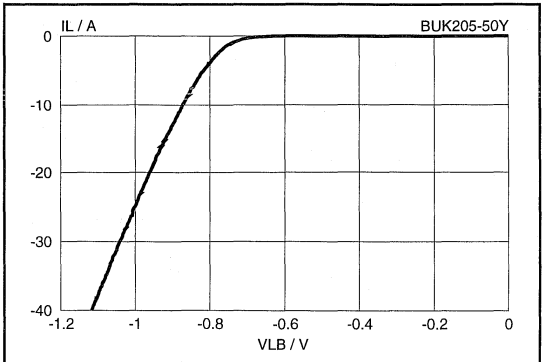


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

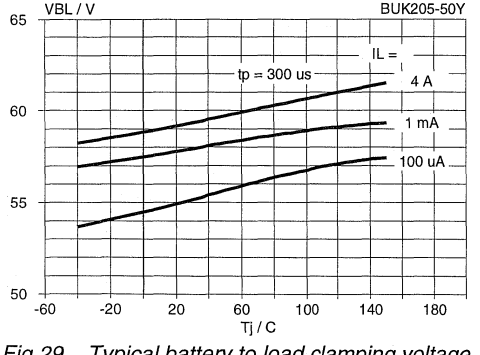


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

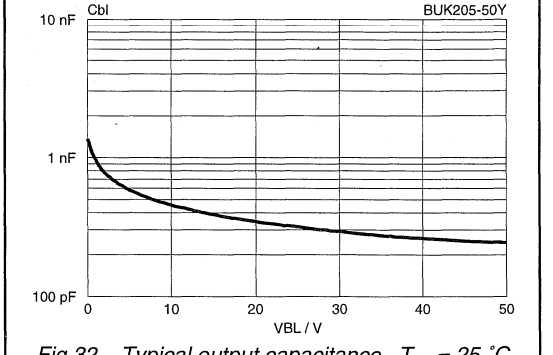


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

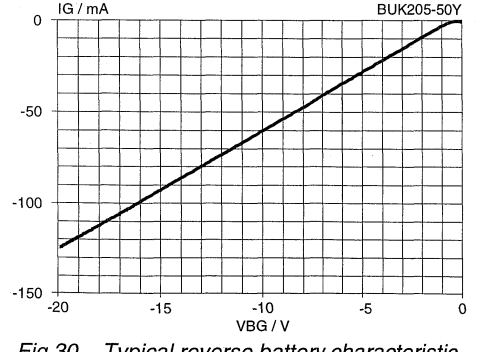


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

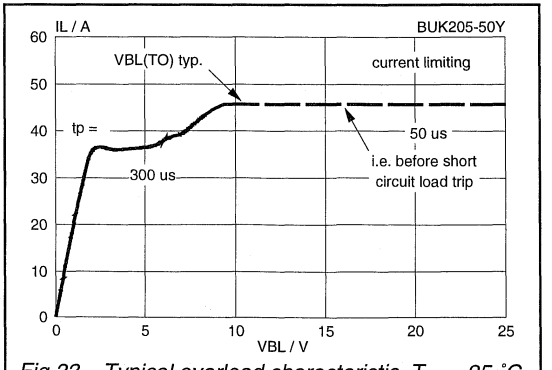


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

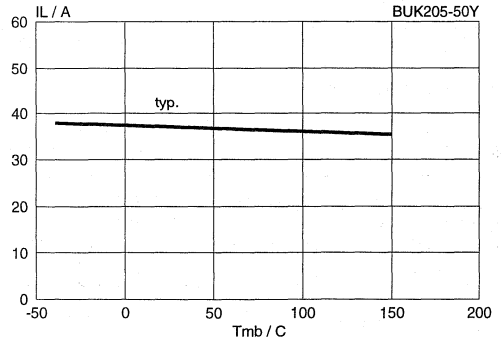


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 300 µs

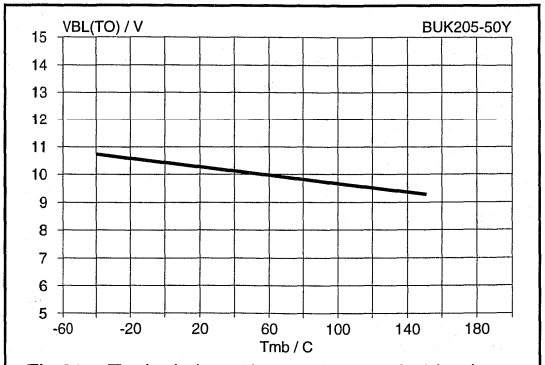


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

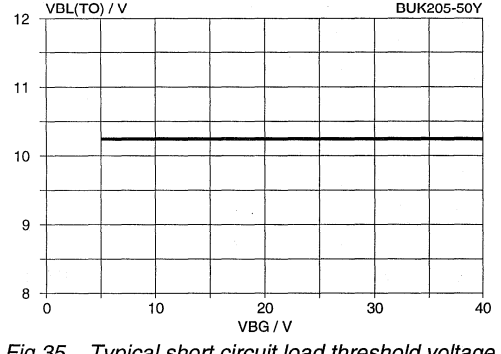


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

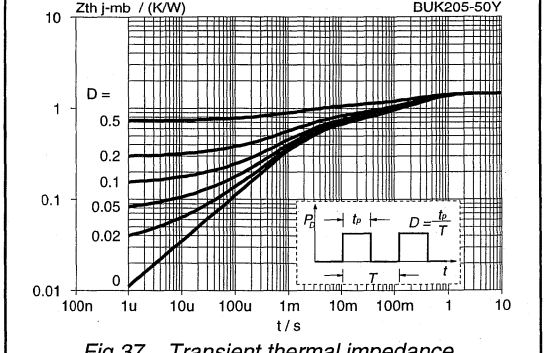


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch
SMD version of BUK202-50X

BUK206-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FUNCTIONAL BLOCK DIAGRAM

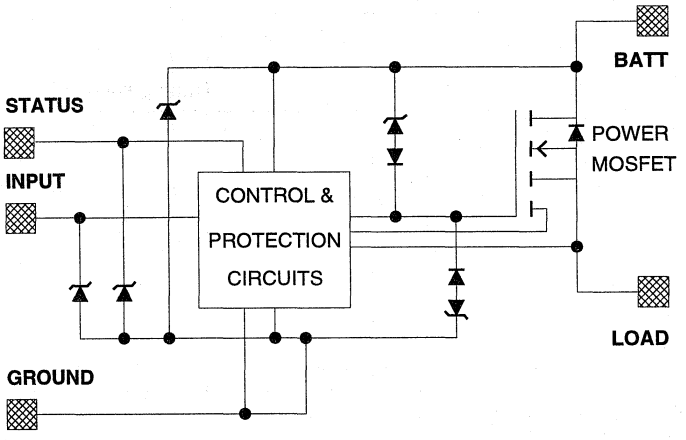


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

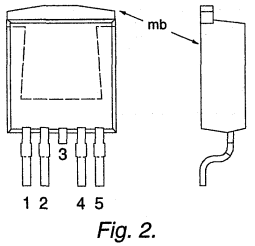


Fig. 2.

SYMBOL

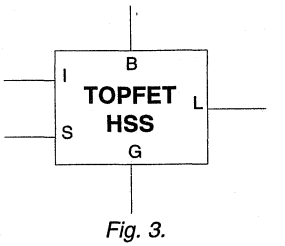


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W

1 Reverse battery voltage is allowed only with external ground, input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	50	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	34	45	64	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

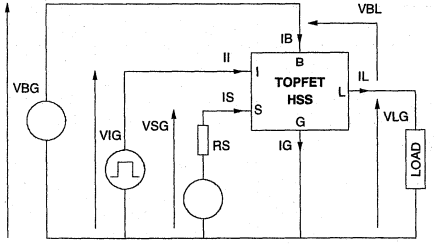


Fig.4. High side switch measurements schematic. (current and voltage conventions)

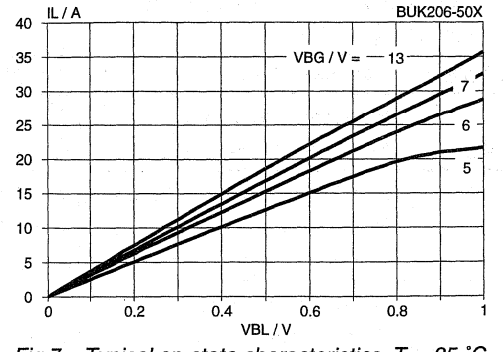


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

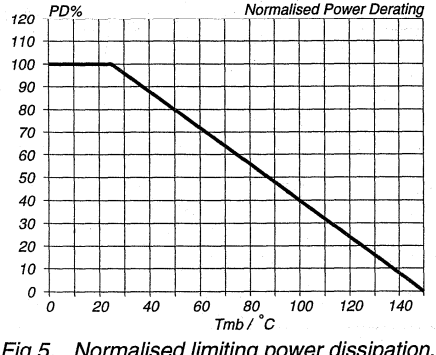


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

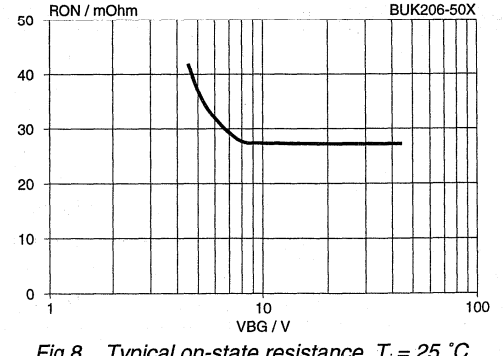


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

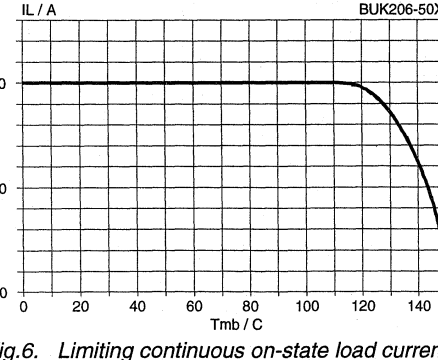


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

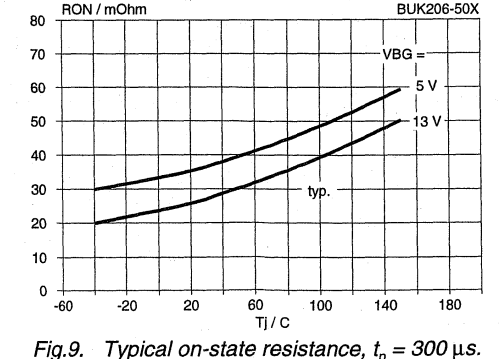


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

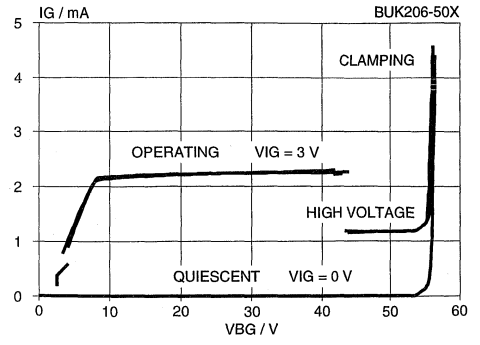


Fig.10. Typical supply characteristics, 25 °C.
$I_G = f(V_{BG})$; parameter V_{IG}

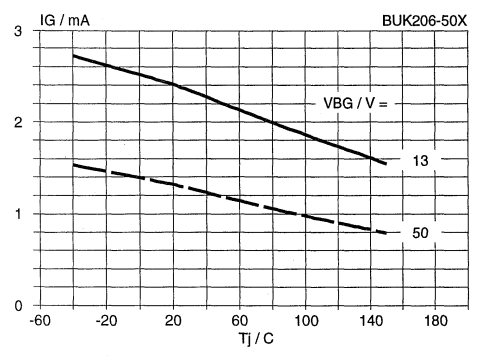


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

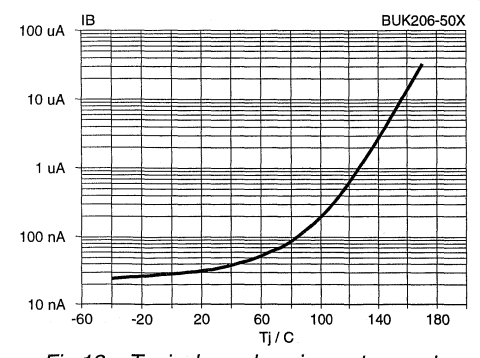


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

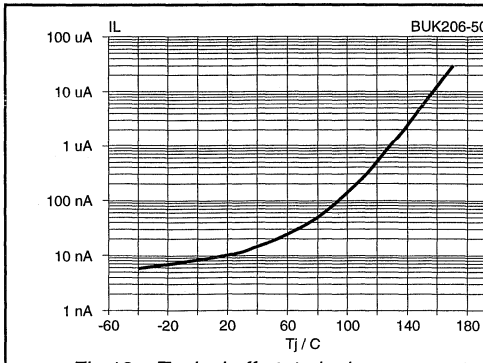


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

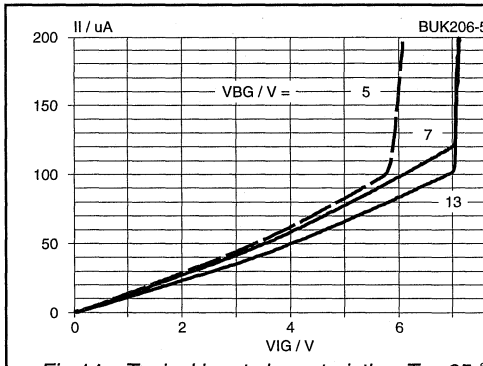


Fig.14. Typical input characteristics, T_j = 25 °C.
$I_I = f(V_{IG})$; parameter V_{BG}

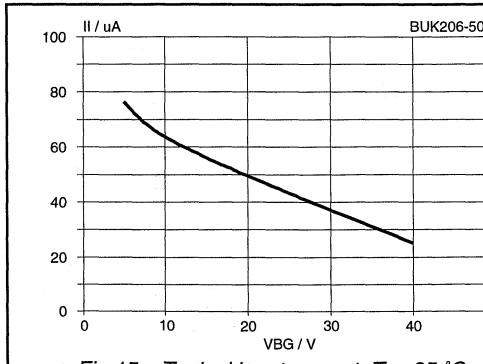


Fig.15. Typical input current, T_j = 25 °C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

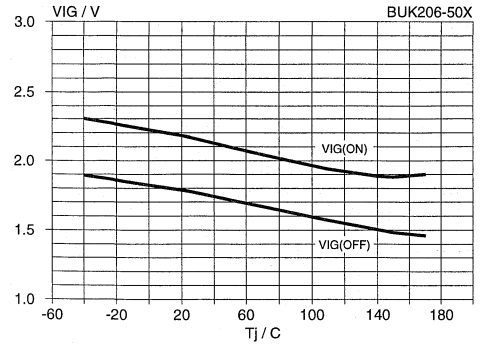


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

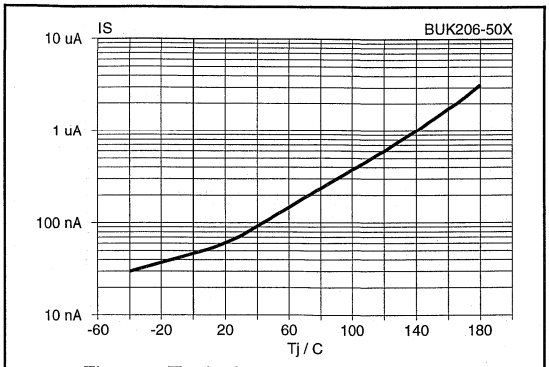


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

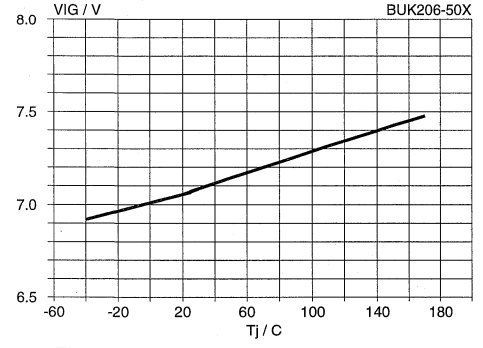


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

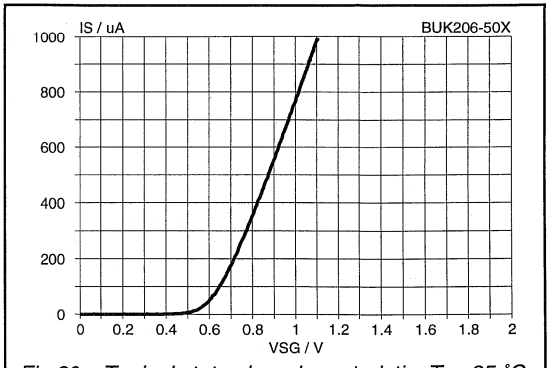


Fig.20. Typical status low characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

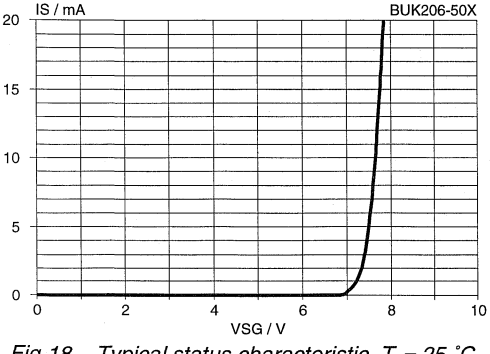


Fig.18. Typical status characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

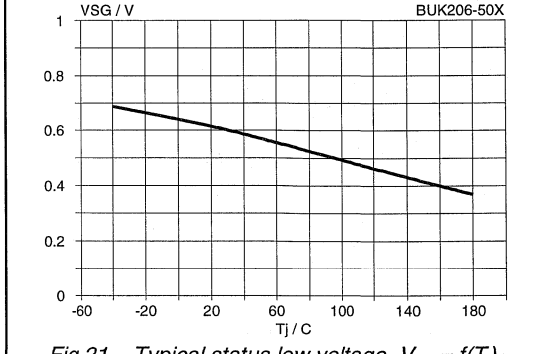


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

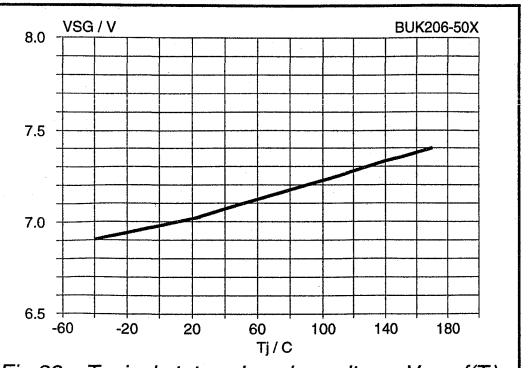


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

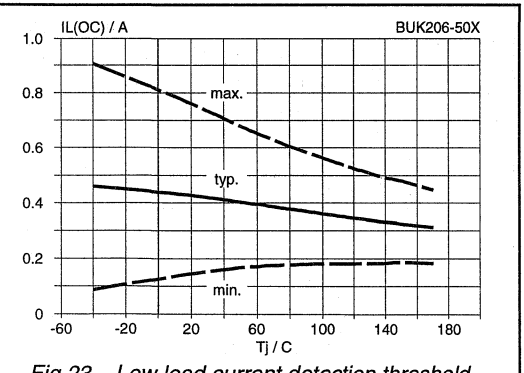


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

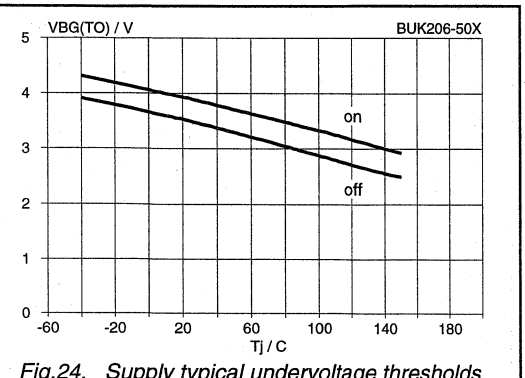


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

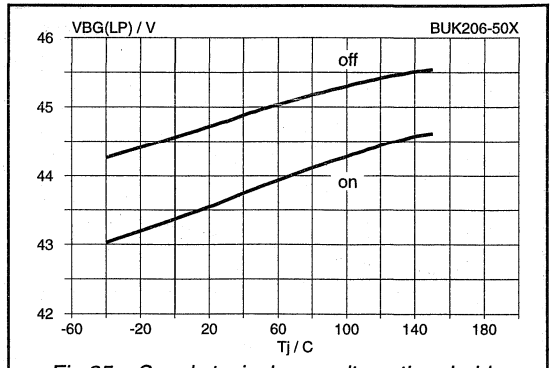


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

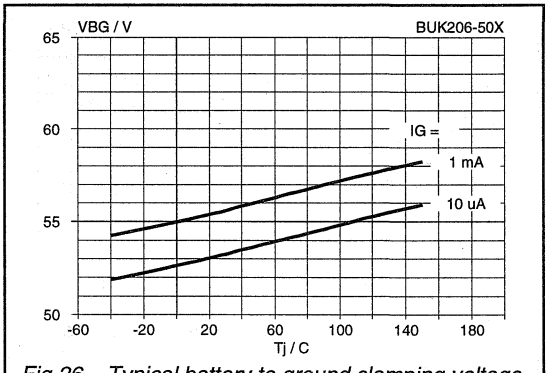


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

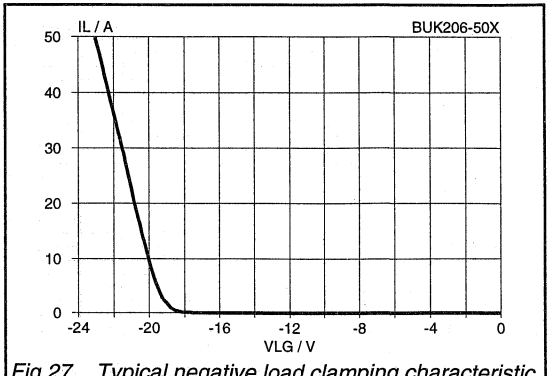


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

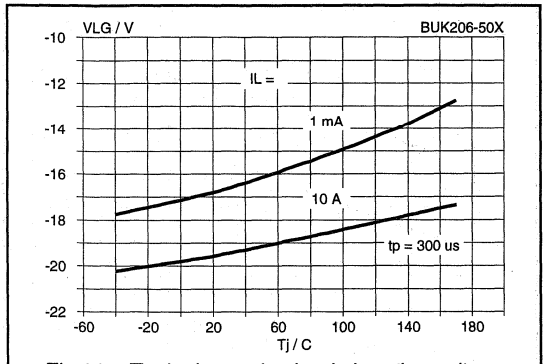


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

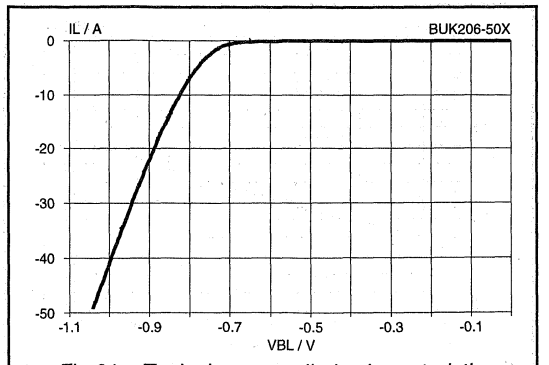


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

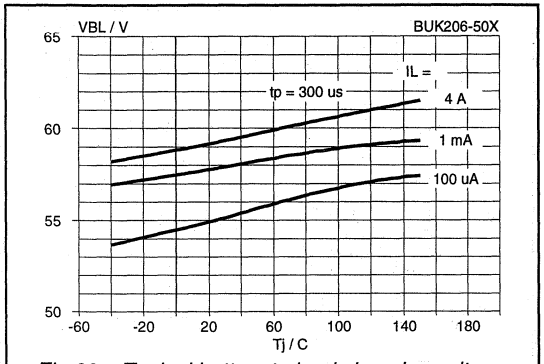


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

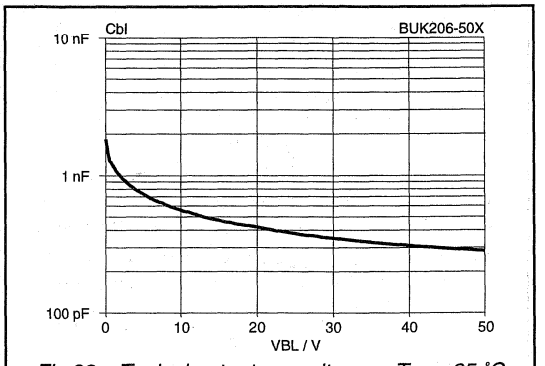


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

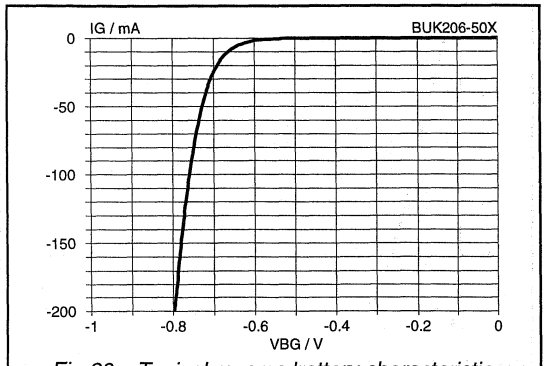


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

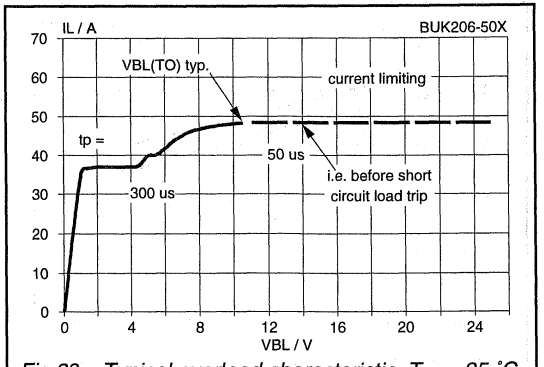


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

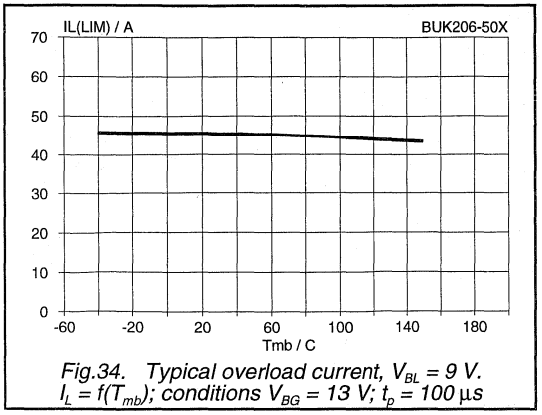


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

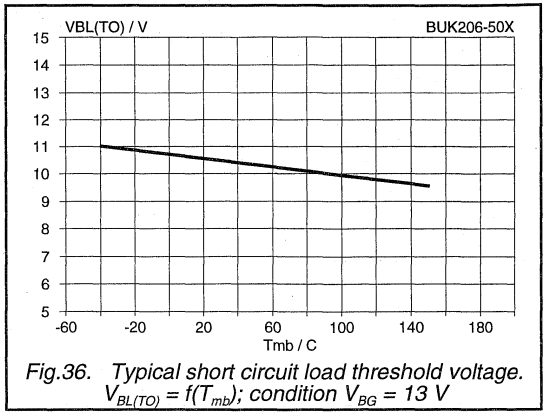


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

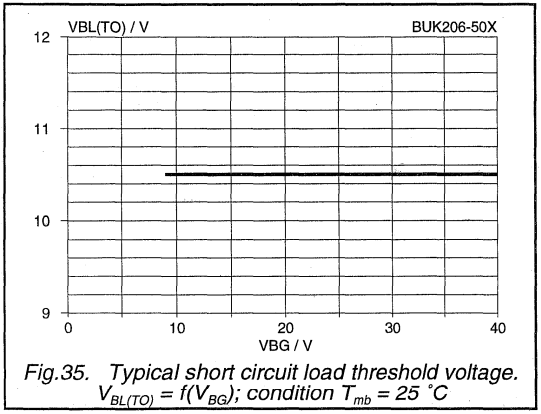


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

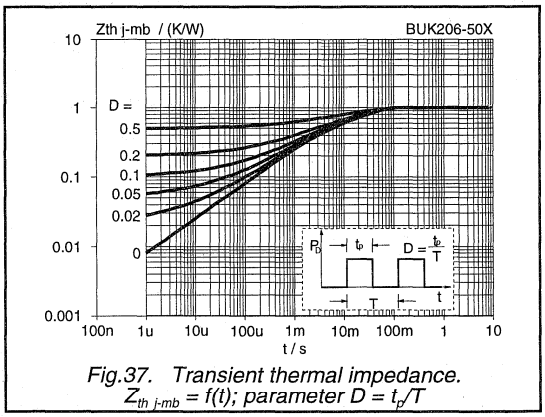


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch
SMD version of BUK202-50Y

BUK206-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	9	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	20	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	38	mΩ

FUNCTIONAL BLOCK DIAGRAM

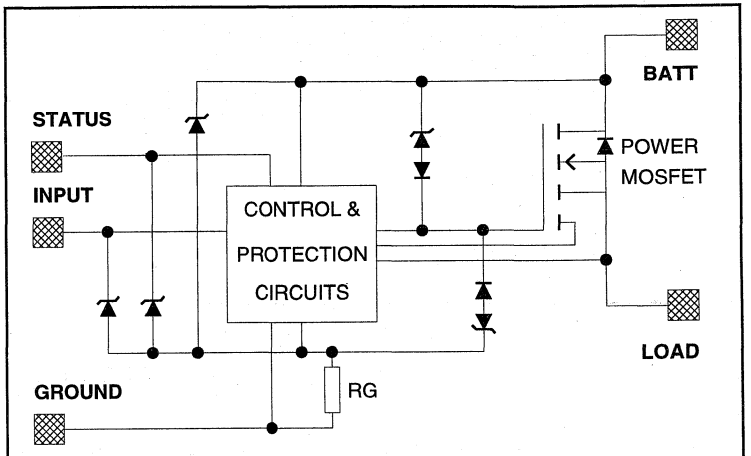


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

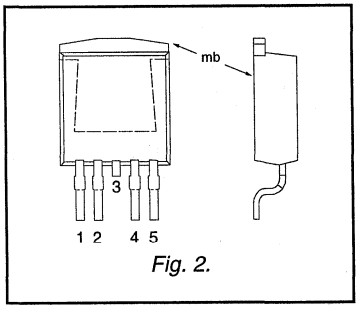


Fig. 2.

SYMBOL

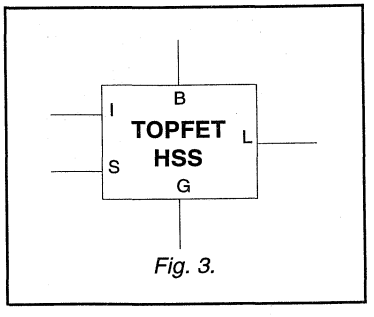


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110\ ^\circ C$	-	20	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	125	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.7	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	0.8	1	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	9	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 10 A; t_p = 300 µs	-	28	38	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 2 A; t_p = 300 µs	-	36	48	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the supply when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the supply with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	150	450	750	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 230 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 10 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq$ 10 mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	50	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	34	45	64	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	0.7	2	V/µs
t_{on}	Total switching time	to 90% V_L	-	140	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	40	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	0.7	2	V/µs
t_{off}	Total switching time	to 10% V_L	-	70	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	500	700	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

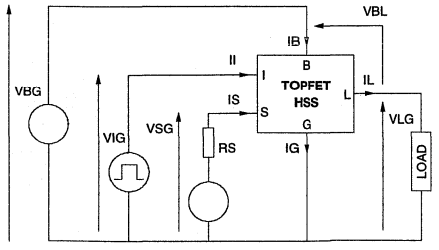


Fig.4. High side switch measurements schematic. (current and voltage conventions)

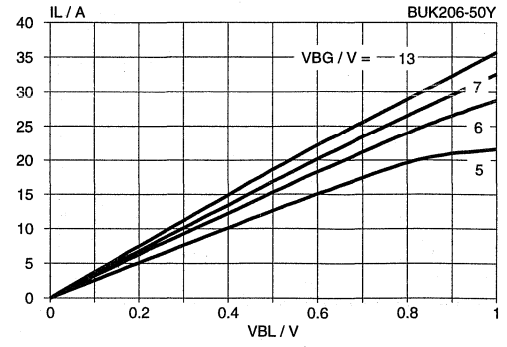


Fig.7. Typical on-state characteristics, T_j = 25 °C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

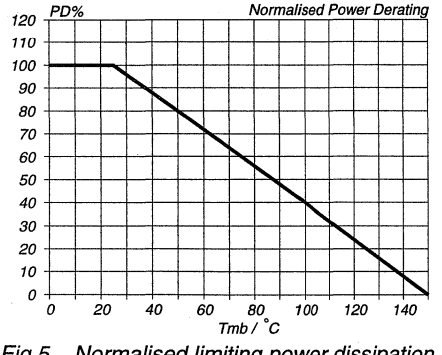


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ °C) = f(T_{mb})$

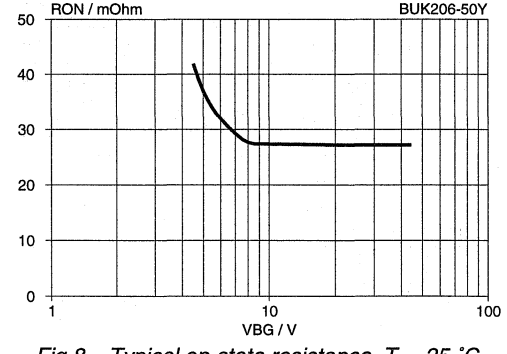


Fig.8. Typical on-state resistance, T_j = 25 °C. $R_{ON} = f(V_{BG})$; conditions: I_L = 10 A; t_p = 300 µs

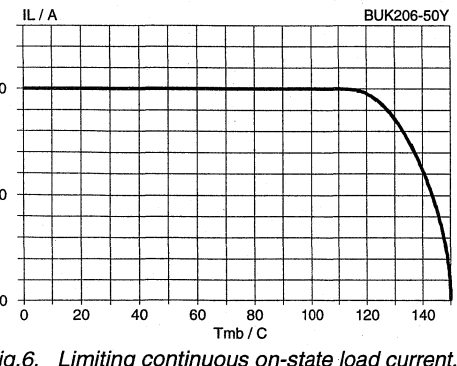


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

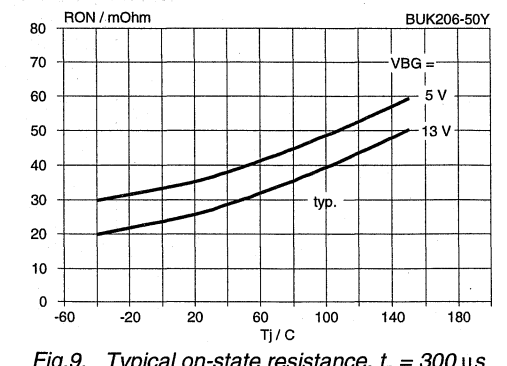


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 2 A

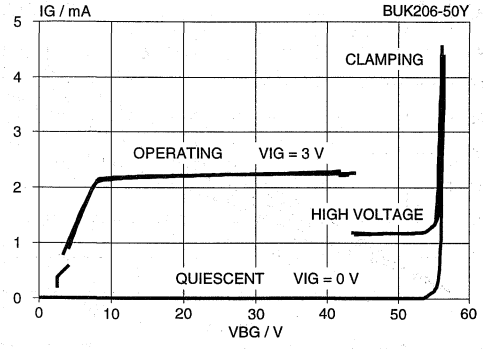


Fig.10. Typical supply characteristics, 25 °C.
$I_G = f(V_{BG})$; parameter V_{IG}

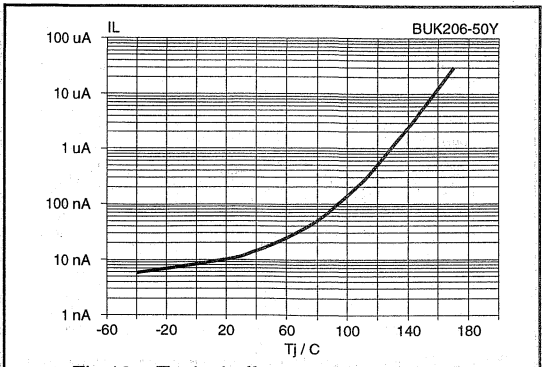


Fig.13. Typical off-state leakage current.
$I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

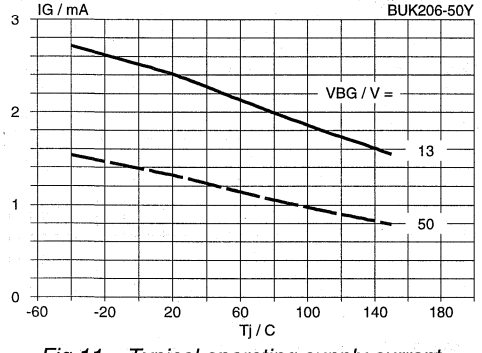


Fig.11. Typical operating supply current.
$I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

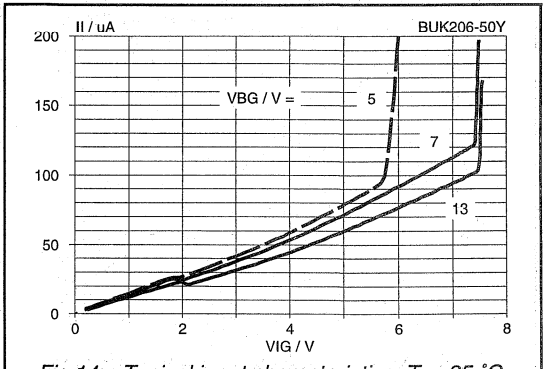


Fig.14. Typical input characteristics, T_j = 25 °C.
$I_I = f(V_{IG})$; parameter V_{BG}

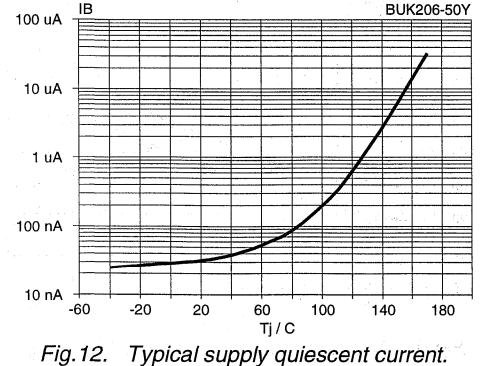


Fig.12. Typical supply quiescent current.
$I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

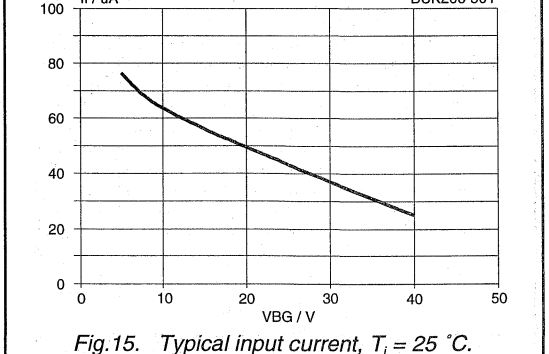


Fig.15. Typical input current, T_j = 25 °C.
$I_I = f(V_{BG})$; condition V_{IG} = 5 V

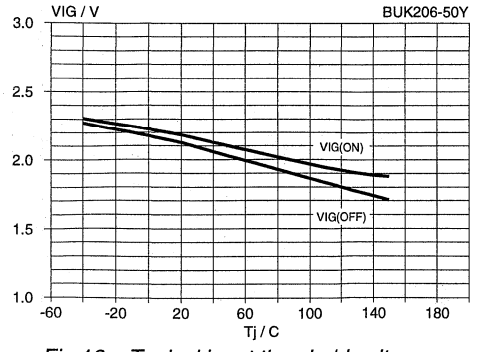


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions $V_{BG} = 13$ V, $I_L = 100$ mA

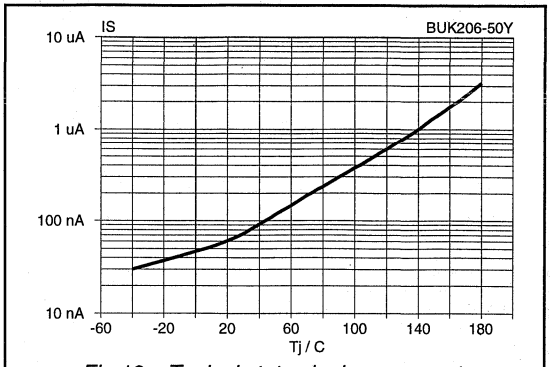


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions $V_{SG} = 5$ V, $V_{IG} = V_{BG} = 0$ V

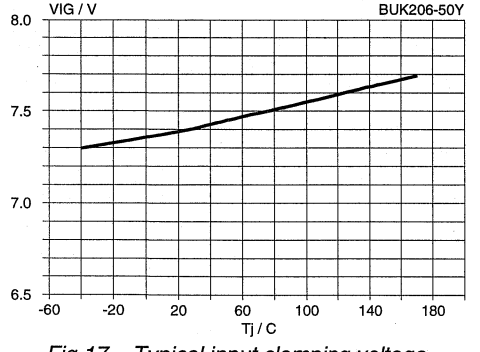


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions $I_I = 200$ µA, $V_{BG} = 13$ V

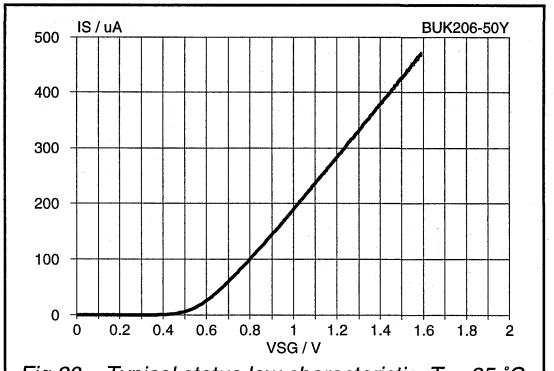


Fig.20. Typical status low characteristic, $T_j = 25$ °C. $I_S = f(V_{SG})$; conditions $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

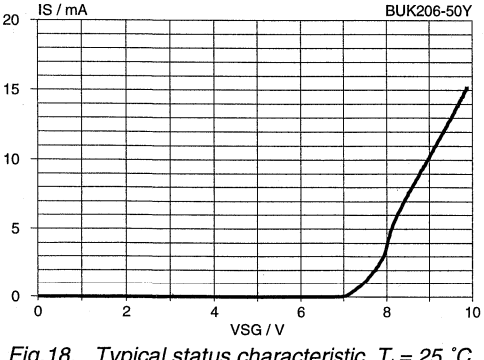


Fig.18. Typical status characteristic, $T_j = 25$ °C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG} = 0$ V

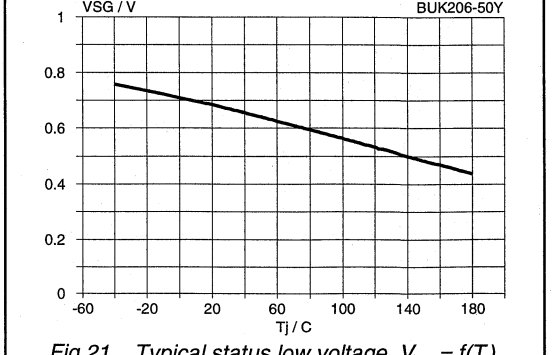


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions $I_S = 50$ µA, $V_{IG} = 5$ V, $V_{BG} = 13$ V, $I_L = 0$ A

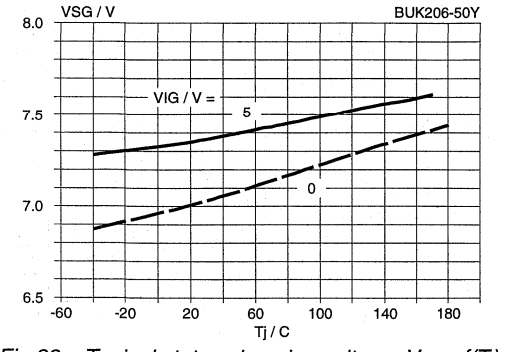


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100$ µA, $V_{BG} = 13$ V

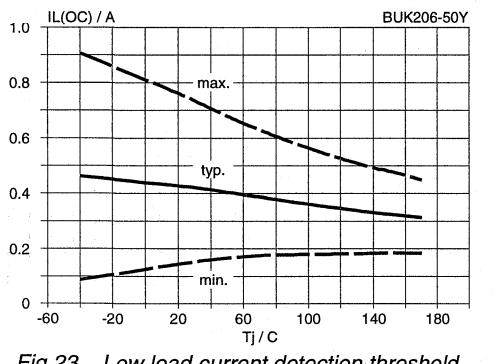


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5$ V; $V_{BG} = 13$ V

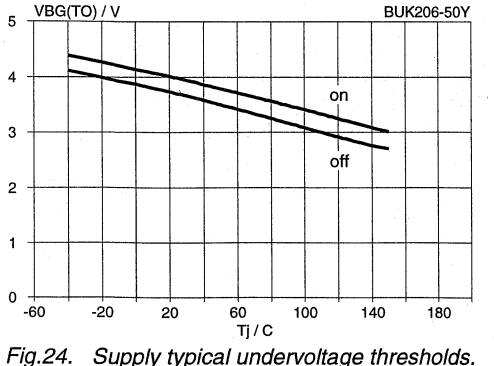


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3$ V; $I_L = 100$ mA

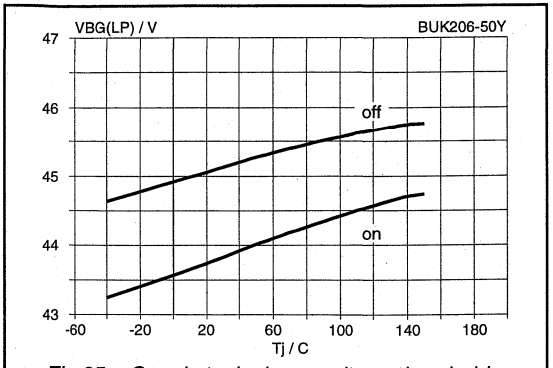


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5$ V; $I_L = 100$ mA

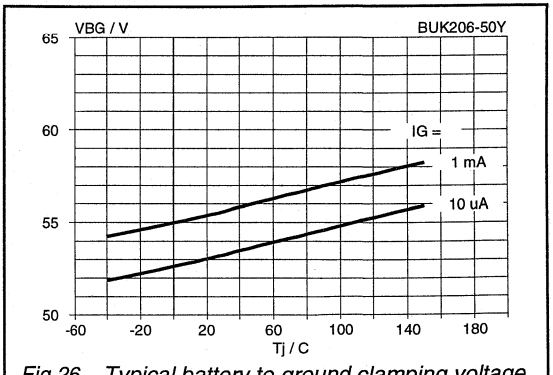


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

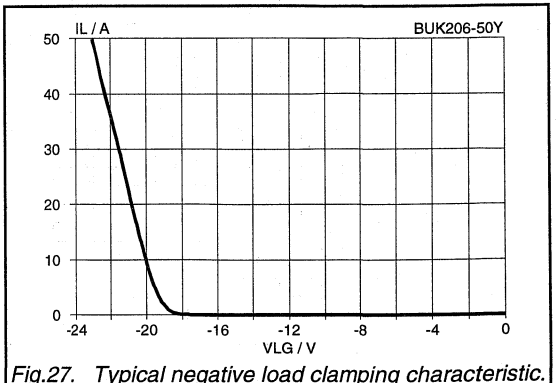


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0$ V, $t_p = 300$ µs, 25 °C

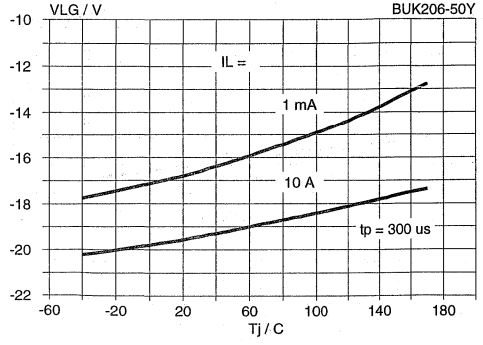


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

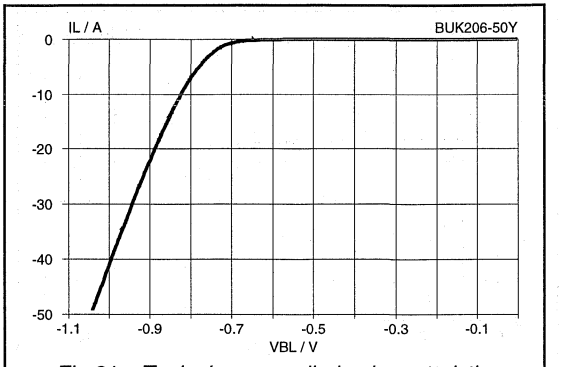


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

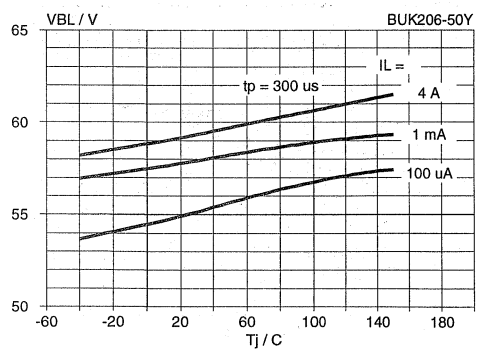


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

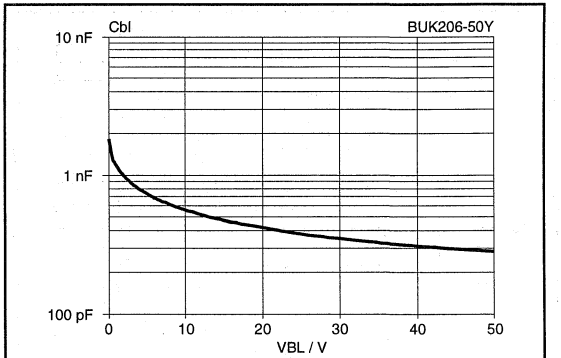


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

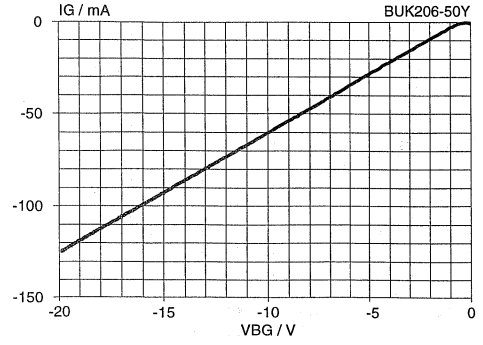


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

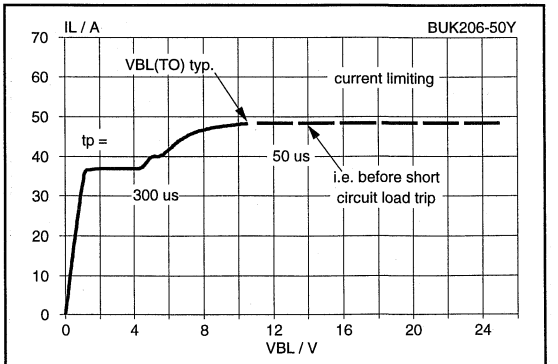


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

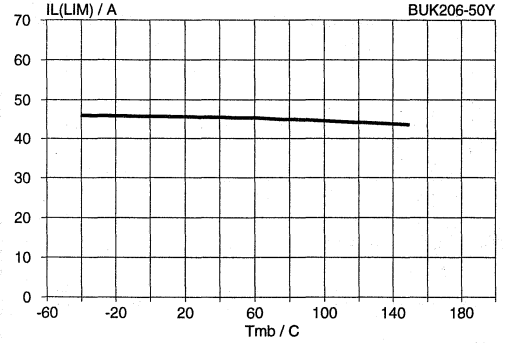


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

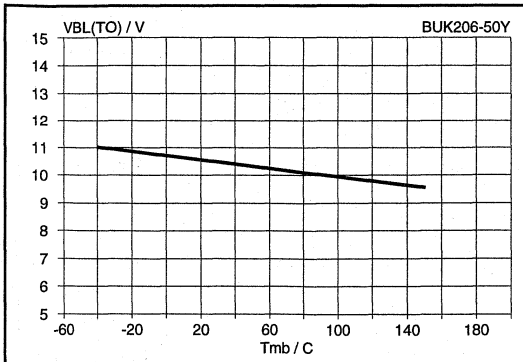


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

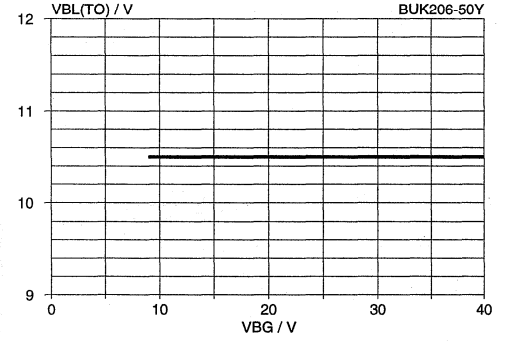


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

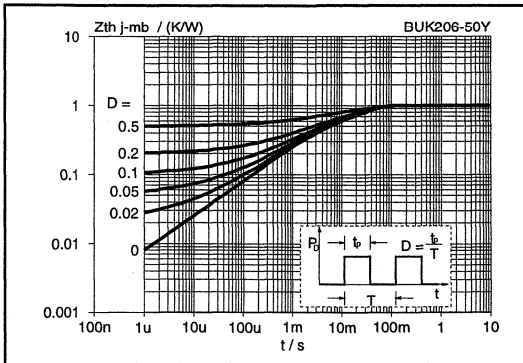


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch
SMD version of BUK203-50X

BUK207-50X

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input with hysteresis
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection with external ground resistor

FUNCTIONAL BLOCK DIAGRAM

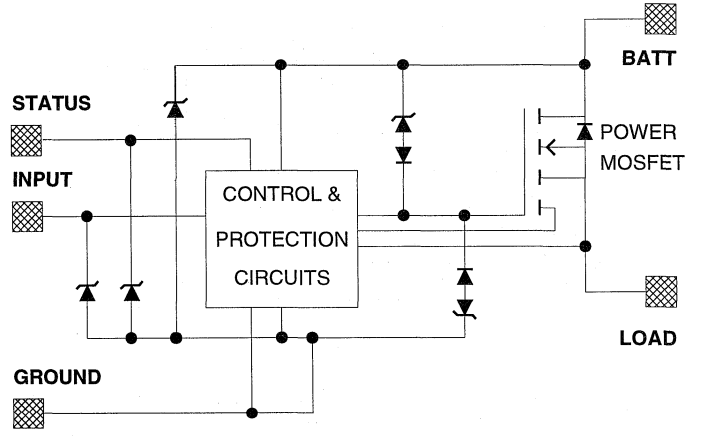


Fig.1. Elements of the TOPFET HSS.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

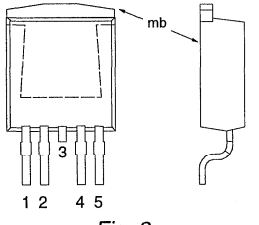


Fig. 2.

SYMBOL

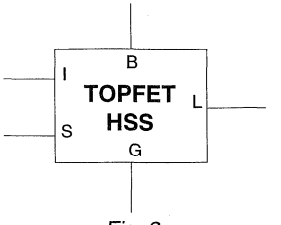


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_G \geq 150\ \Omega$; $R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110$ °C	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25$ °C	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150$ °C prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7	8	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.4	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	1.7	-	V
ΔV_{IG}	Input turn-on hysteresis		-	0.4	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	9	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.5 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.1 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time	V_{IG} = 5 V	-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	17	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	12	15	22	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

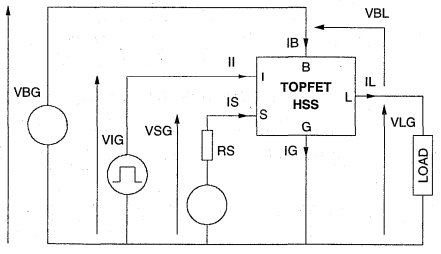


Fig.4. High side switch measurements schematic. (current and voltage conventions)

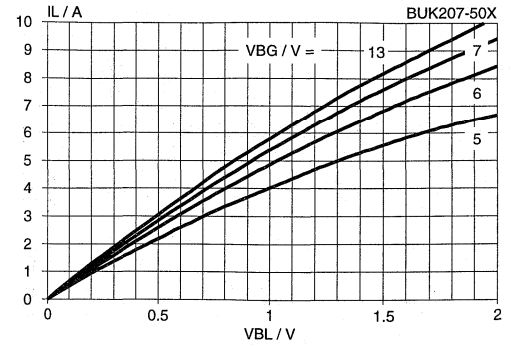


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

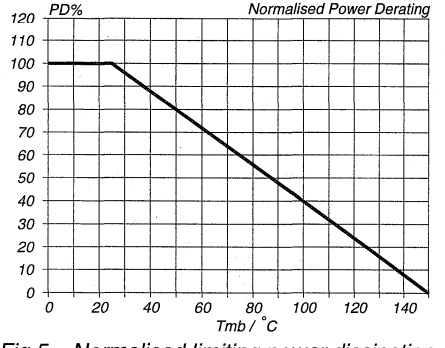


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

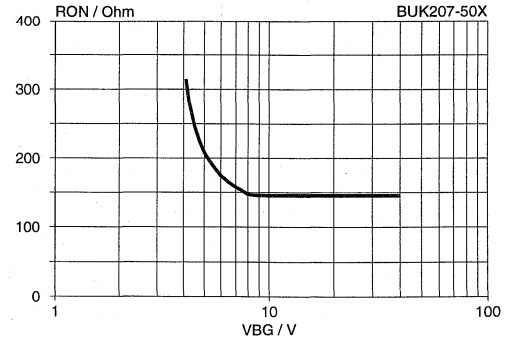


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

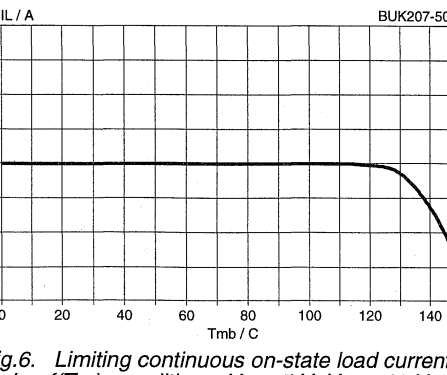


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

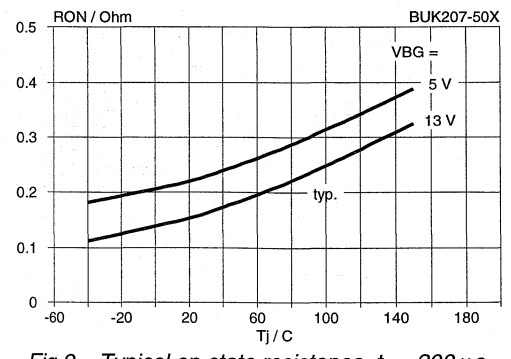


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

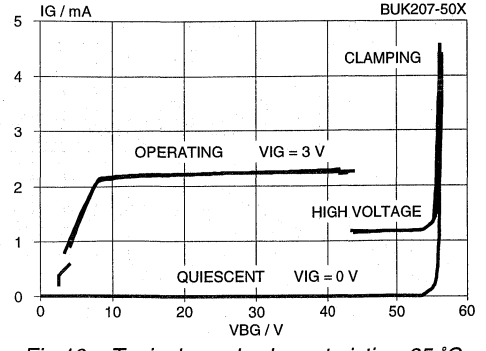


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

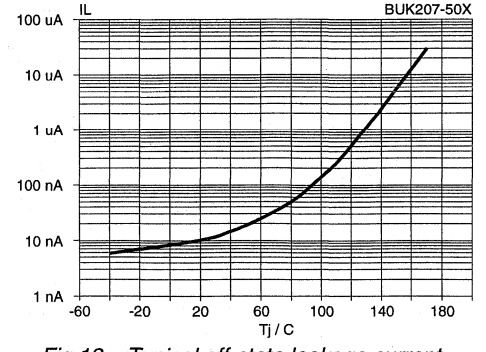


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

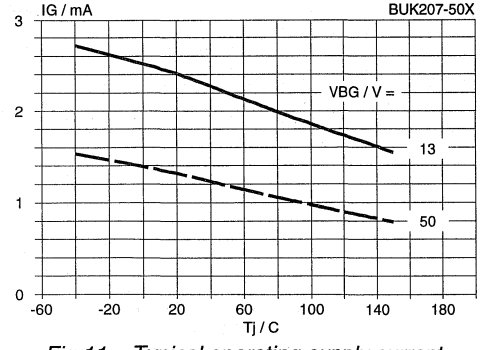


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

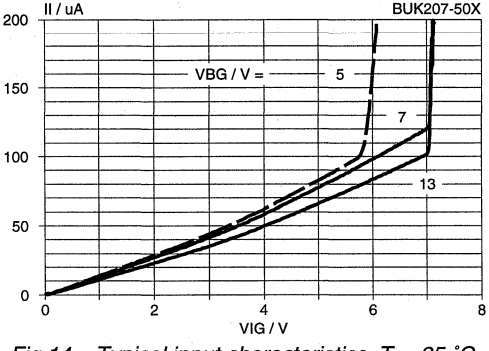


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

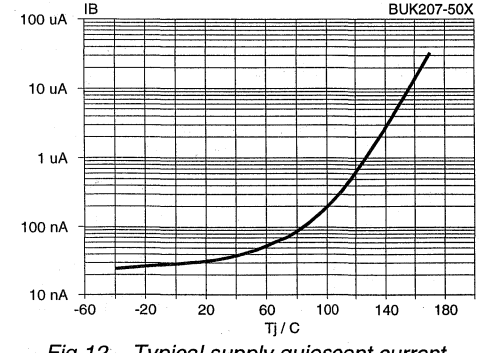


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

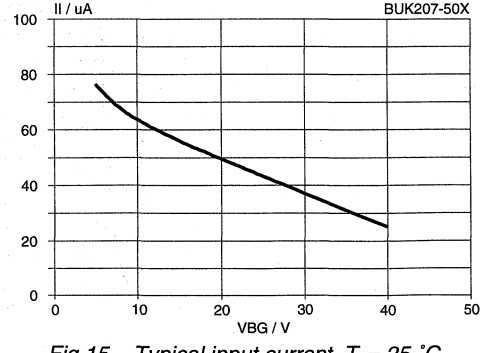


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

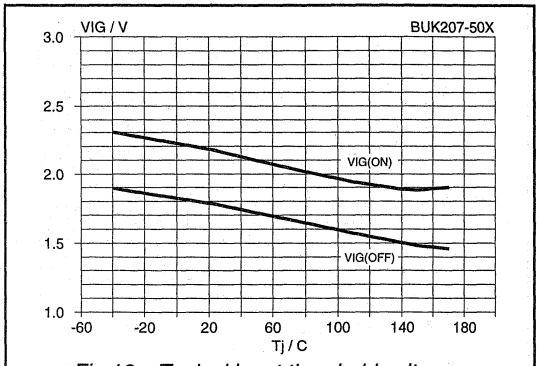


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

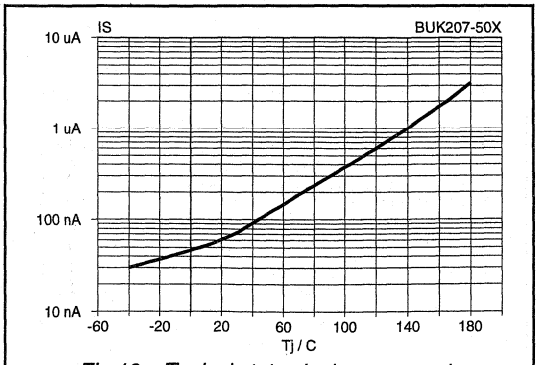


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

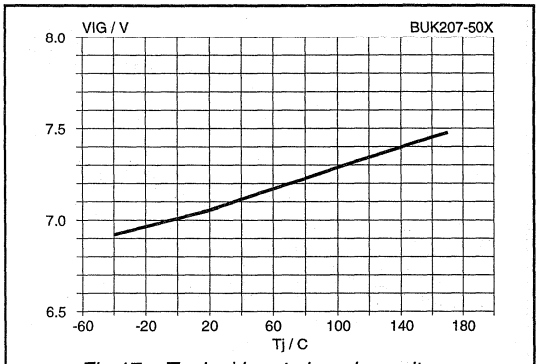


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

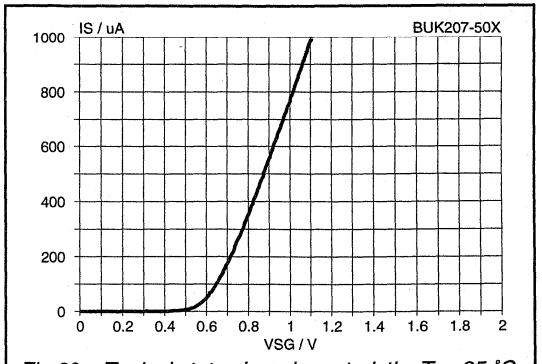


Fig.20. Typical status low characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

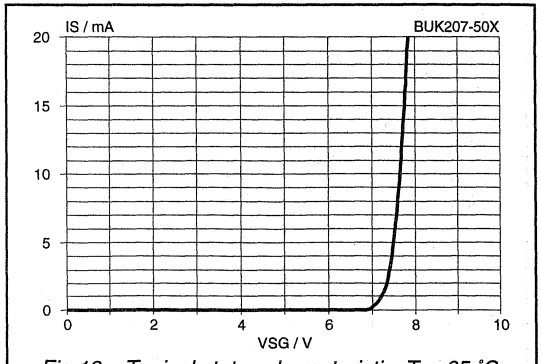


Fig.18. Typical status characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

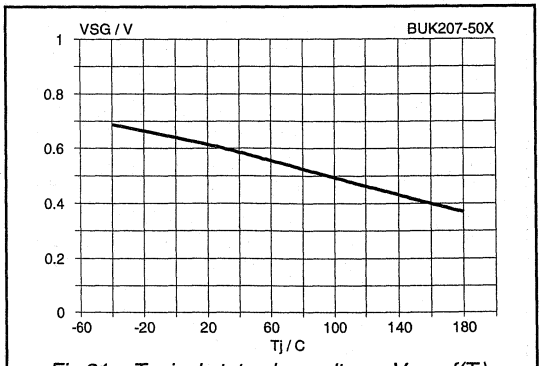


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

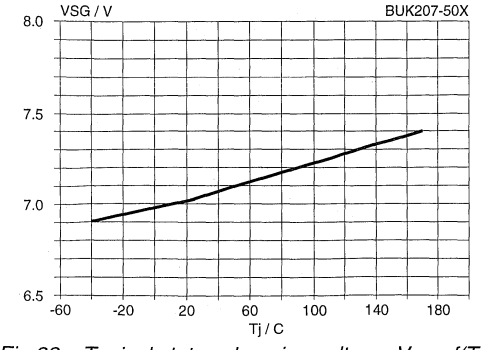


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

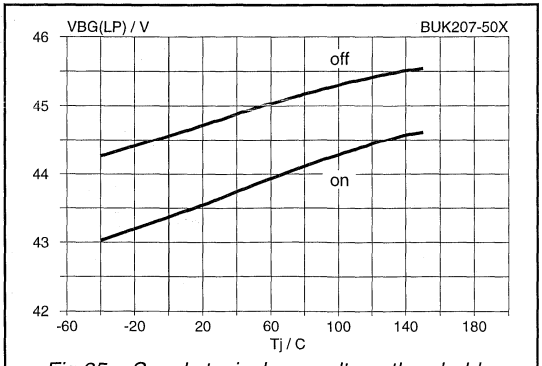


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

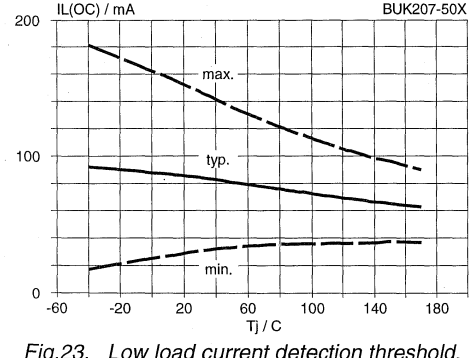


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

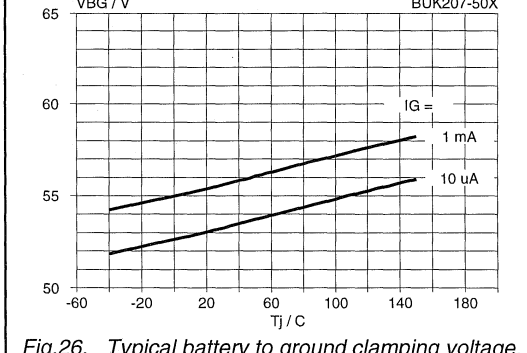


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

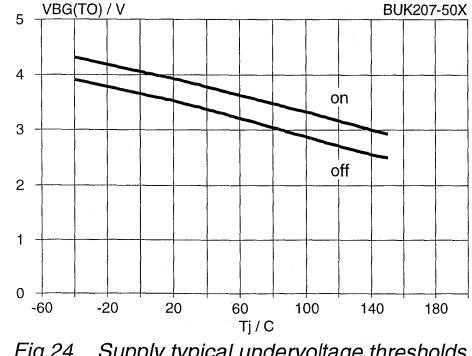


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

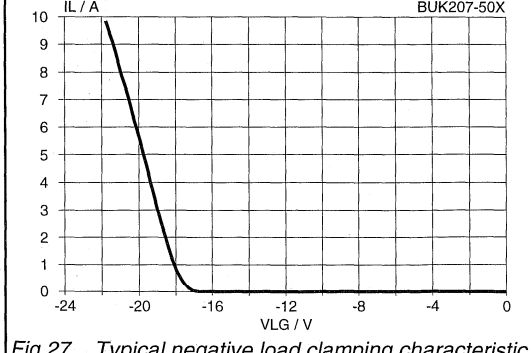


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 ˚C

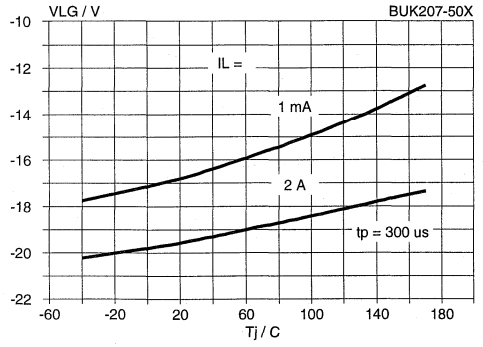


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

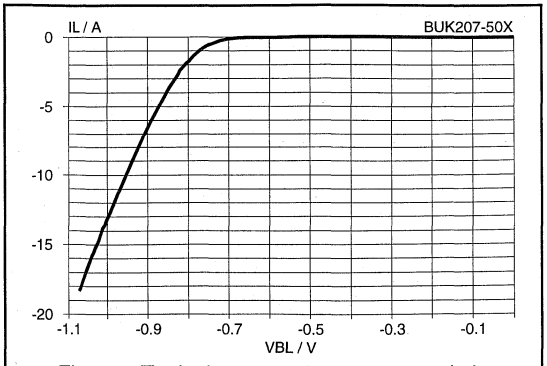


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ ˚C

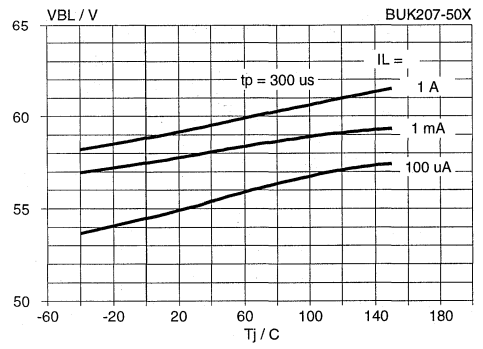


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

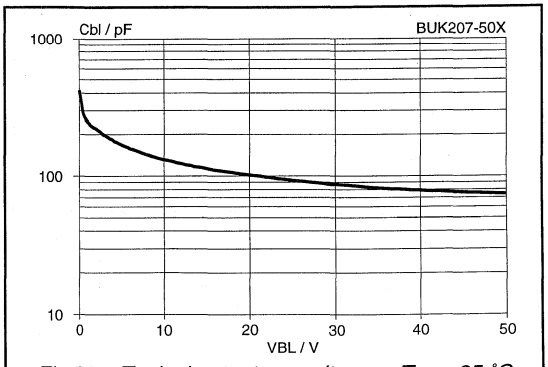


Fig.32. Typical output capacitance. $T_{mb} = 25$ ˚C $C_{bl} = f(V_{BL})$; conditions f = 1 MHz, $V_{IG} = 0$ V

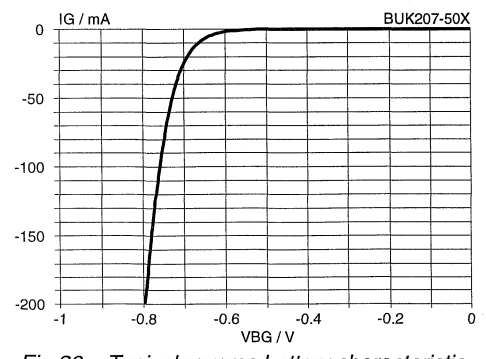


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ ˚C

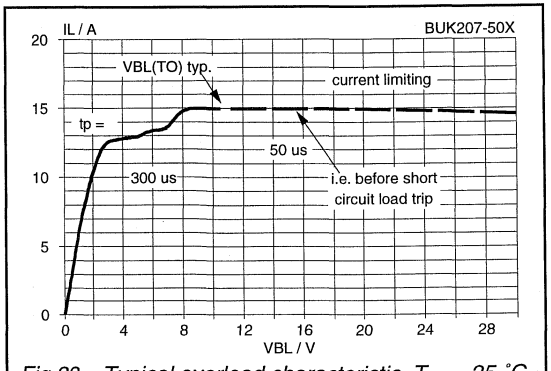


Fig.33. Typical overload characteristic, $T_{mb} = 25$ ˚C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

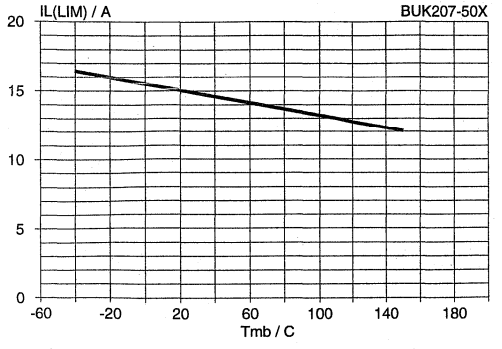


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

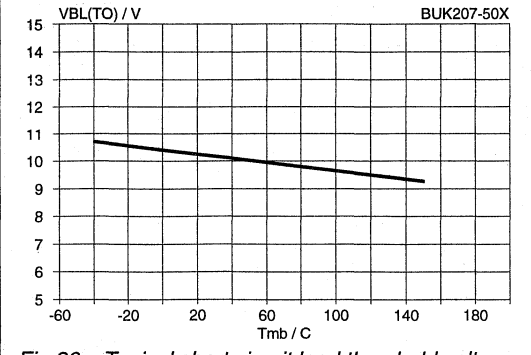


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

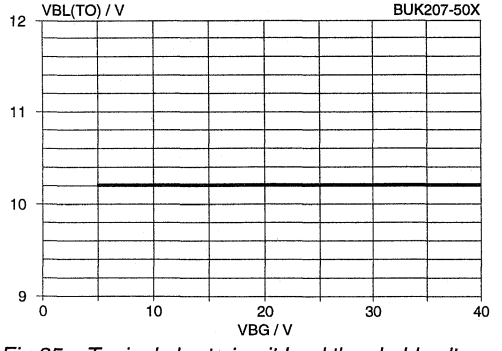


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

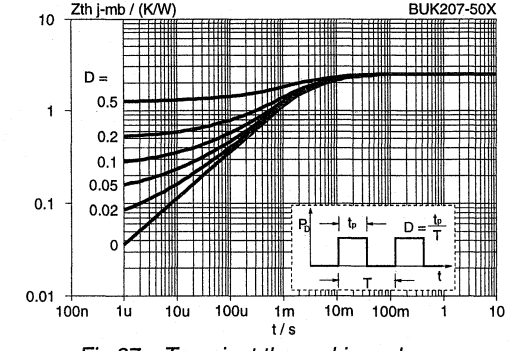


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

TOPFET high side switch SMD version of BUK203-50Y

BUK207-50Y

DESCRIPTION

Monolithic temperature and overload protected power switch based on MOSFET technology in a 5 pin plastic surface mount envelope, configured as a single high side switch.

APPLICATIONS

General controller for driving lamps, motors, solenoids, heaters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	UNIT
I_L	Nominal load current (ISO)	1.6	A
SYMBOL	**PARAMETER**	**MAX.**	**UNIT**
V_{BG}	Continuous off-state supply voltage	50	V
I_L	Continuous load current	4	A
T_j	Continuous junction temperature	150	°C
R_{ON}	On-state resistance	220	mΩ

FEATURES

- Vertical power DMOS switch
- Low on-state resistance
- 5 V logic compatible input
- Overtemperature protection - self resets with hysteresis
- Overload protection against short circuit load with output current limiting; latched - reset by input
- High supply voltage load protection
- Supply undervoltage lock out
- Status indication for overload protection activated
- Diagnostic status indication of open circuit load
- Very low quiescent current
- Voltage clamping for turn off of inductive loads
- ESD protection on all pins
- Reverse battery and overvoltage protection

FUNCTIONAL BLOCK DIAGRAM

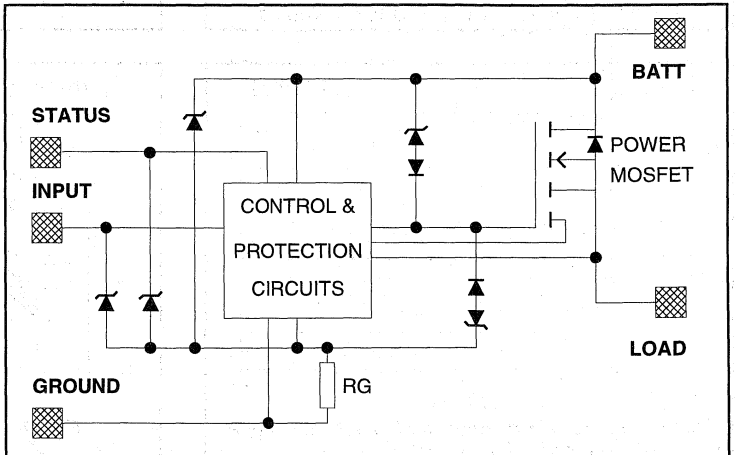


Fig.1. Elements of the TOPFET HSS with internal ground resistor.

PINNING - SOT426

PIN	DESCRIPTION
1	Ground
2	Input
3	(connected to mb)
4	Status
5	Load
mb	Battery

PIN CONFIGURATION

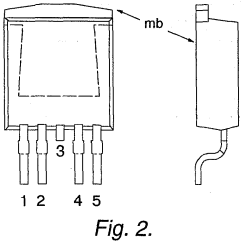


Fig. 2.

SYMBOL

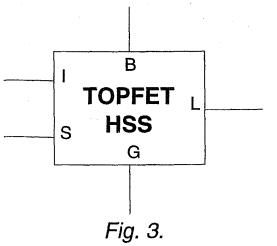


Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
	Battery voltages				
V_{BG}	Continuous off-state supply voltage	-	0	50	V
	Reverse battery voltages[1]	External resistors:			
$-V_{BG}$	Repetitive peak supply voltage	$R_I = R_S \geq 4.7\ k\Omega$, $\delta \leq 0.1$	-	32	V
$-V_{BG}$	Continuous reverse supply voltage	$R_I = R_S \geq 4.7\ k\Omega$	-	16	V
I_L	Continuous load current	$T_{mb} \leq 110\ ^\circ C$	-	4	A
P_D	Total power dissipation	$T_{mb} \leq 25\ ^\circ C$	-	50	W
T_{stg}	Storage temperature	-	-55	175	°C
T_j	Continuous junction temperature[2]	-	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C
	Input and status				
I_I	Continuous input current	-	-5	5	mA
I_S	Continuous status current	-	-5	5	mA
I_I	Repetitive peak input current	$\delta \leq 0.1$	-20	20	mA
I_S	Repetitive peak status current	$\delta \leq 0.1$	-20	20	mA
	Inductive load clamping				
E_{BL}	Non-repetitive clamping energy	$T_{mb} = 150\ ^\circ C$ prior to turn-off	-	1.4	J

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance[3]					
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	2	2.5	K/W

1 Reverse battery voltage is allowed only with external input and status resistors to limit the currents to a safe value.

2 For normal continuous operation. A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 Of the output Power MOS transistor.

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Clamping voltages					
V_{BG}	Battery to ground	I_G = 1 mA	50	55	65	V
V_{BL}	Battery to load	$I_L = I_G$ = 1 mA	50	55	65	V
$-V_{LG}$	Negative load to ground	I_L = 1 mA	12	17	21	V
	Supply voltage	battery to ground				
V_{BG}	Operating range[1]	-	5	-	40	V
	Currents	V_{BG} = 13 V				
I_L	Nominal load current[2]	V_{BL} = 0.5 V; T_{mb} = 85 °C	1.6	-	-	A
I_B	Quiescent current[3]	V_{IG} = 0 V; V_{LG} = 0 V	-	0.1	2	µA
I_G	Operating current[4]	V_{IG} = 5 V; I_L = 0 A	1.5	2.2	4	mA
I_L	Off-state load current[5]	V_{BL} = 13 V; V_{IG} = 0 V	-	0.1	1	µA
	Resistances					
R_{ON}	On-state resistance[6]	V_{BG} = 13 V; I_L = 2 A; t_p = 300 µs	-	160	220	mΩ
R_{ON}	On-state resistance	V_{BG} = 5 V; I_L = 0.5 A; t_p = 300 µs	-	225	320	mΩ
R_G	Internal ground resistance	I_G = 10 mA	-	150	-	Ω

INPUT CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	Input current	V_{IG} = 5 V	35	60	100	µA
V_{IG}	Input clamping voltage	I_I = 200 µA	6	7.5	8.5	V
$V_{IG(ON)}$	Input turn-on threshold voltage		-	2.1	2.7	V
$V_{IG(OFF)}$	Input turn-off threshold voltage		1.5	2	-	V

1 On-state resistance is increased if the supply voltage is less than 9 V. Refer to figure 8.

2 Defined as in ISO 10483-1.

3 This is the continuous current drawn from the battery when the input is low and includes leakage current to the load.

4 This is the continuous current drawn from the battery with no load connected, but with the input high.

5 The measured current is in the load pin only.

6 The supply and input voltage for the R_{ON} tests are continuous. The specified pulse duration t_p refers only to the applied load current.

PROTECTION FUNCTIONS AND STATUS INDICATIONS

Truth table for normal, open-circuit load and overload conditions and abnormal supply voltages.

FUNCTIONS		TRUTH TABLE			THRESHOLD			
SYMBOL	CONDITION	INPUT	STATUS	OUTPUT	MIN.	TYP.	MAX.	UNIT
	Normal on-state	1	1	1				
	Normal off-state	0	1	0				
$I_{L(OC)}$	Open circuit load[1]	1	0	1	30	90	150	mA
	Open circuit load	0	1	0				
$T_{j(TO)}$	Over temperature[2]	1	0	0	150	175	-	°C
	Over temperature[3]	0	0	0				
$V_{BL(TO)}$	Short circuit load[4]	1	0	0	9	10.5	12	V
	Short circuit load	0	1	0				
$V_{BG(TO)}$	Low supply voltage[5]	X	1	0	3	4	5	V
$V_{BG(LP)}$	High supply voltage[6]	X	1	0	40	45	50	V

For input '0' equals low, '1' equals high, 'X' equals don't care.
For status '0' equals low, '1' equals open or high.
For output switch '0' equals off, '1' equals on.

STATUS CHARACTERISTICS

T_{mb} = 25 °C.
The status output is an open drain transistor, and requires an external pull-up circuit to indicate a logic high.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SG}	Status clamping voltage	I_S = 100 µA; V_{IG} = 0 V	6	7	8	V
V_{SG}	Status low voltage	I_S = 50 µA; V_{BG} = 13 V; V_{IG} = 5 V	-	0.7	0.8	V
I_S	Status leakage current	V_{SG} = 5 V	-	0.1	1	µA
I_S	Status saturation current[7]	V_{SS} = 5 V; R_S = 0 Ω; V_{BG} = 13 V	-	5	-	mA
	Application information					
R_S	External pull-up resistor[8]	V_{SS} = 5 V	-	100	-	kΩ

1 In the on-state, the switch detects whether the load current is less than the quoted open load threshold current. This is for status indication only. Typical hysteresis equals 25 mA. The thresholds are specified for supply voltage within the normal working range.

2 After cooling below the reset temperature the switch will resume normal operation. The reset temperature is lower than the trip temperature by typically 10 °C.

3 If the overtemperature protection has operated, status remains low to indicate the overtemperature condition even if the input is taken low, providing the device has not cooled below the reset temperature.

4 After short circuit protection has operated, the input voltage must be toggled low for the switch to resume normal operation.

5 Undervoltage sensor causes the device to switch off. Typical hysteresis equals 0.7 V.

6 Overvoltage sensor causes the device to switch off to protect the load. Typical hysteresis equals 1.3 V.

7 In a fault condition with the pull-up resistor short circuited while the status transistor is conducting.

8 The pull-up resistor also protects the status pin during reverse battery conditions.

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C; V_{BG} = 13 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Inductive load turn-off					
$-V_{LG}$	Negative load voltage[1]	V_{IG} = 0 V; I_L = 2 A; t_p = 300 µs	15	20	25	V
	Short circuit load protection[2]	V_{IG} = 5 V; $R_L \leq 10$ mΩ				
$t_{d\,sc}$	Response time		-	75	-	µs
I_L	Load current prior to turn-off	$t < t_{d\,sc}$	-	17	-	A
	Overload protection[3]					
$I_{L(lim)}$	Load current limiting	V_{BL} = 9 V; t_p = 300 µs	12	15	22	A

SWITCHING CHARACTERISTICS

T_{mb} = 25 °C, V_{BG} = 13 V, for resistive load R_L = 13 Ω.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	During turn-on	to V_{IG} = 5 V				
$t_{d\,on}$	Delay time	to 10% V_L	-	16	-	µs
dV/dt_{on}	Rate of rise of load voltage		-	1.3	3	V/µs
t_{on}	Total switching time	to 90% V_L	-	40	-	µs
	During turn-off	to V_{IG} = 0 V				
$t_{d\,off}$	Delay time	to 90% V_L	-	20	-	µs
dV/dt_{off}	Rate of fall of load voltage		-	1.6	3	V/µs
t_{off}	Total switching time	to 10% V_L	-	35	-	µs

CAPACITANCES

T_{mb} = 25 °C; f = 1 MHz; V_{IG} = 0 V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ig}	Input capacitance	V_{BG} = 13 V	-	15	20	pF
C_{bl}	Output capacitance	$V_{BL} = V_{BG}$ = 13 V	-	120	170	pF
C_{sg}	Status capacitance	V_{SG} = 5 V	-	11	15	pF

1 For a high side switch, the load pin voltage goes negative with respect to ground during the turn-off of an inductive load. This negative voltage is clamped by the device.

2 The load current is self-limited during the response time for short circuit load protection. Response time is measured from when input goes high.

3 If the load resistance is low, but not a complete short circuit, such that the on-state voltage remains less than $V_{BL(TO)}$, the device remains in current limiting until the overtemperature protection operates.

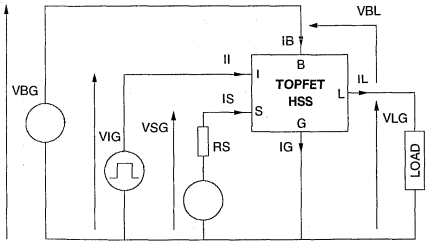


Fig.4. High side switch measurements schematic. (current and voltage conventions)

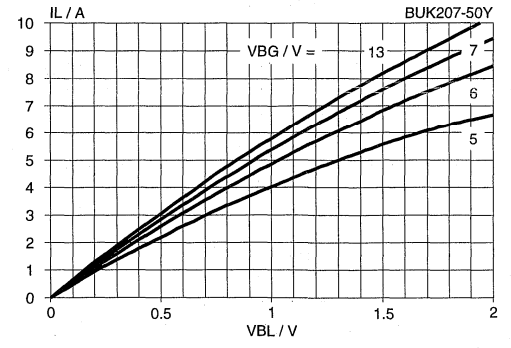


Fig.7. Typical on-state characteristics, T_j = 25 ˚C. $I_L = f(V_{BL})$; parameter V_{BG}; t_p = 250 µs

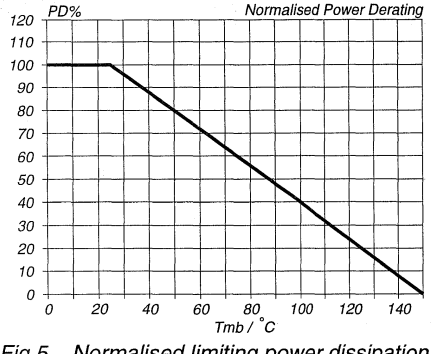


Fig.5. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

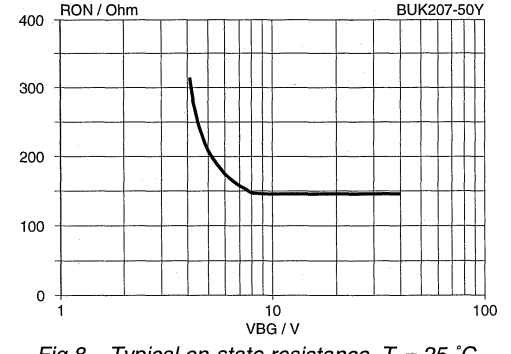


Fig.8. Typical on-state resistance, T_j = 25 ˚C. $R_{ON} = f(V_{BG})$; conditions: I_L = 2 A; t_p = 300 µs

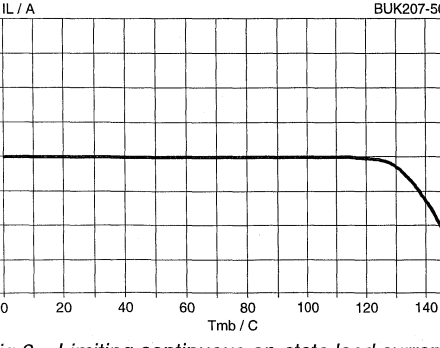


Fig.6. Limiting continuous on-state load current. $I_L = f(T_{mb})$; conditions: V_{IG} = 5 V, V_{BG} = 13 V

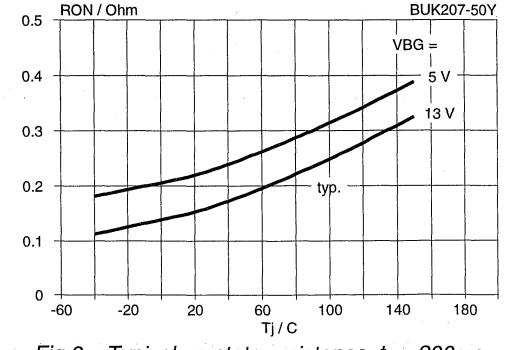


Fig.9. Typical on-state resistance, t_p = 300 µs. $R_{ON} = f(T_j)$; parameter V_{BG}; condition I_L = 0.5 A

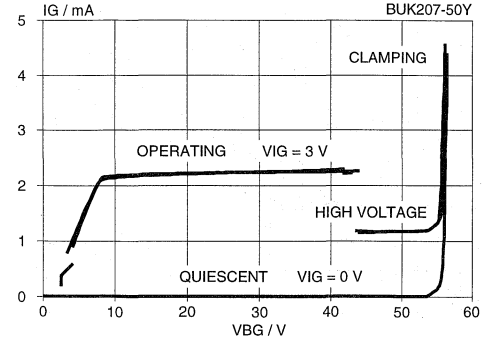


Fig.10. Typical supply characteristics, 25 ˚C. $I_G = f(V_{BG})$; parameter V_{IG}

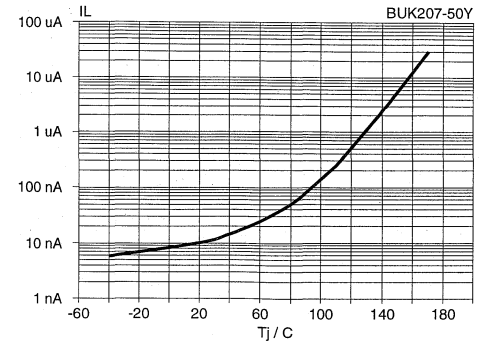


Fig.13. Typical off-state leakage current. $I_L = f(T_j)$; conditions: V_{BL} = 13 V = V_{BG}; V_{IG} = 0 V.

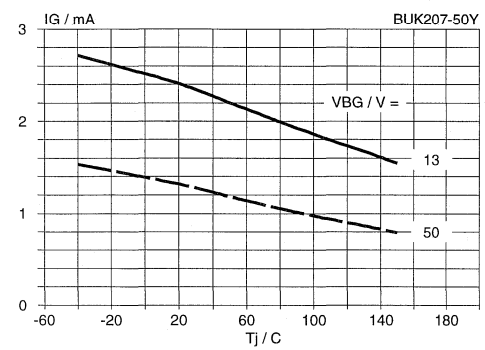


Fig.11. Typical operating supply current. $I_G = f(T_j)$; parameter V_{BG}; condition V_{IG} = 5 V

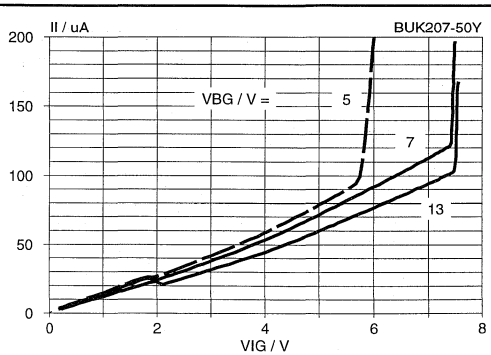


Fig.14. Typical input characteristics, T_j = 25 ˚C. $I_I = f(V_{IG})$; parameter V_{BG}

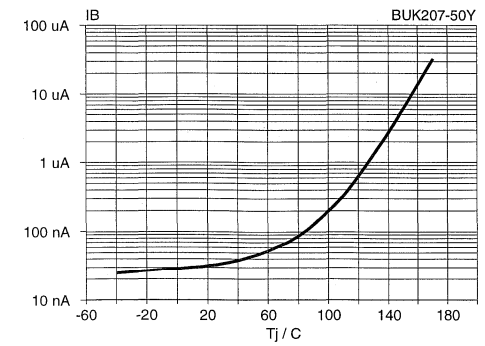


Fig.12. Typical supply quiescent current. $I_B = f(T_j)$; condition V_{BG} = 13 V, V_{IG} = 0 V, V_{LG} = 0 V

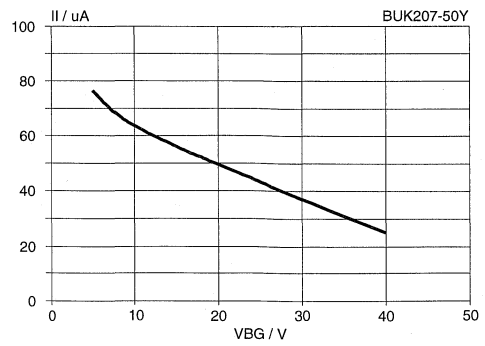


Fig.15. Typical input current, T_j = 25 ˚C. $I_I = f(V_{BG})$; condition V_{IG} = 5 V

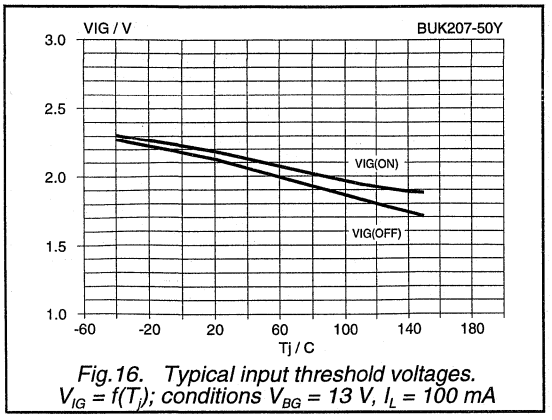


Fig.16. Typical input threshold voltages. $V_{IG} = f(T_j)$; conditions V_{BG} = 13 V, I_L = 100 mA

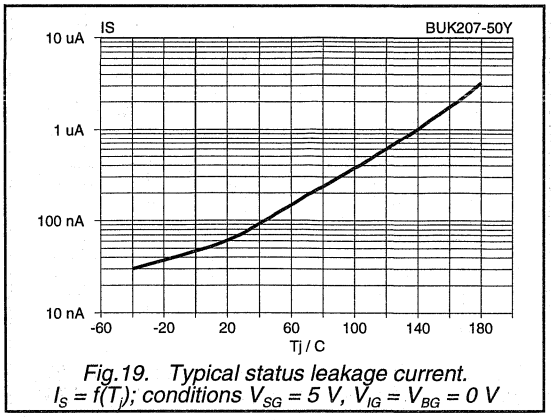


Fig.19. Typical status leakage current. $I_S = f(T_j)$; conditions V_{SG} = 5 V, $V_{IG} = V_{BG}$ = 0 V

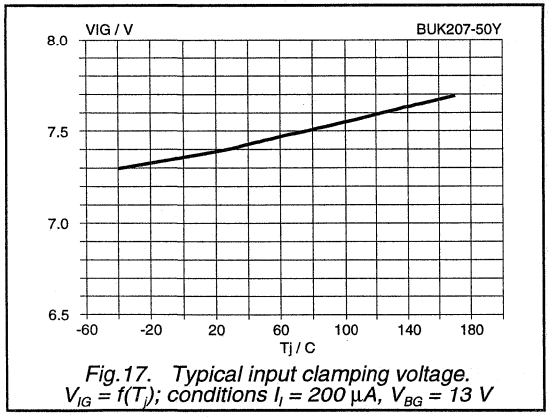


Fig.17. Typical input clamping voltage. $V_{IG} = f(T_j)$; conditions I_I = 200 µA, V_{BG} = 13 V

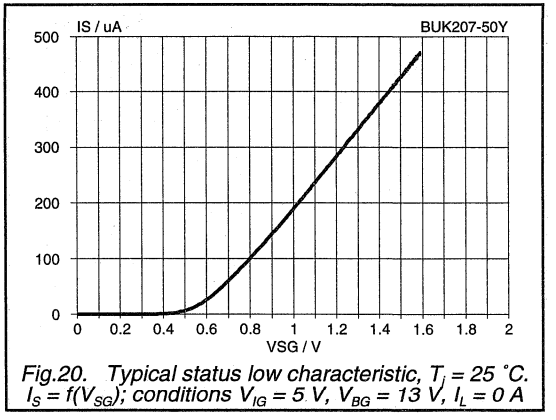


Fig.20. Typical status low characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

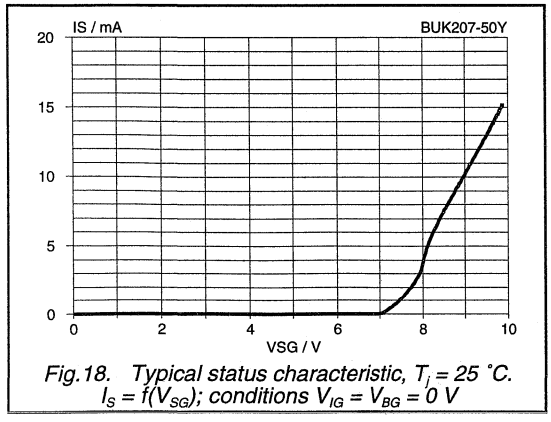


Fig.18. Typical status characteristic, T_j = 25 ˚C. $I_S = f(V_{SG})$; conditions $V_{IG} = V_{BG}$ = 0 V

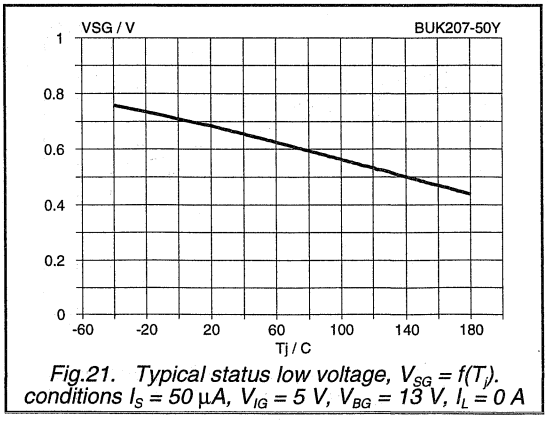


Fig.21. Typical status low voltage, $V_{SG} = f(T_j)$. conditions I_S = 50 µA, V_{IG} = 5 V, V_{BG} = 13 V, I_L = 0 A

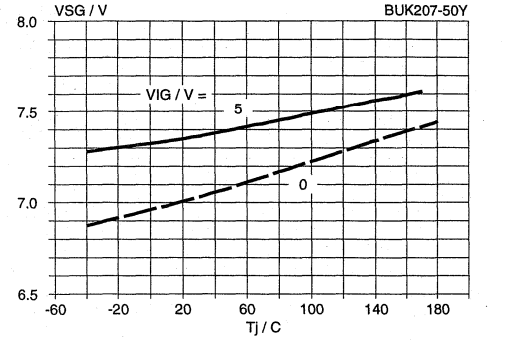


Fig.22. Typical status clamping voltage, $V_{SG} = f(T_j)$. parameter V_{IG}; conditions $I_S = 100\ \mu A$, $V_{BG} = 13\ V$

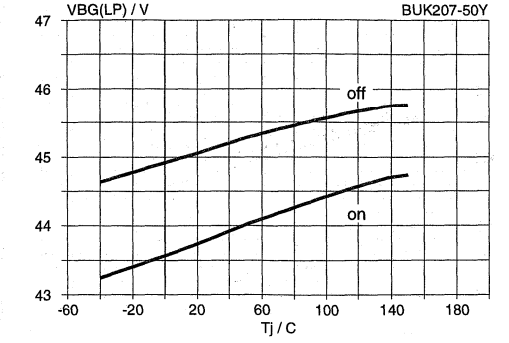


Fig.25. Supply typical overvoltage thresholds. $V_{BG(LP)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $I_L = 100\ mA$

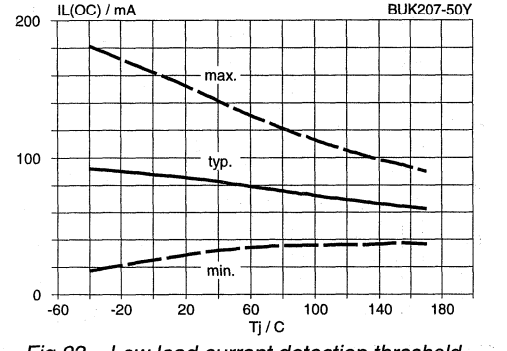


Fig.23. Low load current detection threshold. $I_{L(OC)} = f(T_j)$; conditions $V_{IG} = 5\ V$; $V_{BG} = 13\ V$

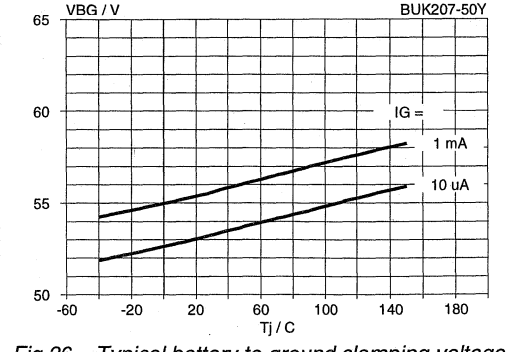


Fig.26. Typical battery to ground clamping voltage. $V_{BG} = f(T_j)$; parameter I_G

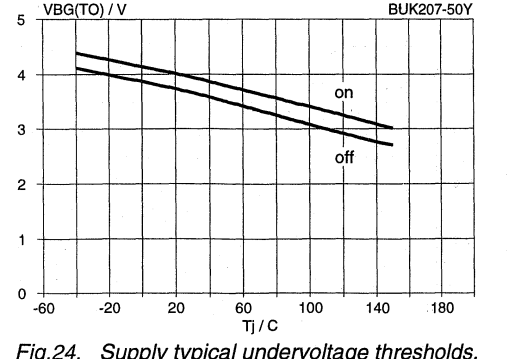


Fig.24. Supply typical undervoltage thresholds. $V_{BG(TO)} = f(T_j)$; conditions $V_{IG} = 3\ V$; $I_L = 100\ mA$

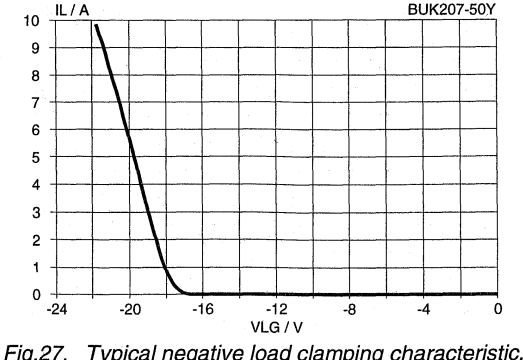


Fig.27. Typical negative load clamping characteristic. $I_L = f(V_{LG})$; conditions $V_{IG} = 0\ V$, $t_p = 300\ \mu s$, 25 °C

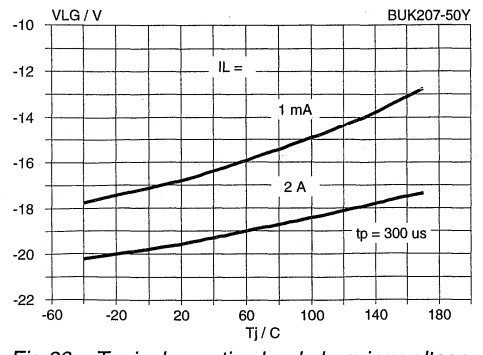


Fig.28. Typical negative load clamping voltage. $V_{LG} = f(T_j)$; parameter I_L; condition $V_{IG} = 0$ V.

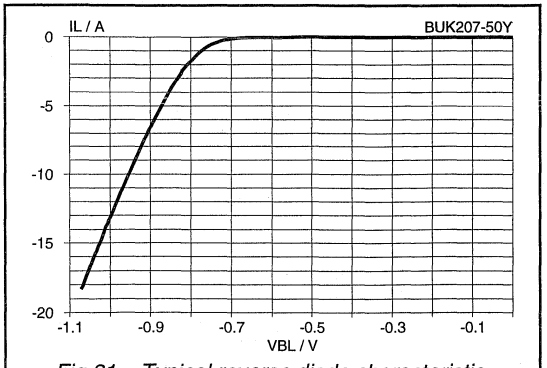


Fig.31. Typical reverse diode characteristic. $I_L = f(V_{BL})$; conditions $V_{IG} = 0$ V, $T_j = 25$ °C

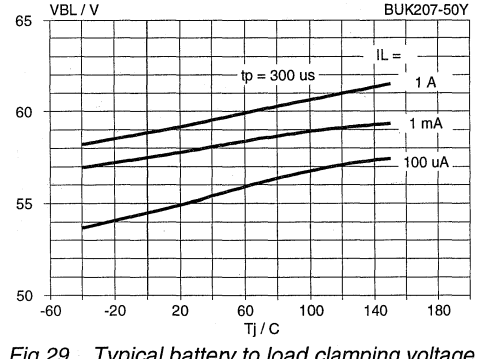


Fig.29. Typical battery to load clamping voltage. $V_{BL} = f(T_j)$; parameter I_L; condition $I_G = 5$ mA.

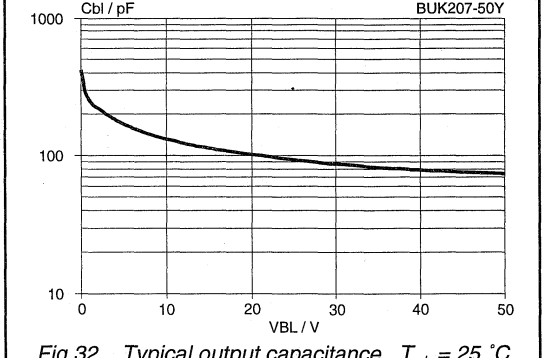


Fig.32. Typical output capacitance. $T_{mb} = 25$ °C $C_{bl} = f(V_{BL})$; conditions $f = 1$ MHz, $V_{IG} = 0$ V

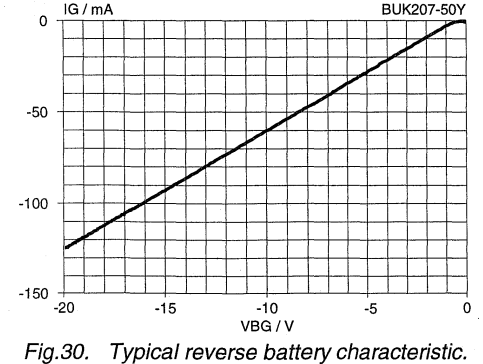


Fig.30. Typical reverse battery characteristic. $I_G = f(V_{BG})$; conditions $I_L = 0$ A, $T_j = 25$ °C

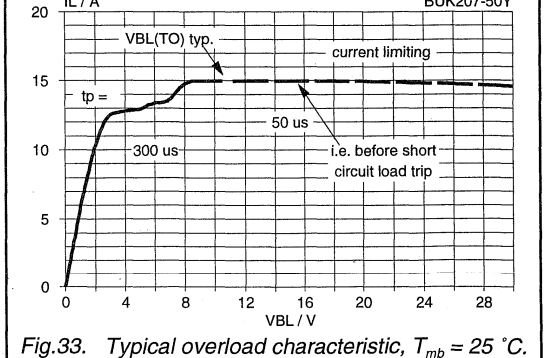


Fig.33. Typical overload characteristic, $T_{mb} = 25$ °C. $I_L = f(V_{BL})$; condition $V_{BG} = 13$ V; parameter t_p

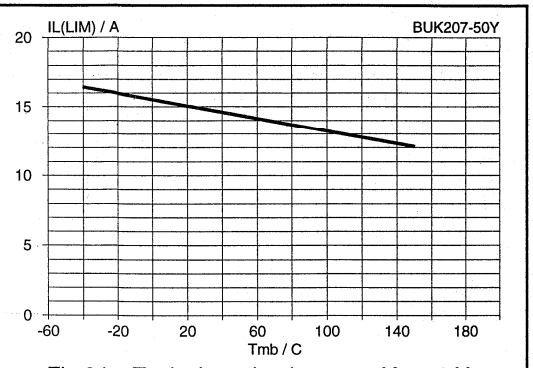


Fig.34. Typical overload current, V_{BL} = 9 V. $I_L = f(T_{mb})$; conditions V_{BG} = 13 V; t_p = 100 µs

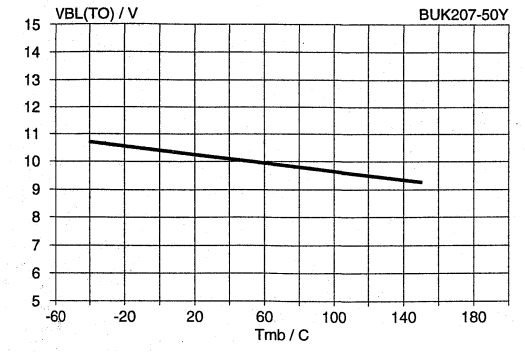


Fig.36. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(T_{mb})$; condition V_{BG} = 13 V

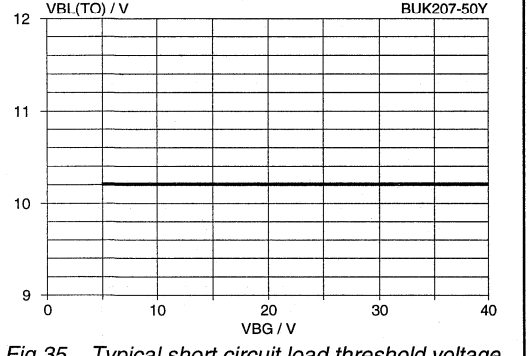


Fig.35. Typical short circuit load threshold voltage. $V_{BL(TO)} = f(V_{BG})$; condition T_{mb} = 25 °C

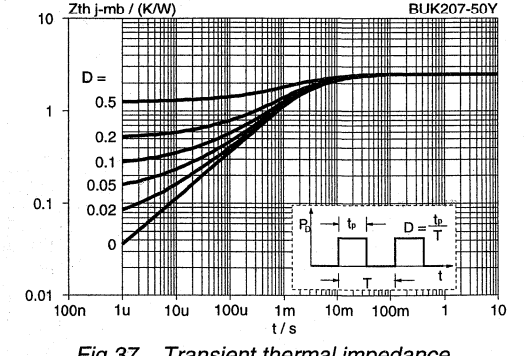


Fig.37. Transient thermal impedance. $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

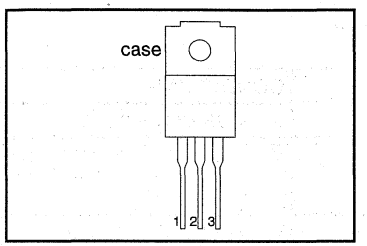
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK444	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	5.3	4.7	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	0.5	Ω

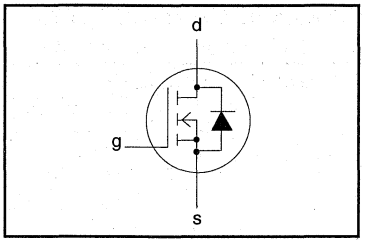
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	5.3	4.7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	3.3	3.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	21	19	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK444-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK444-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	5.3	A
I_{DRM}	Pulsed reverse drain current	-	-	-	21	A
V_{SD}	Diode forward voltage	I_F = 5.3 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 5.3 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.9	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

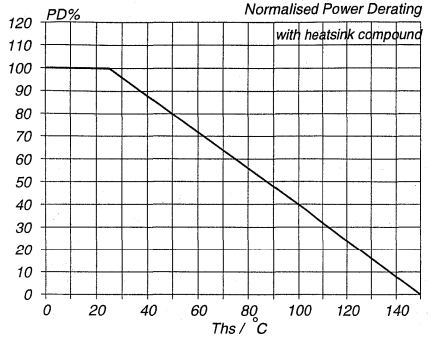


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

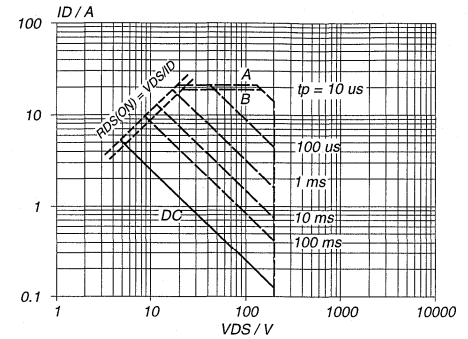


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

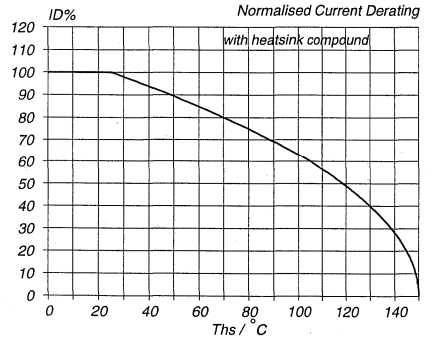


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

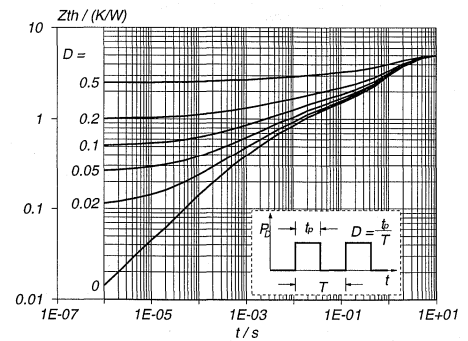


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

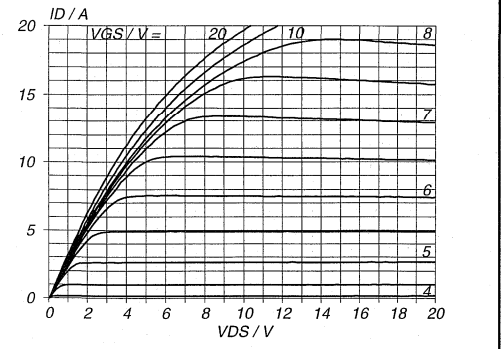


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

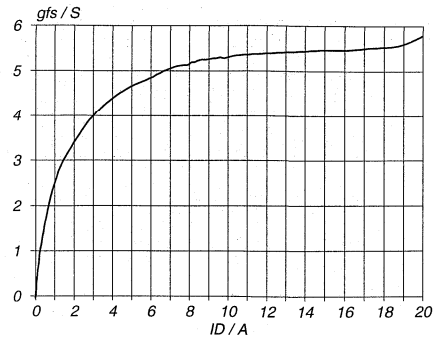


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

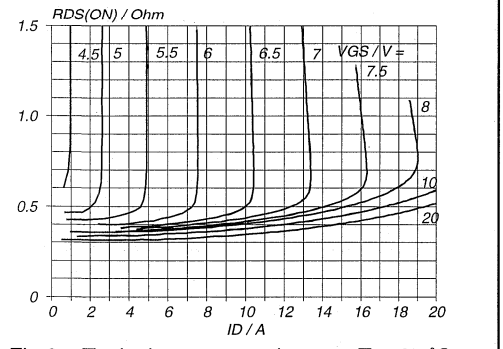


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

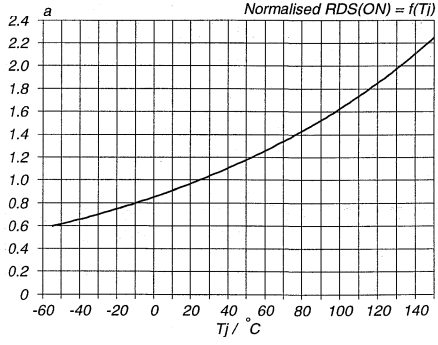


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

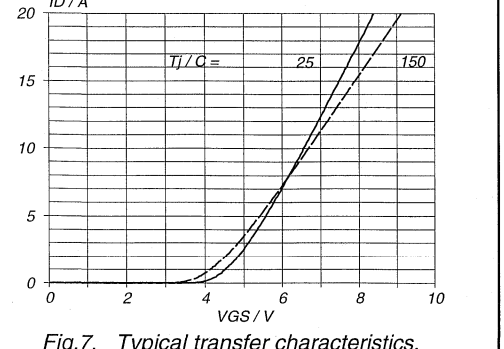


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

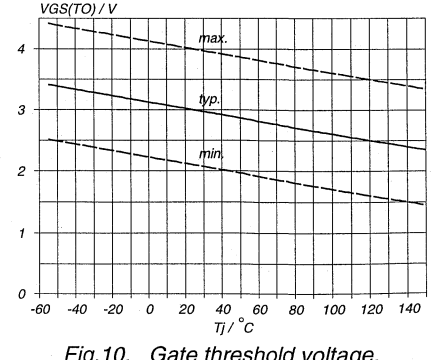


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

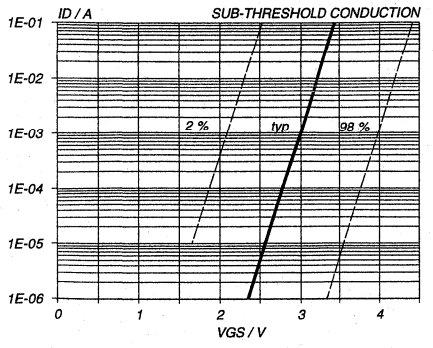


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

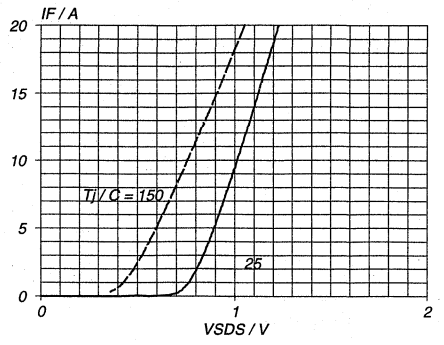


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

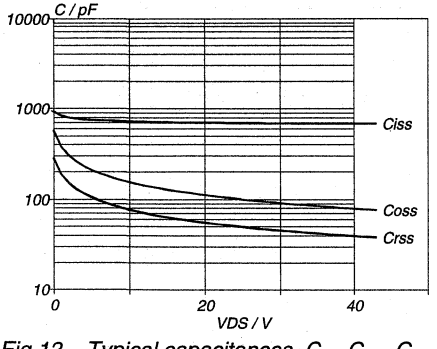


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

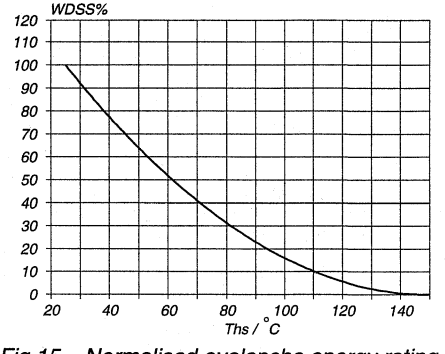


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 9$ A

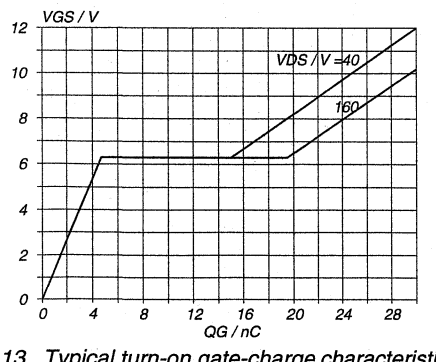


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9$ A; parameter V_{DS}

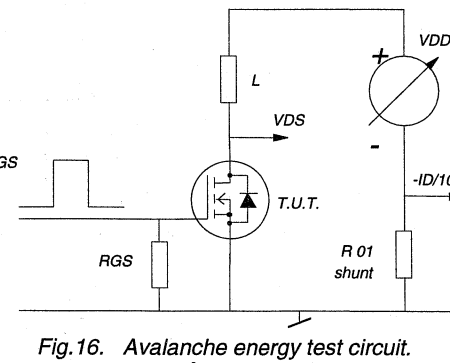


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

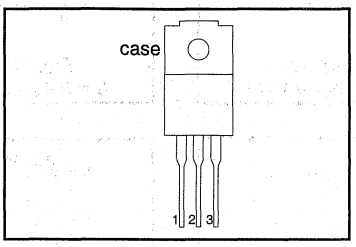
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK444	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	1.4	1.2	A
P_{tot}	Total power dissipation	30	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	6.0	8.0	Ω

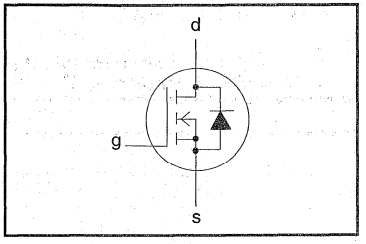
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.4	1.2	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	0.9	0.75	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	5.6	4.8	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK444-800A**	-	5.0	6.0	Ω
		I_D = 1.0 A **BUK444-800B**	-	6.0	8.0	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.0 A	1.0	2.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	450	750	pF
C_{oss}	Output capacitance		-	42	70	pF
C_{rss}	Feedback capacitance		-	15	30	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1.9 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.4	A
I_{DRM}	Pulsed reverse drain current	-	-	-	5.6	A
V_{SD}	Diode forward voltage	I_F = 1.4 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 1.4 A; -dI_F/dt = 100 A/µs;	-	230	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.9	-	µC

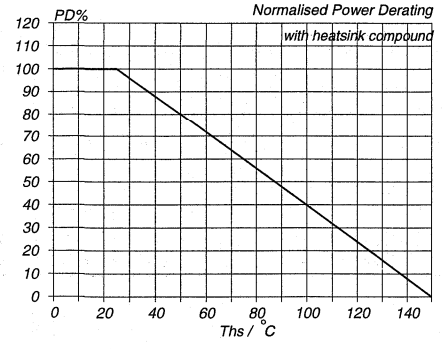


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

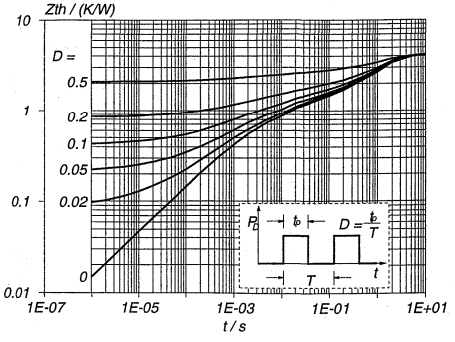


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

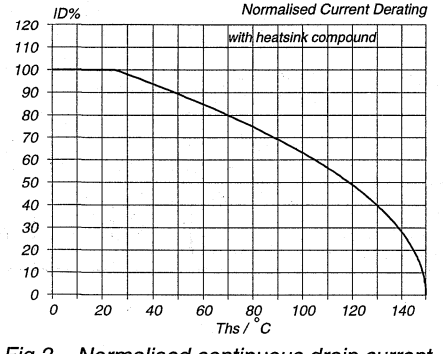


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

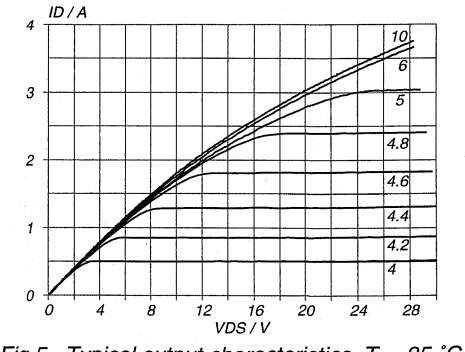


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

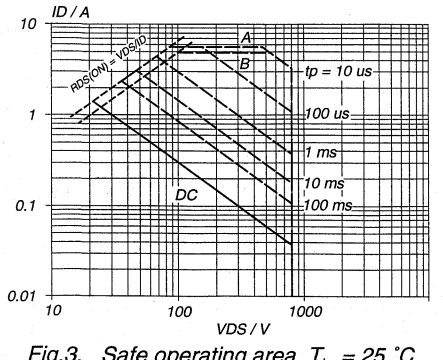


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

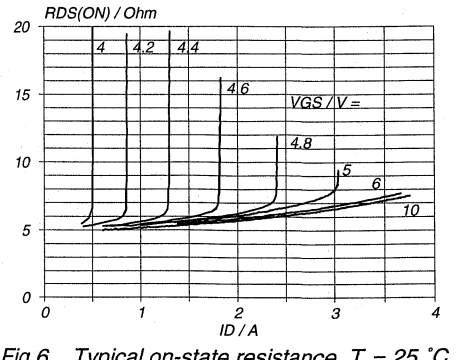


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

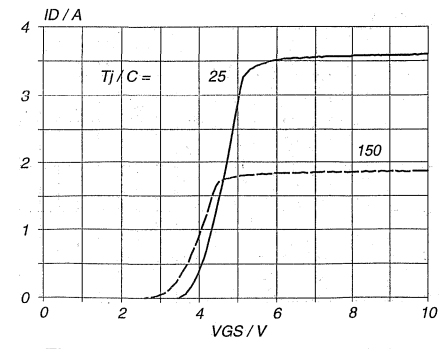


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

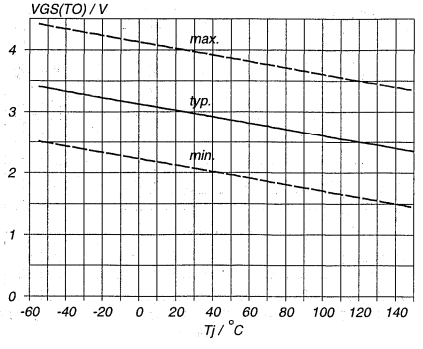


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

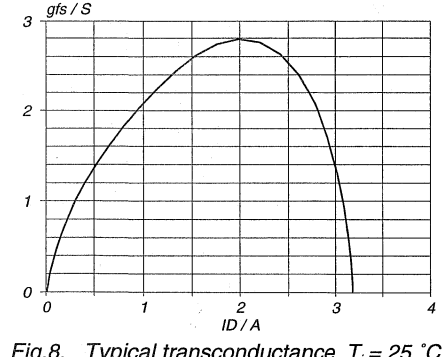


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

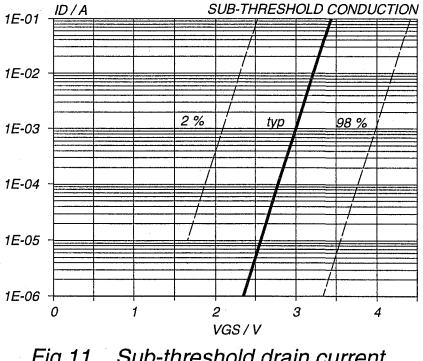


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

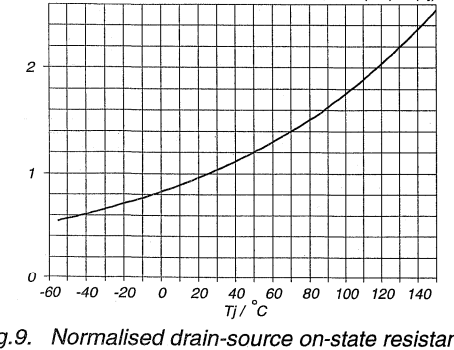


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.0 A; V_{GS} = 10 V

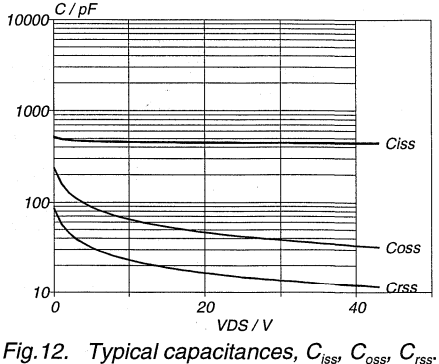


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

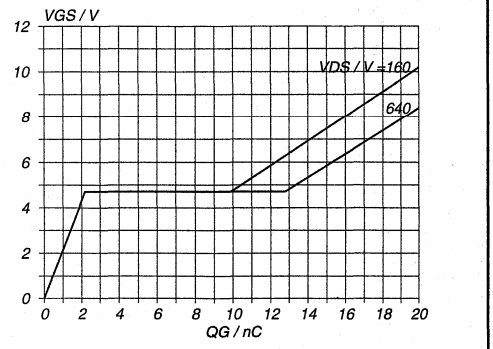


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2.4$ A; parameter V_{DS}

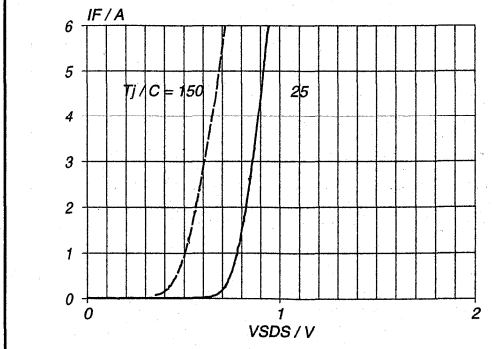


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

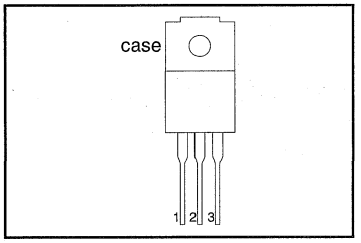
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK445	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	7.6	7	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.23	0.28	Ω

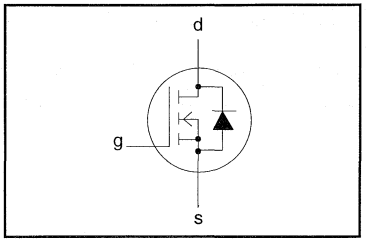
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	7.6	7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.8	4.4	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	30	28	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 7 A **BUK445-200A**	-	0.2	0.23	Ω
		BUK445-200B	-	0.22	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	7.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 7.6 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 7.6 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.3	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

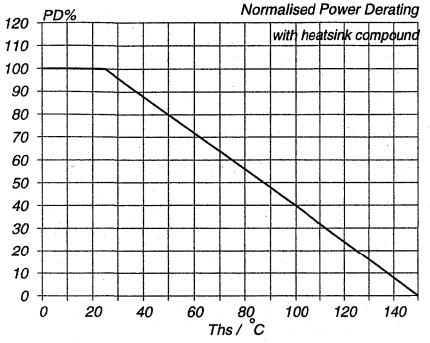


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

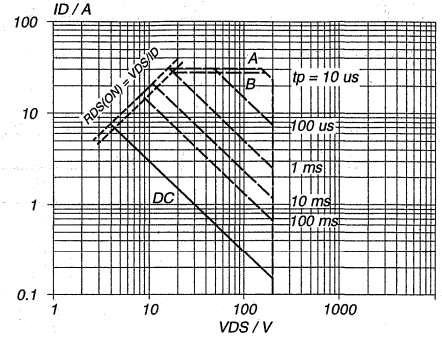


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

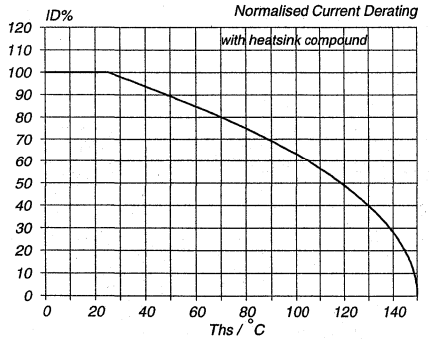


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

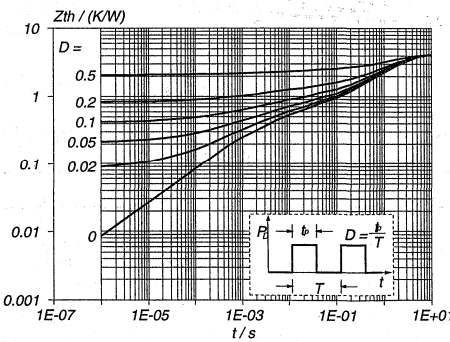


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

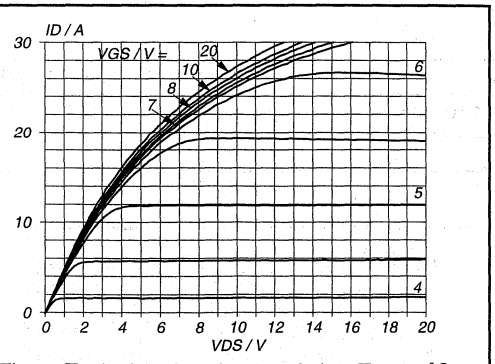


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

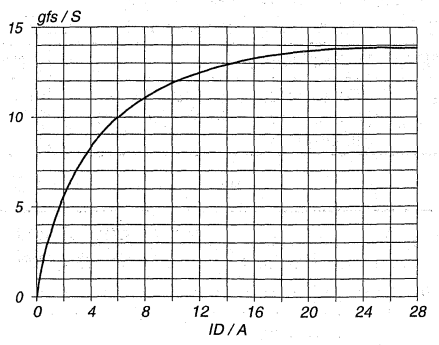


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

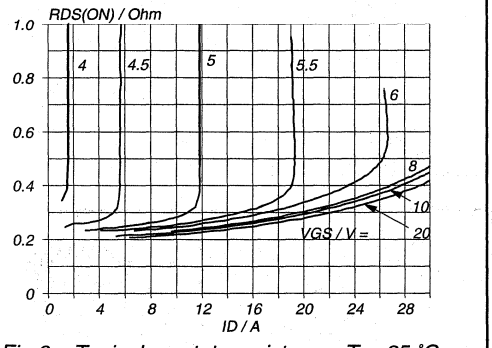


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

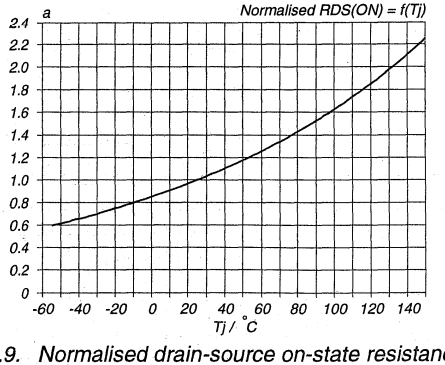


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 10 V

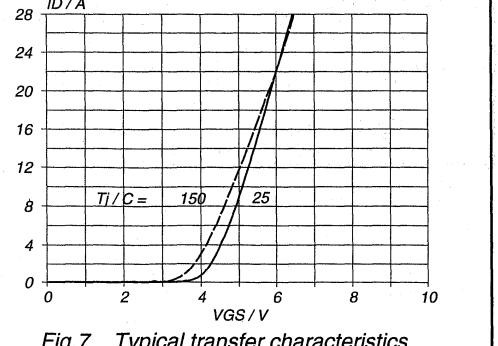


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

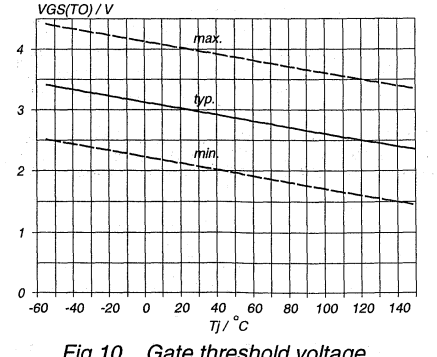


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

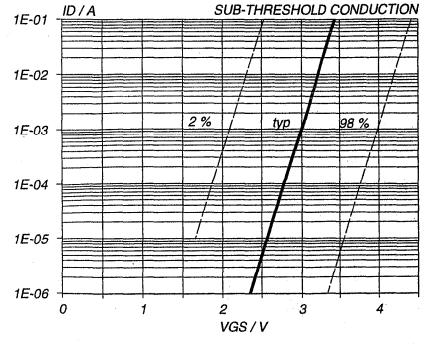


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

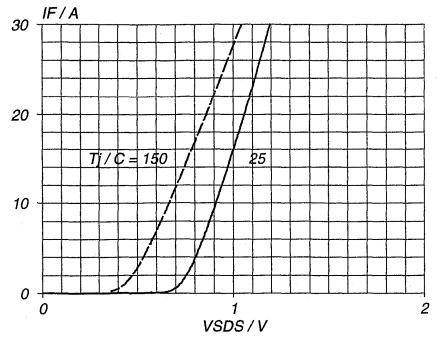


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

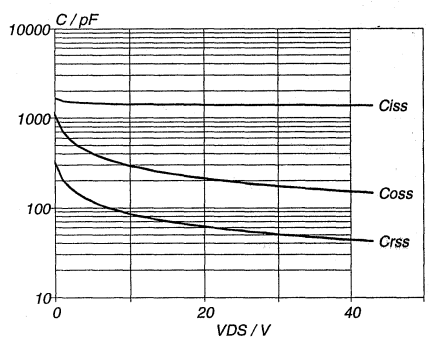


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

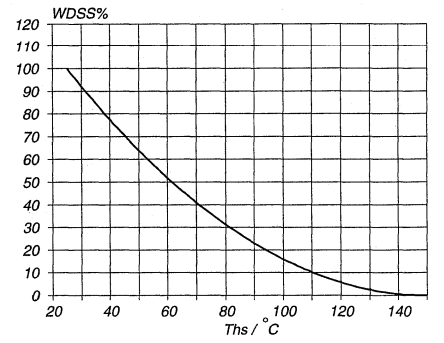


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 14$ A

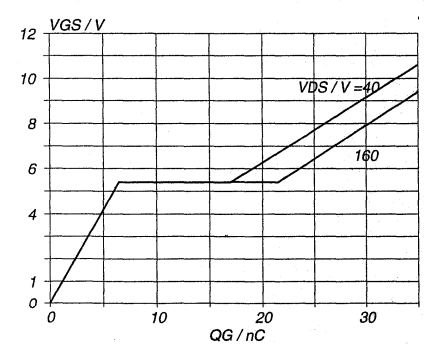


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

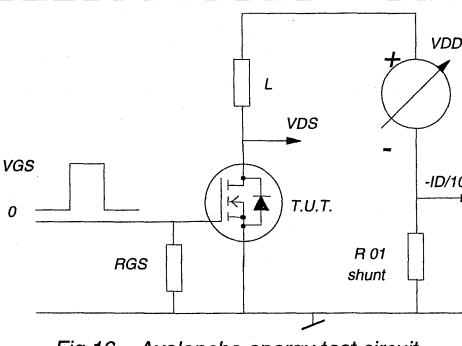


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

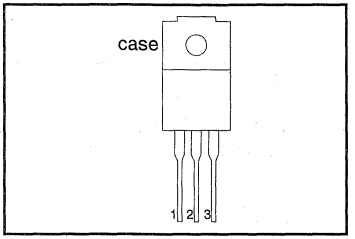
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK446	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	2.0	1.7	A
P_{tot}	Total power dissipation	30	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	3	4	Ω

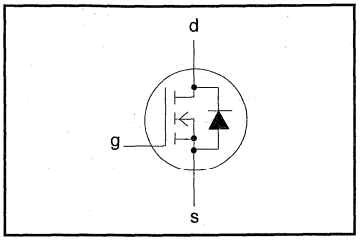
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	2.0	1.7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	1.3	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	8	6.8	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.16	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK446-800A**	-	2.7	3.0	Ω
		I_D = 1.5 A **BUK446-800B**	-	3.5	4.0	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	2.0	A
I_{DRM}	Pulsed reverse drain current	-	-	-	8	A
V_{SD}	Diode forward voltage	I_F = 2.0 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 2.0 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

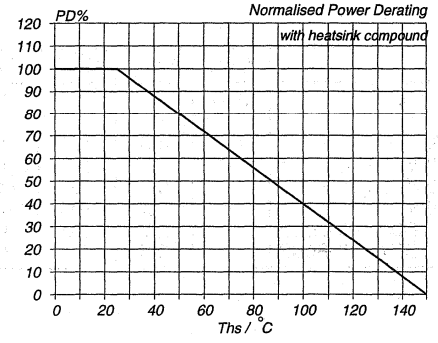


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

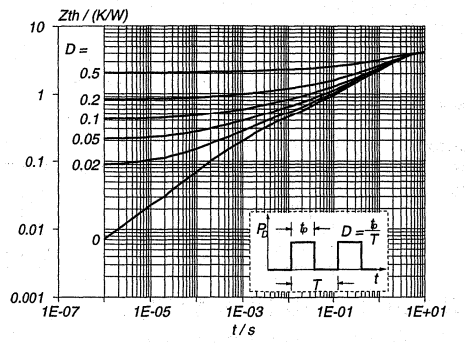


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

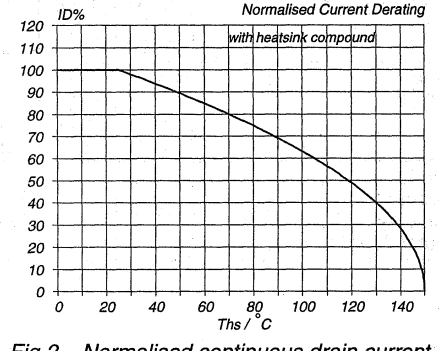


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

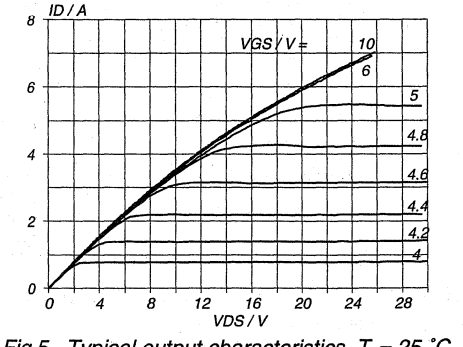


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

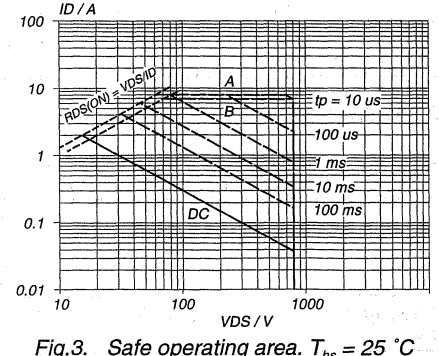


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

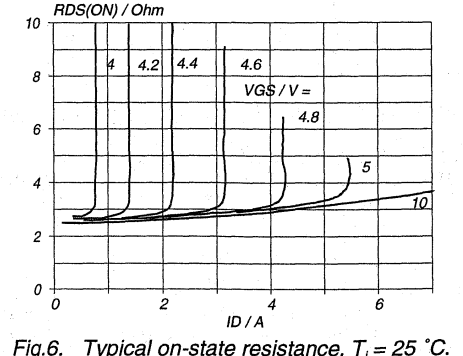


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

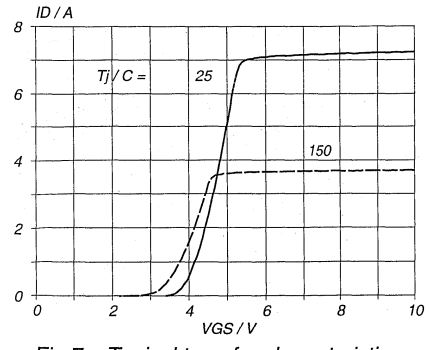


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

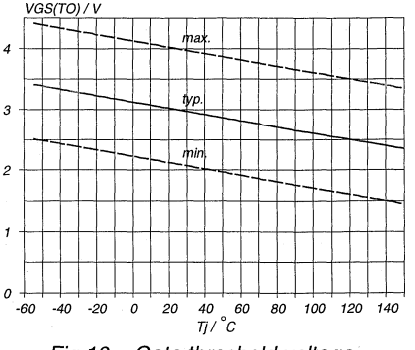


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

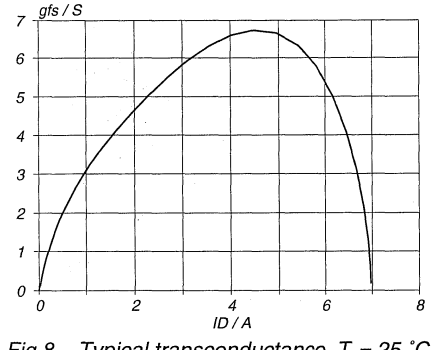


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

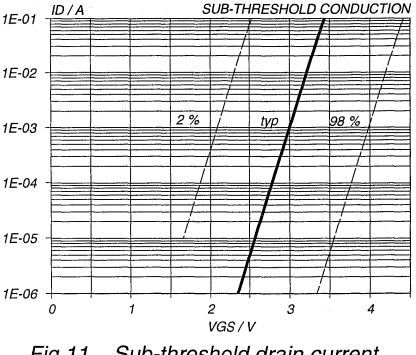


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

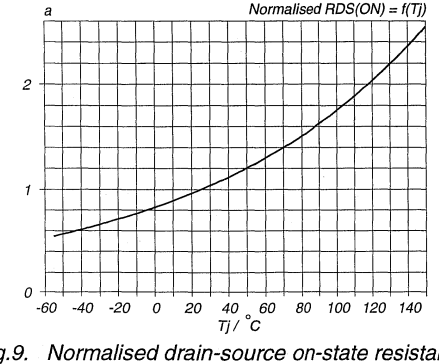


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

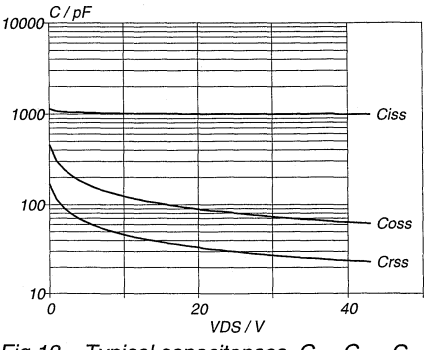


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

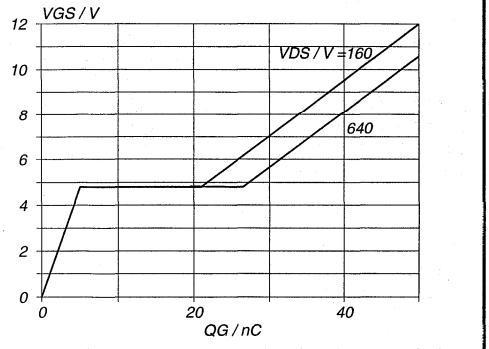


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 4$ A; parameter V_{DS}

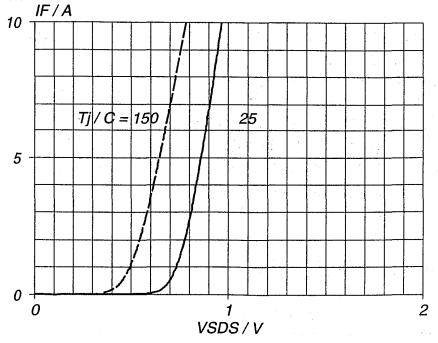


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

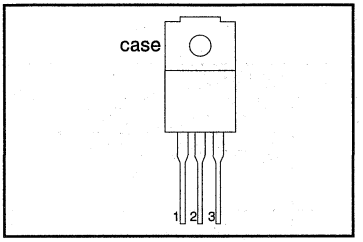
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (DC)	1.5	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	5	Ω

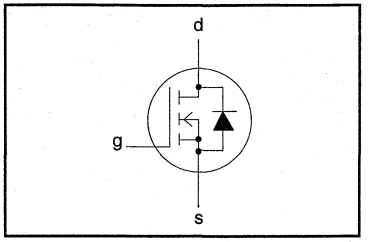
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	1000	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.5	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	1.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.16	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	1000	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.5 A	-	4.5	5.0	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.7	A
I_{DRM}	Pulsed reverse drain current	-	-	-	6.8	A
V_{SD}	Diode forward voltage	I_F = 1.7 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 1.7 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

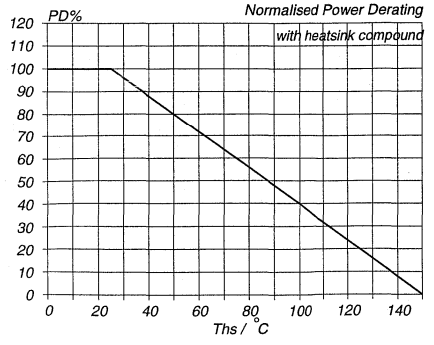


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

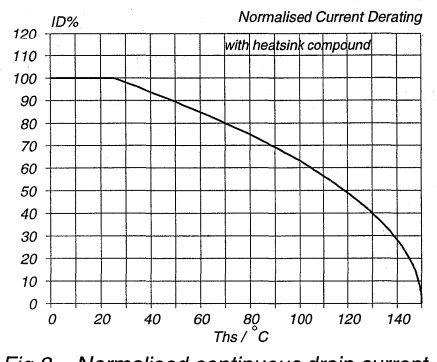


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 10 V

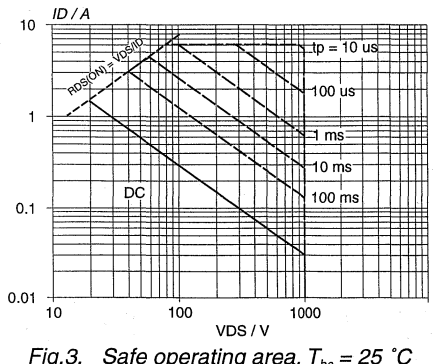


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

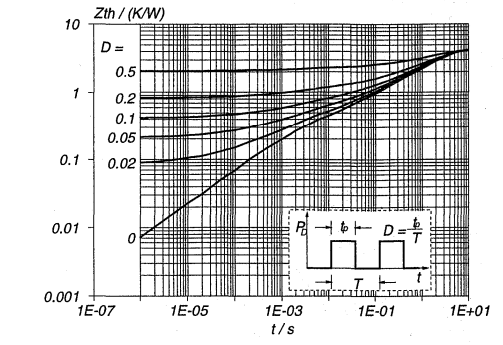


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

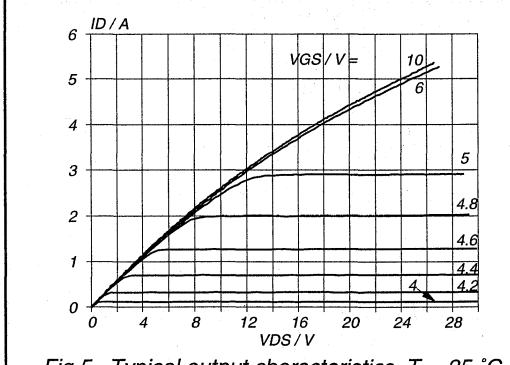


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

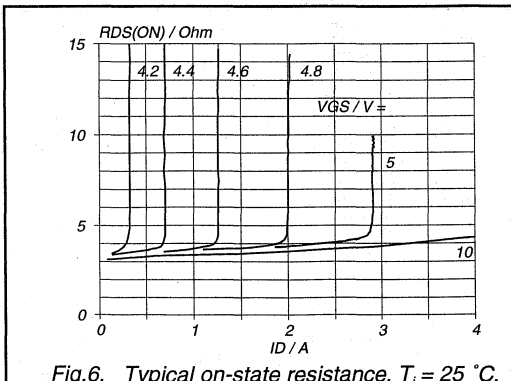


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

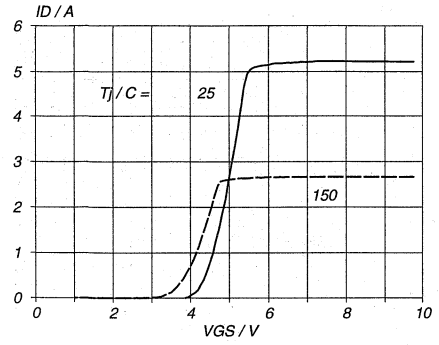


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

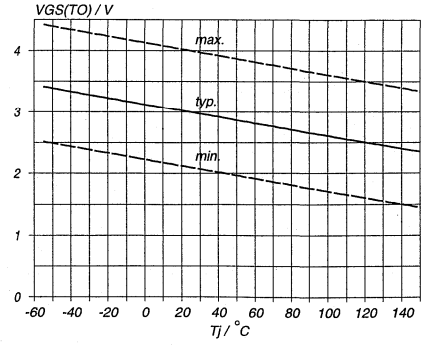


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

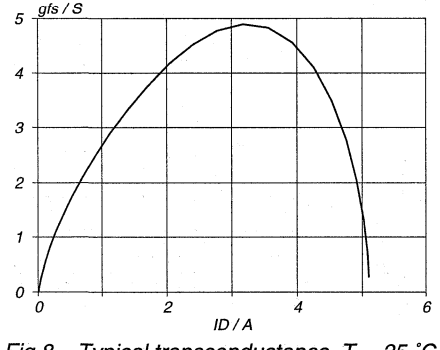


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

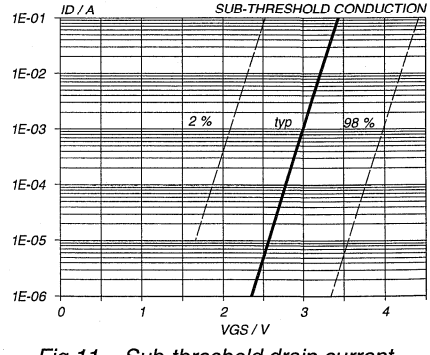


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

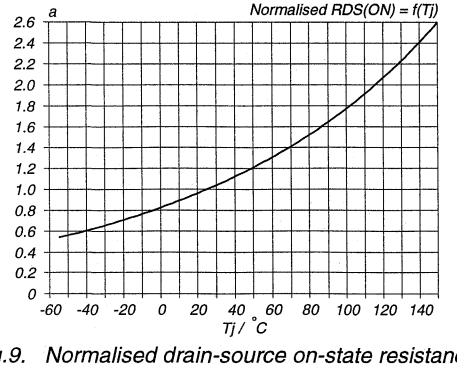


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

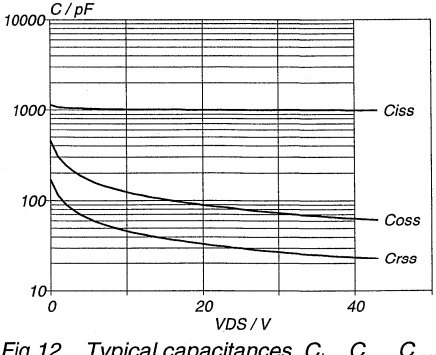


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

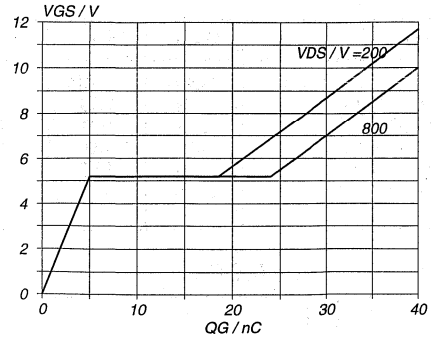


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3.5$ A; parameter V_{DS}

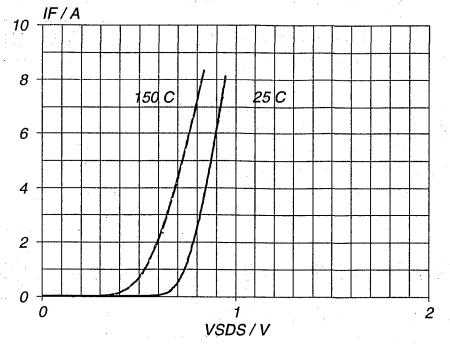


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

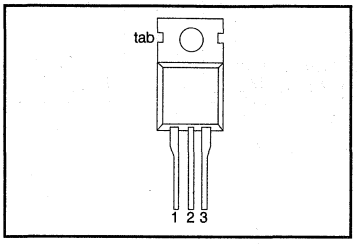
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK451	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	3.0	3.0	A
P_{tot}	Total power dissipation	40	40	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.85	1.1	Ω

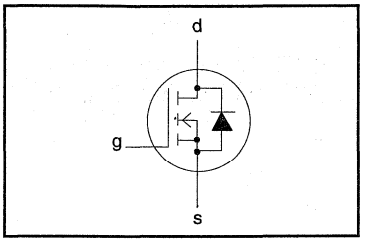
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	3.0	3.0	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	3.0	3.0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	12	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK451-100A**	-	0.75	0.85	Ω
		I_D = 2.5 A **BUK451-100B**	-	0.90	1.10	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2.5 A	1.3	1.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	160	240	pF
C_{oss}	Output capacitance		-	45	60	pF
C_{rss}	Feedback capacitance		-	16	25	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	4	6	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	15	25	ns
$t_{d\ off}$	Turn-off delay time	R_{gen} = 50 Ω	-	10	20	ns
t_f	Turn-off fall time		-	10	20	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	3.0	A
I_{DRM}	Pulsed reverse drain current	-	-	-	12	A
V_{SD}	Diode forward voltage	I_F = 3.0 A ; V_{GS} = 0 V	-	1.1	1.4	V
t_{rr}	Reverse recovery time	I_F = 3.0 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

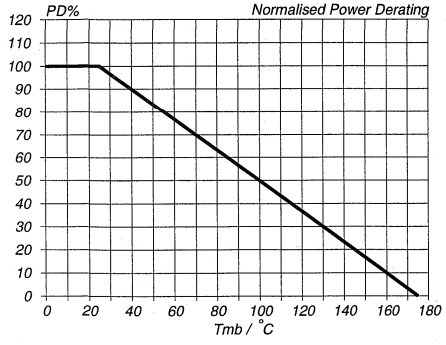


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

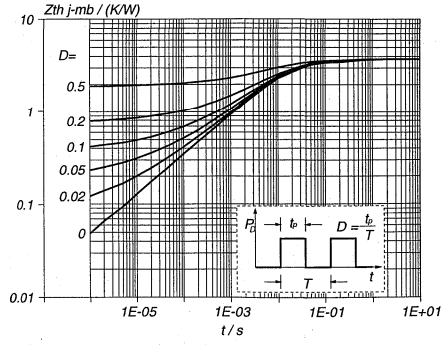


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

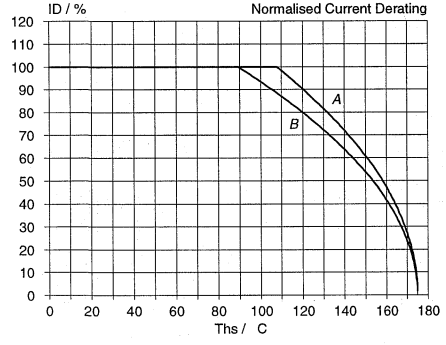


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

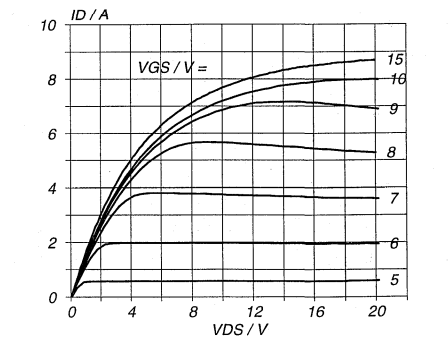


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

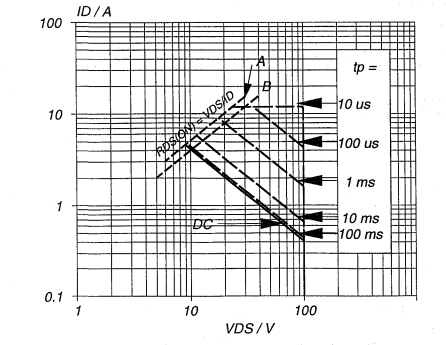


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

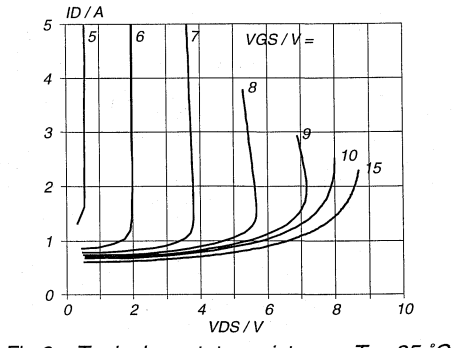


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

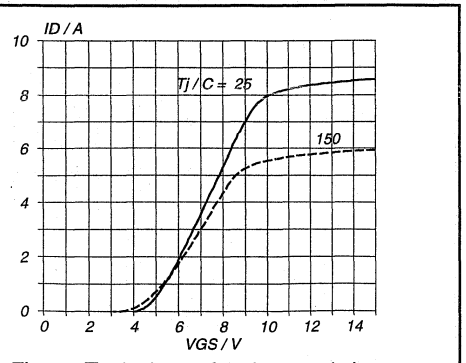


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

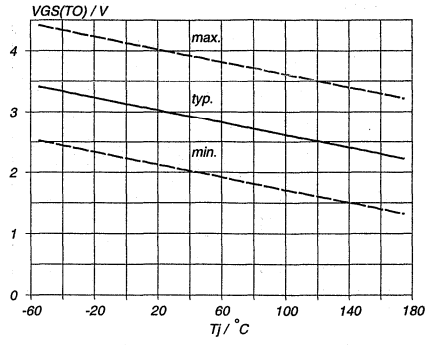


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

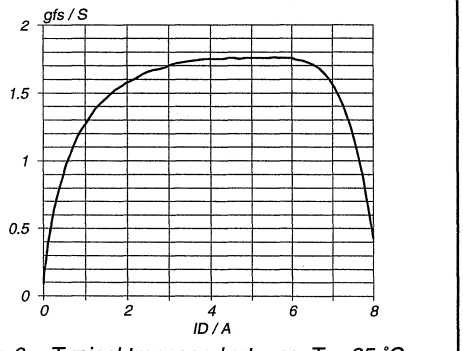


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

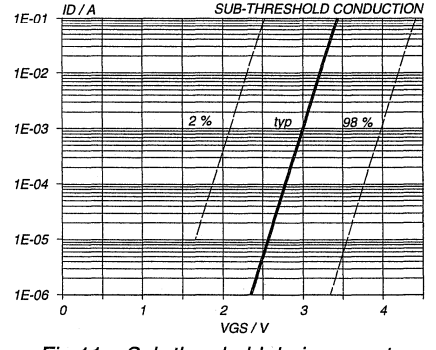


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

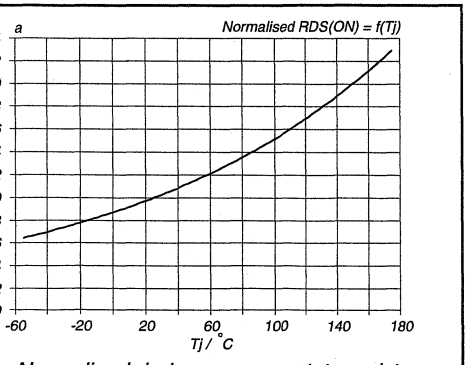


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.5 A; V_{GS} = 5 V

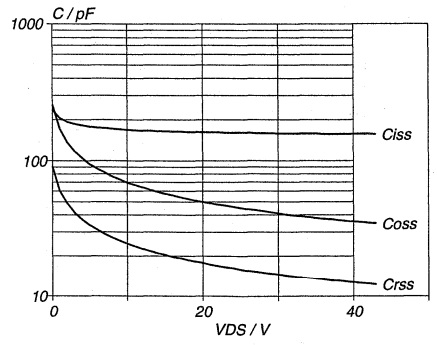


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

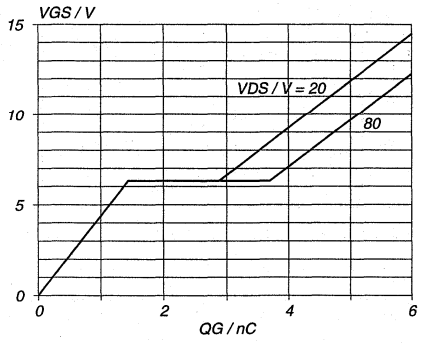


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3$ A; parameter V_{DS}

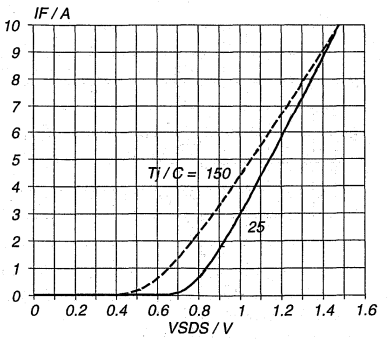


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

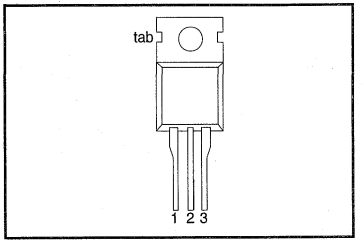
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK452	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	15	14	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.13	0.15	Ω

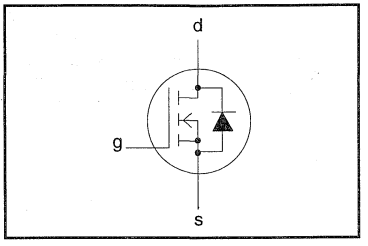
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	15	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	11	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	60	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK452-60A**	-	0.11	0.13	Ω
		I_D = 8.5 A **BUK452-60B**	-	0.13	0.15	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	3.5	4.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	70	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	8	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	45	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	15	A
I_{DRM}	Pulsed reverse drain current	-	-	-	60	A
V_{SD}	Diode forward voltage	I_F = 15 A ; V_{GS} = 0 V	-	1.4	1.7	V
t_{rr}	Reverse recovery time	I_F = 15 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 15 A ; $V_{DD} \leq$ 30 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	30	mJ

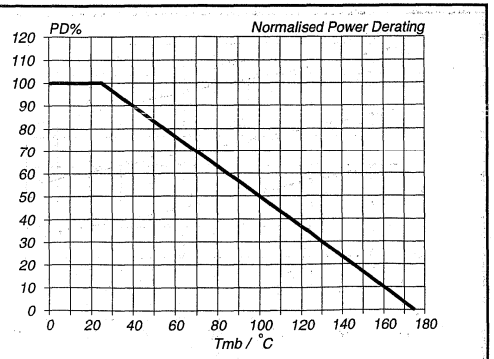


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

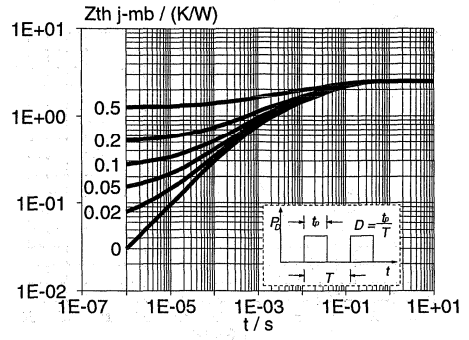


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

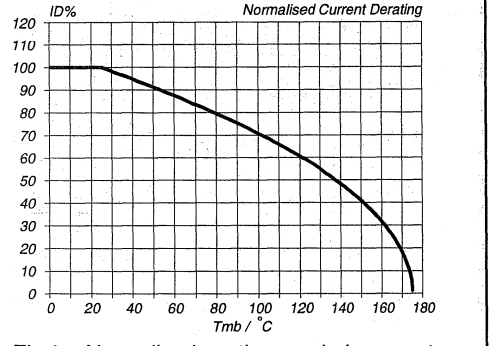


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

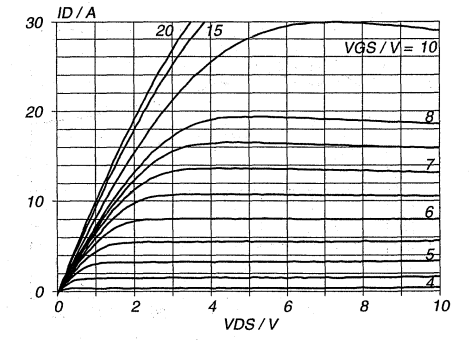


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

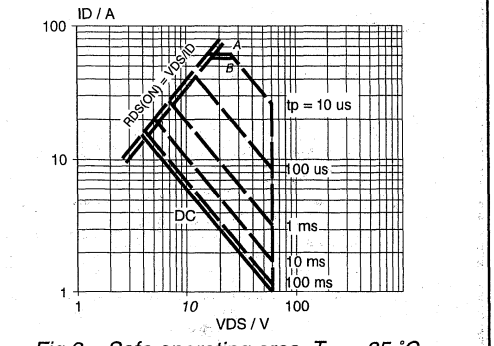


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

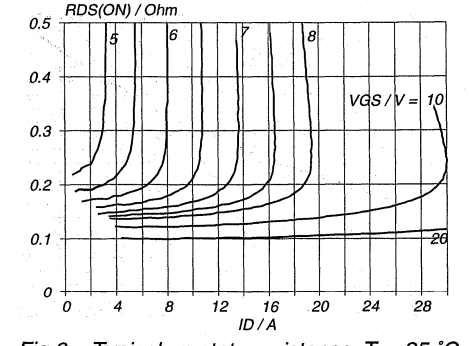


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

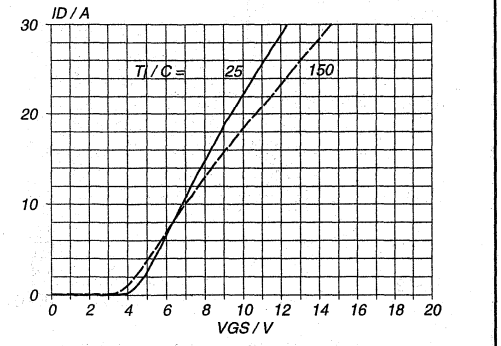


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

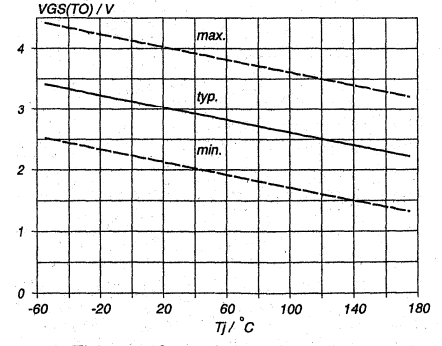


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

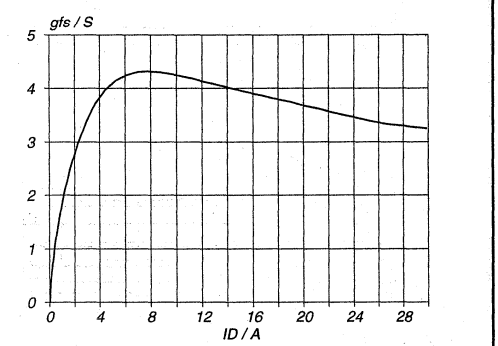


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

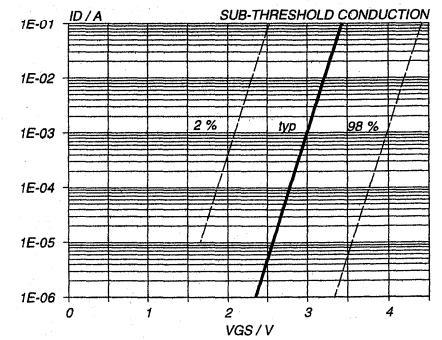


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

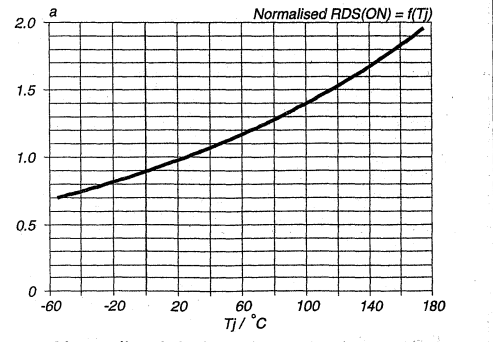


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 8.5$ A; $V_{GS} = 10$ V

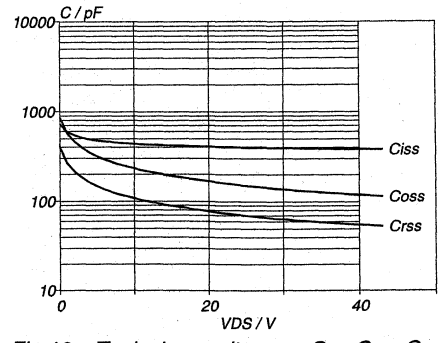


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

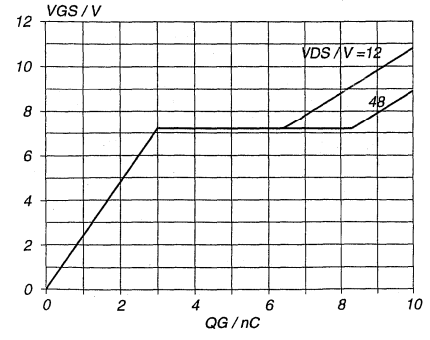


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 15 A; parameter V_{DS}

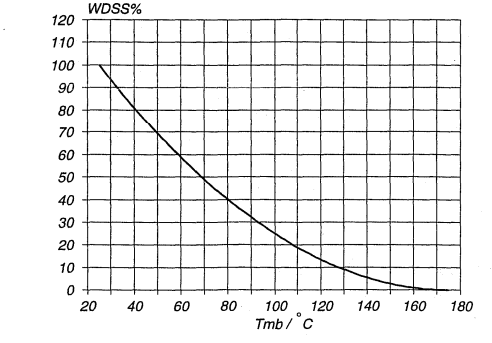


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 15 A

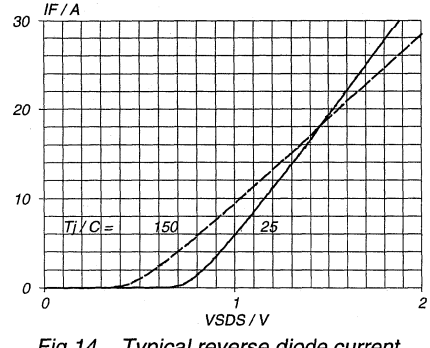


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

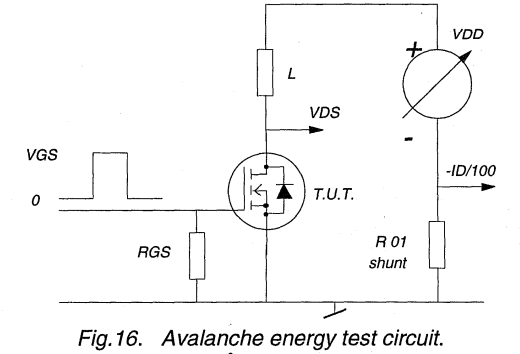


Fig.16. Avalanche energy test circuit. $W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

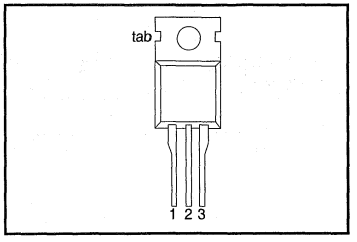
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK452	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	11	10	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	0.3	Ω

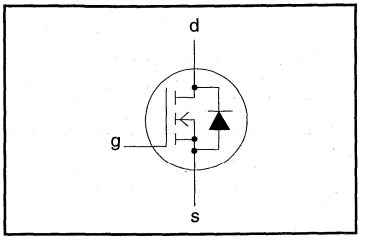
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11	10	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.7	7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	44	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK452-100A**	-	0.22	0.25	Ω
		I_D = 5.5 A **BUK452-100B**	-	0.25	0.3	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	11	A
I_{DRM}	Pulsed reverse drain current	-	-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

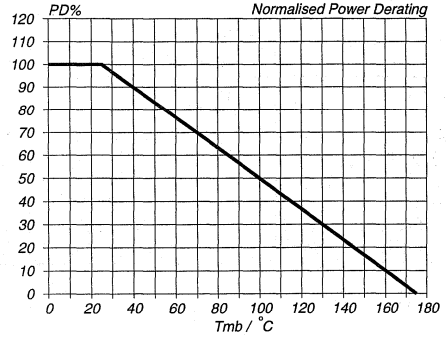


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

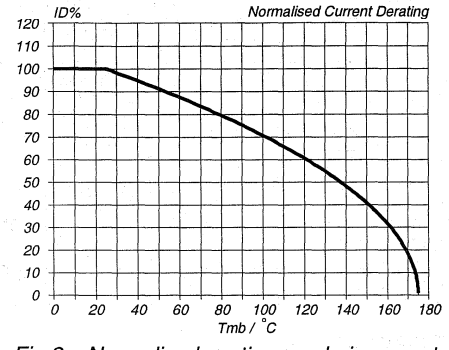


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

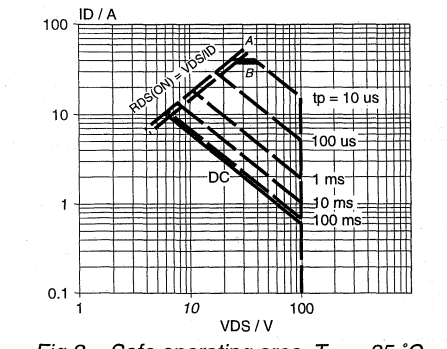


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

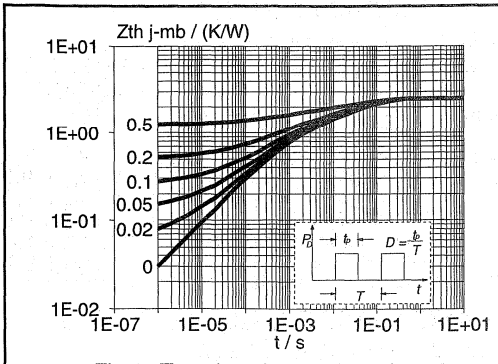


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

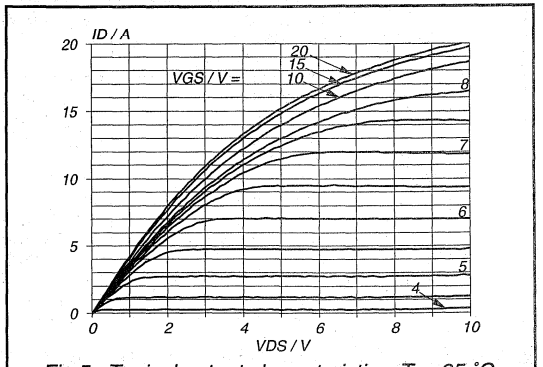


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

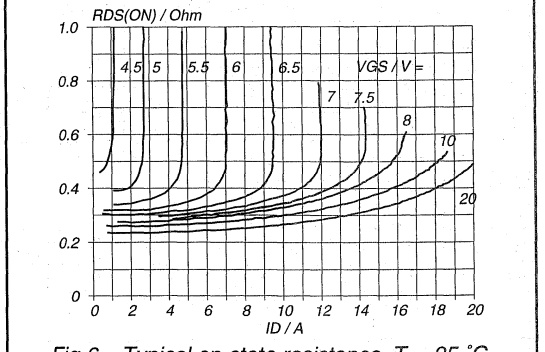


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

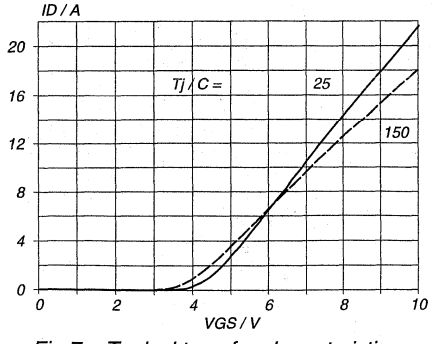


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

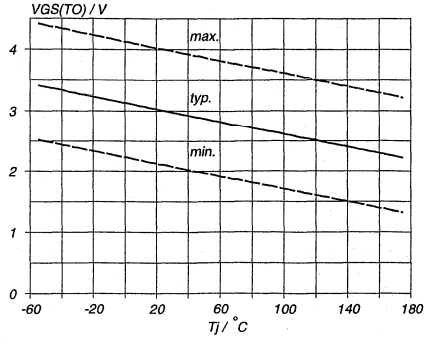


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

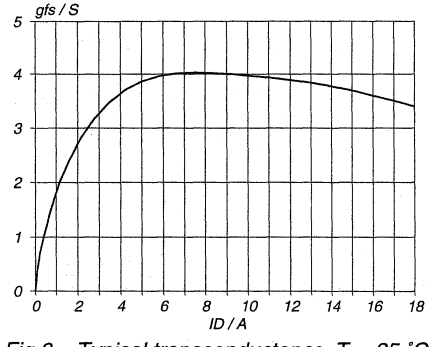


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

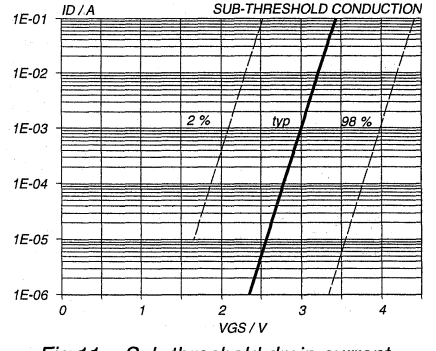


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

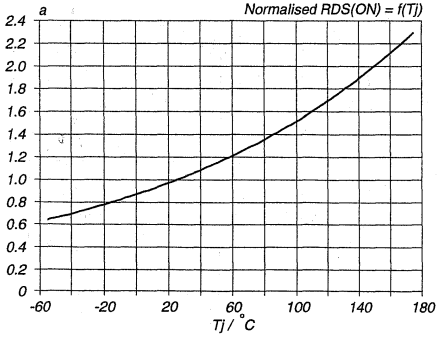


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

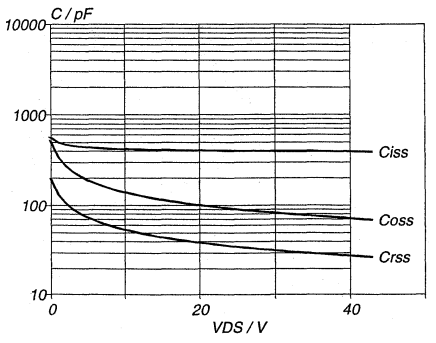


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

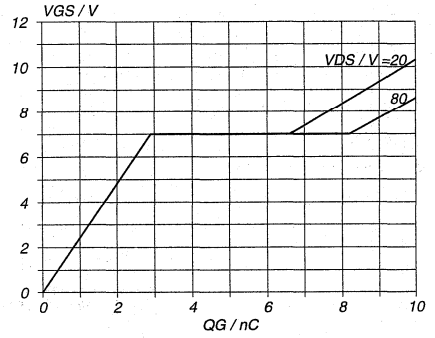


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 11$ A; parameter V_{DS}

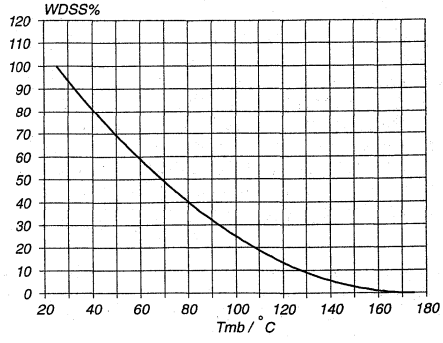


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 11$ A

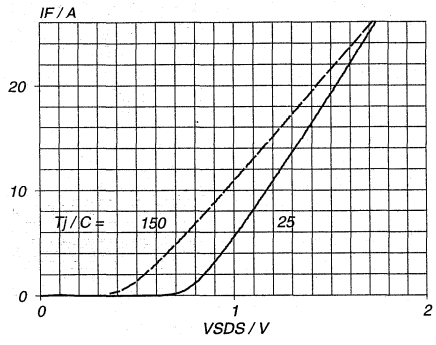


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

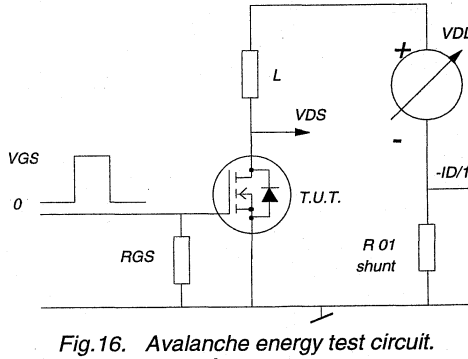


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

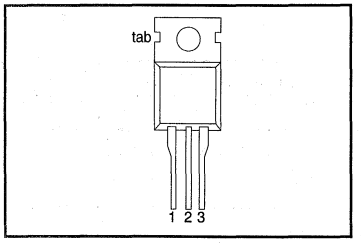
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK453	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	22	20	A
P_{tot}	Total power dissipation	75	75	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	0.10	Ω

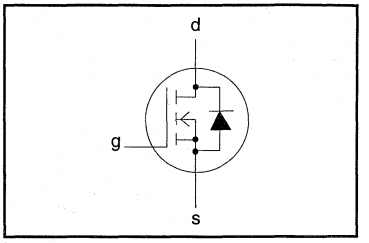
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	22	20	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	15	14	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	88	80	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A **BUK453-60A**	-	0.07	0.08	Ω
		BUK453-60B	-	0.08	0.10	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	4.5	6.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	120	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	55	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	22	A
I_{DRM}	Pulsed reverse drain current	-	-	-	88	A
V_{SD}	Diode forward voltage	I_F = 22 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 22 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 22 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

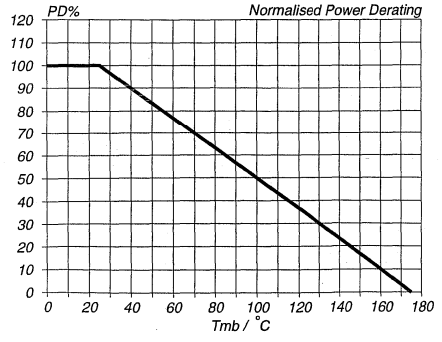


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

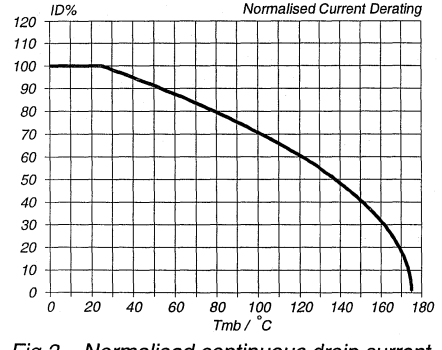


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 10 V

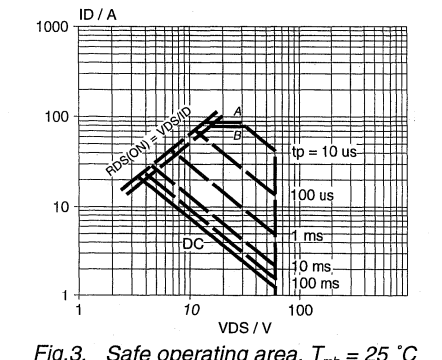


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

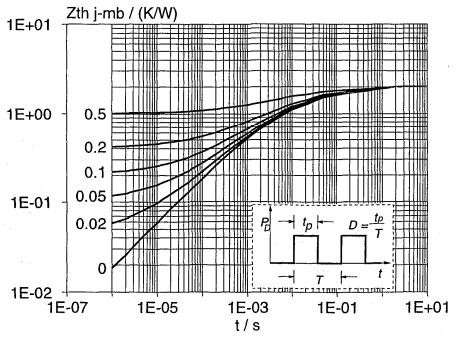


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

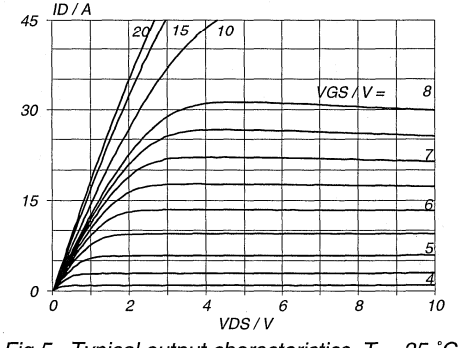


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

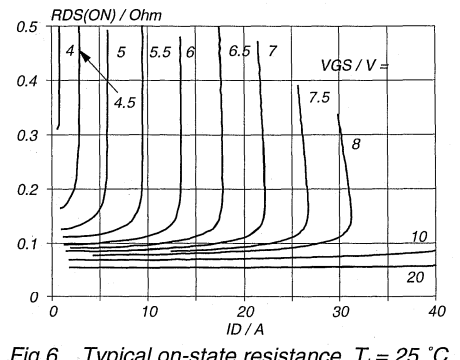


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

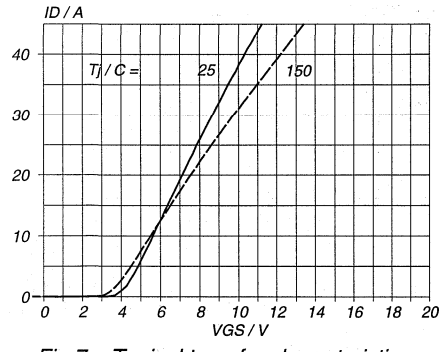


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

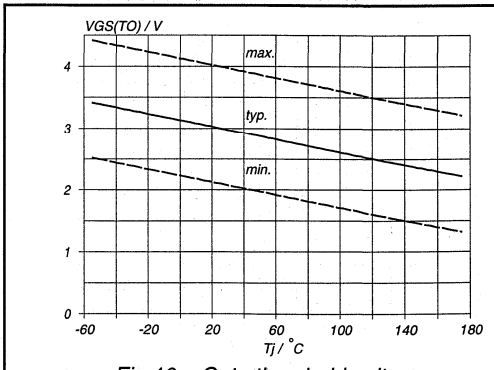


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

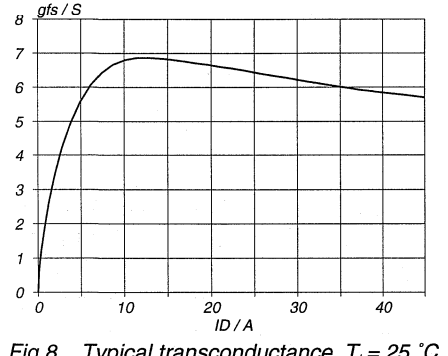


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

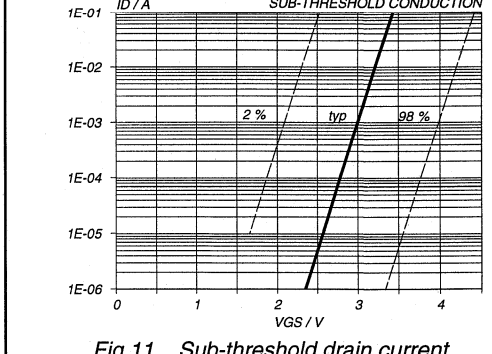


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

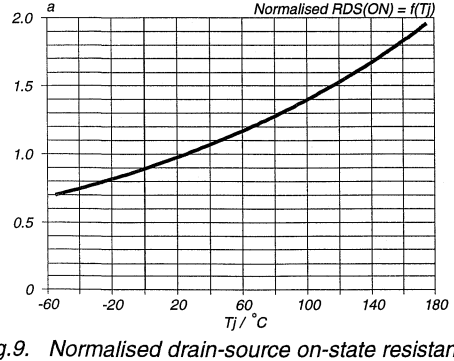


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

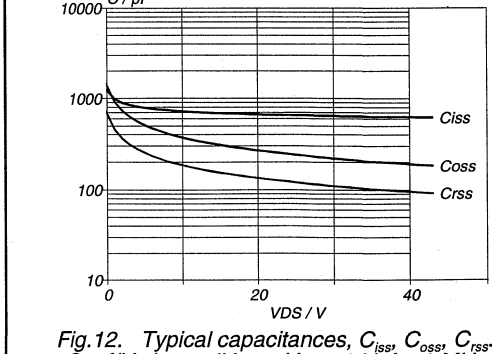


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

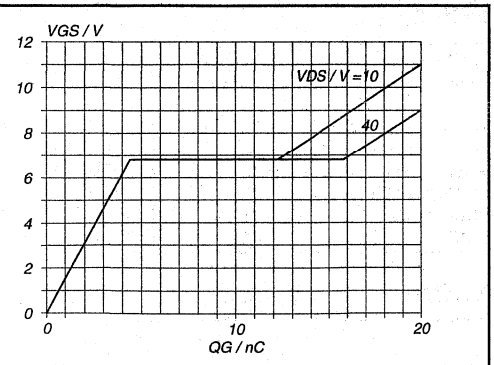


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 22$ A; parameter V_{DS}

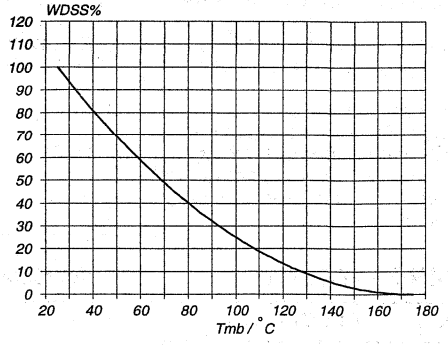


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 22$ A

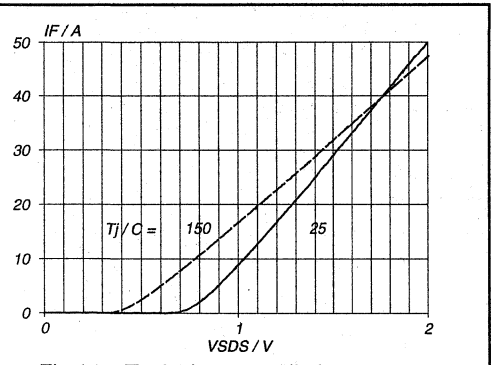


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

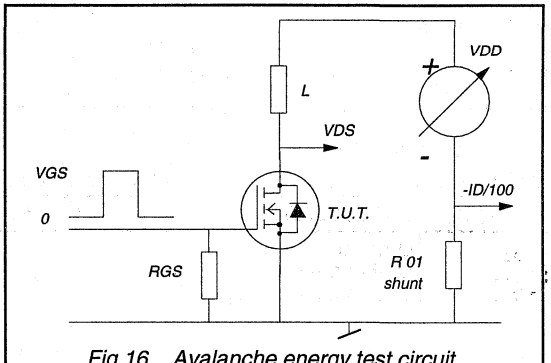


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

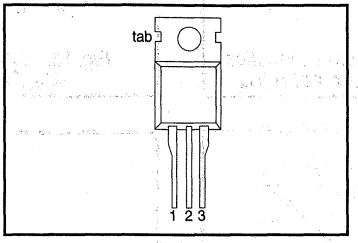
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK453	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	75	75	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.20	Ω

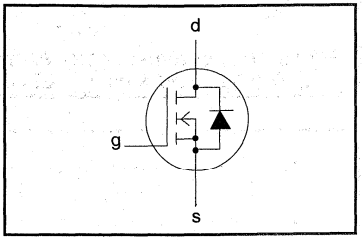
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK453-100A**	-	0.15	0.16	Ω
		I_D = 5 A **BUK453-100B**	-	0.15	0.20	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	70	mJ

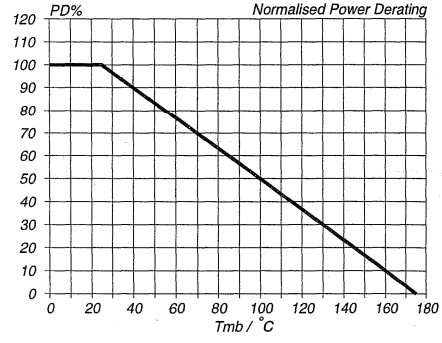


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

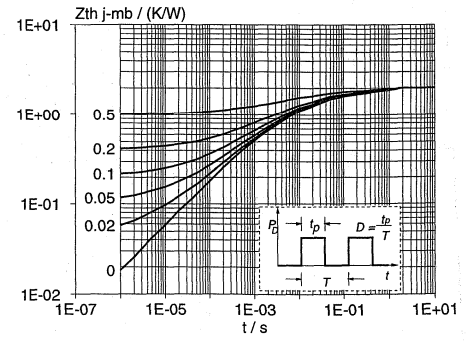


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

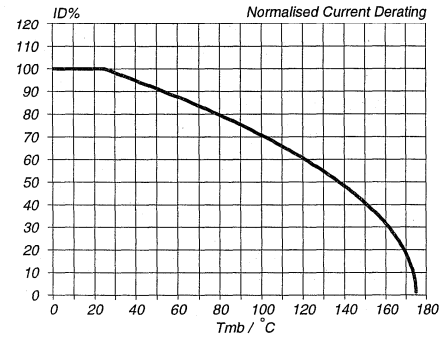


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

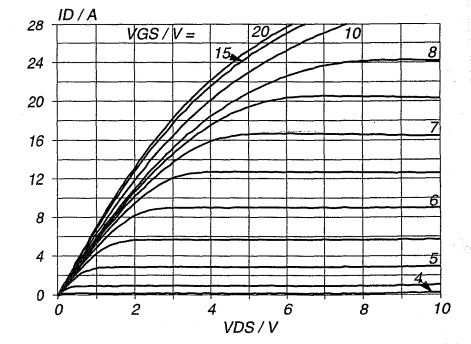


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

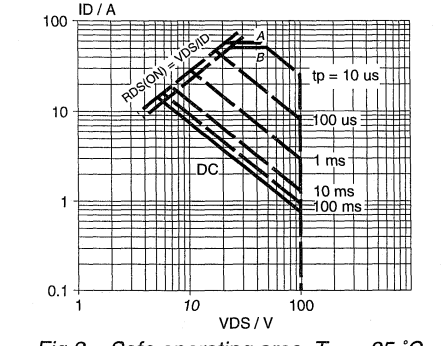


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

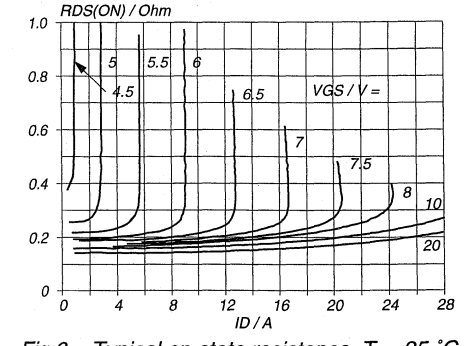


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

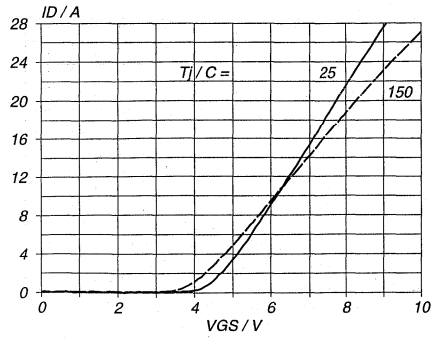


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

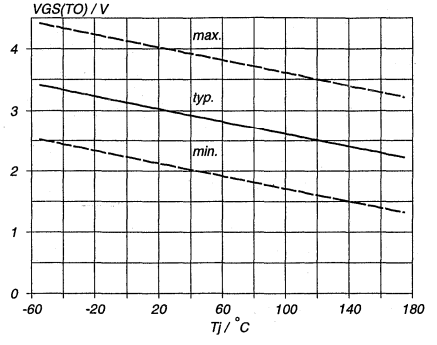


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

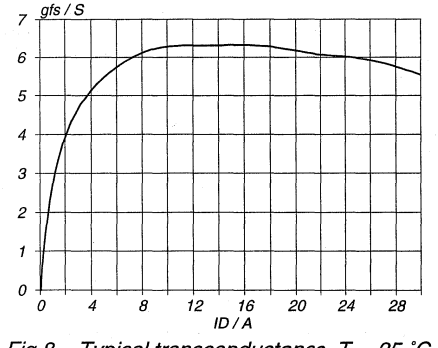


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

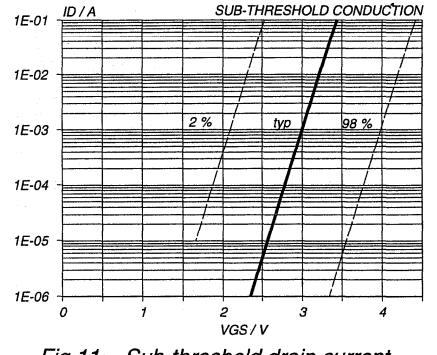


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

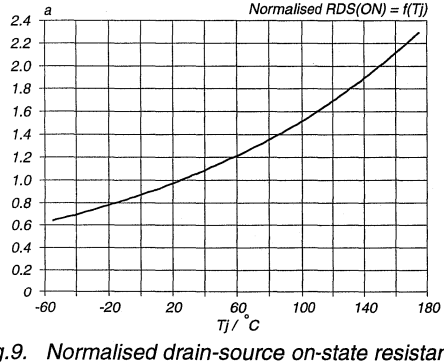


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

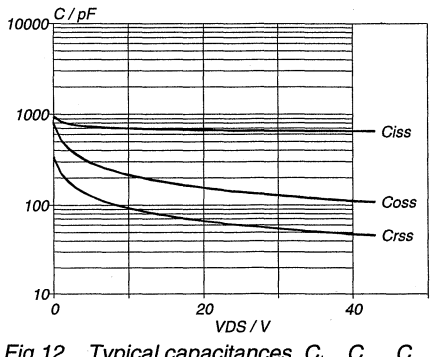


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

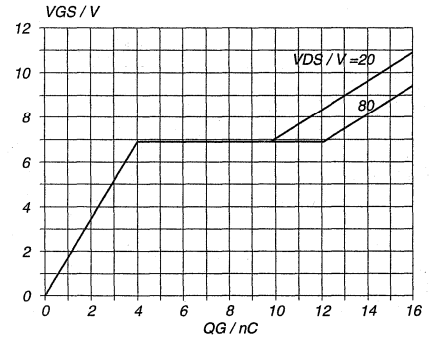


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

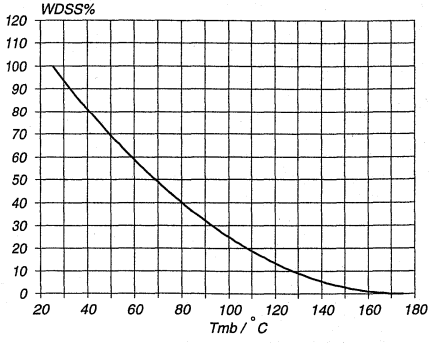


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

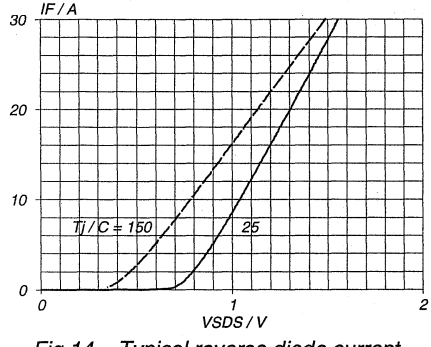


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

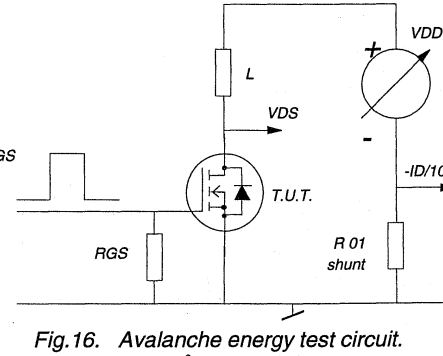


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

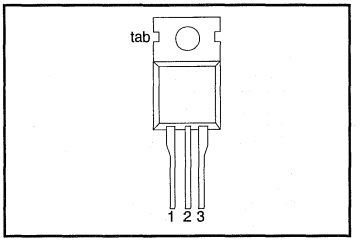
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	41	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	38	mΩ

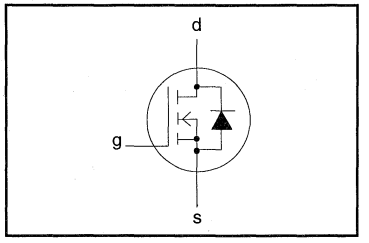
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	30	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	7	14	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	900	1600	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	55	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	75	125	ns
t_f	Turn-off fall time		-	60	100	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

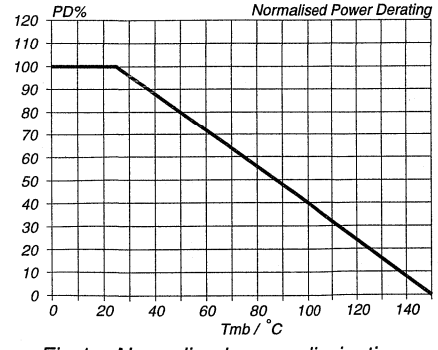


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

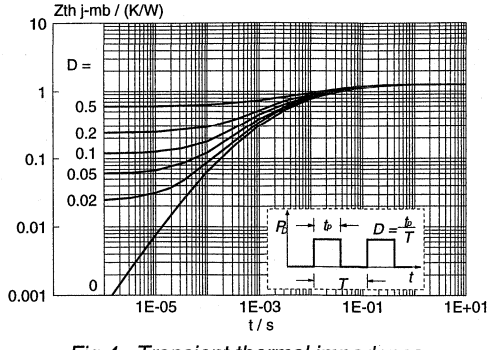


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

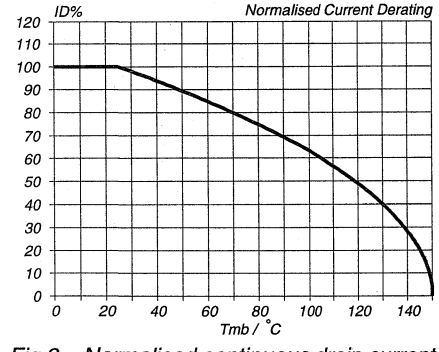


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

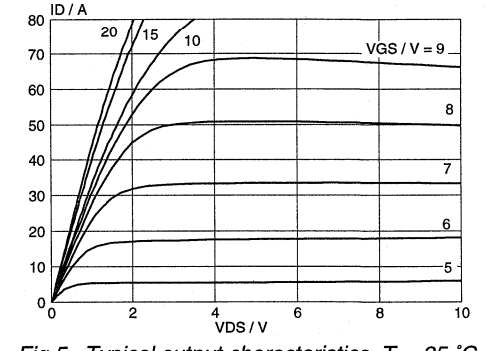


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

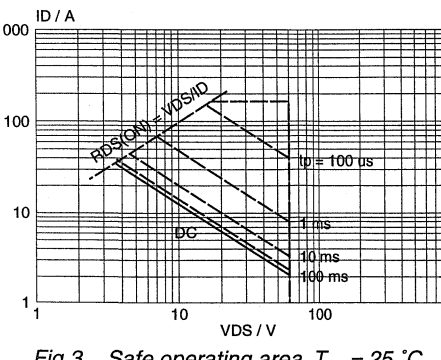


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

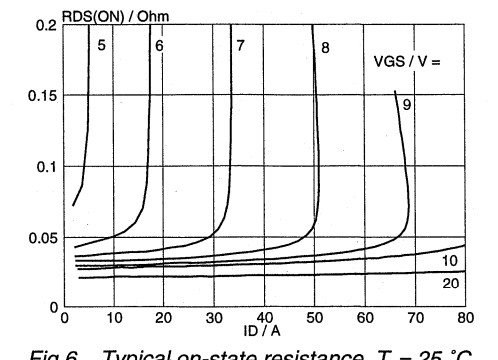


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

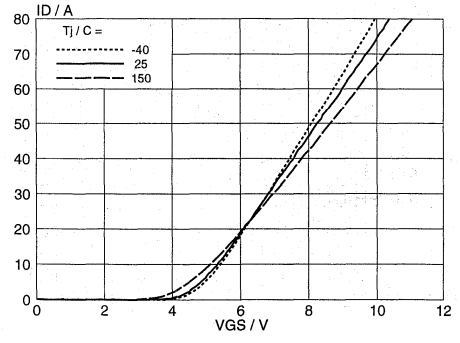


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 15 V; parameter T_j

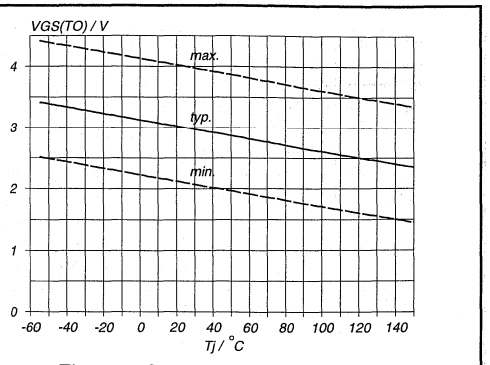


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

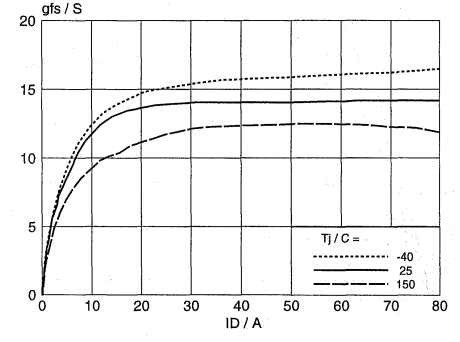


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

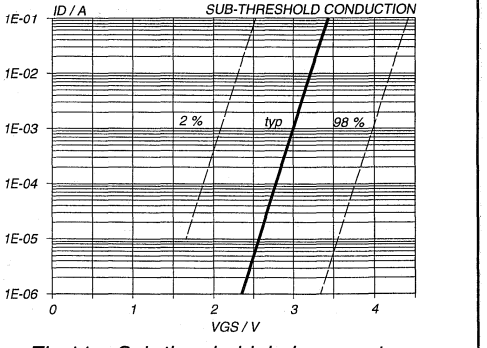


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

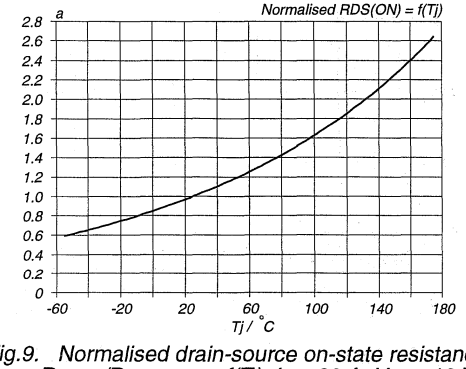


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

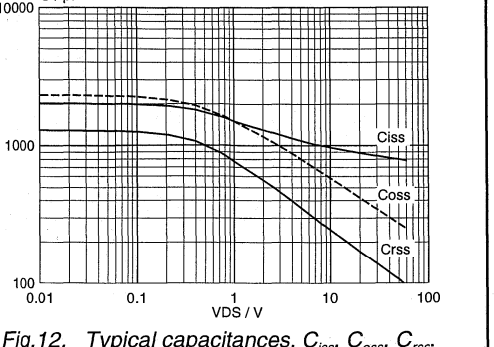


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

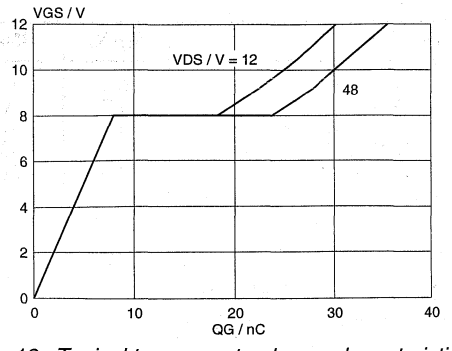


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

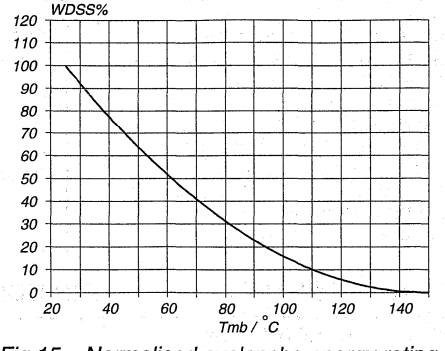


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

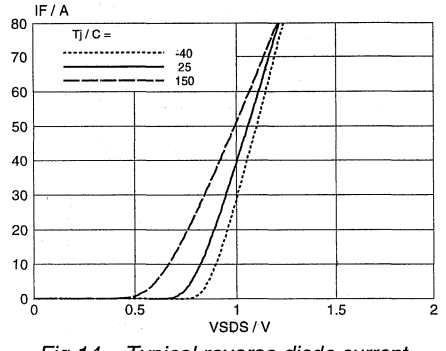


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

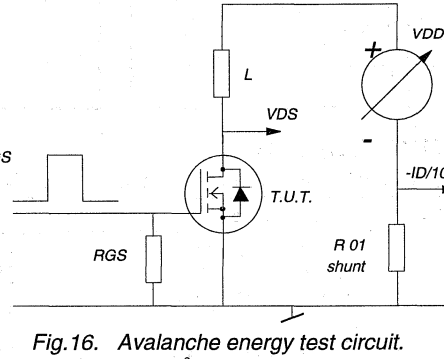


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for use in surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

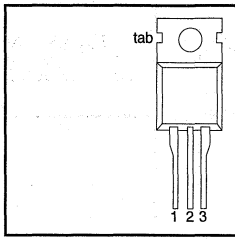
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	Ω

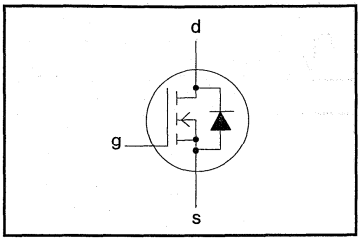
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	**-200B**	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	8.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	5.8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	33	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK454-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK454-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.2	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

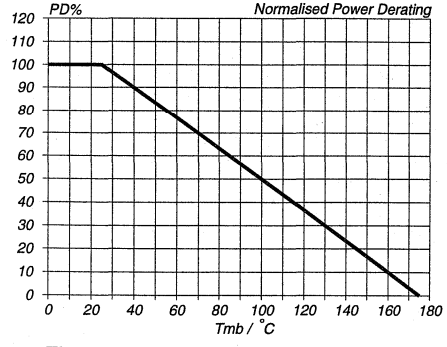


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\ 25\ °C} = f(T_{mb})$

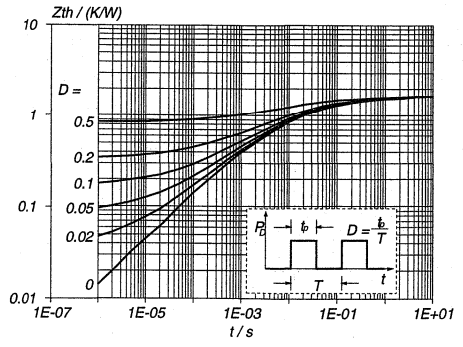


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

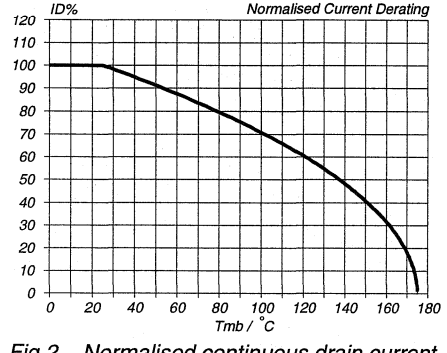


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\ 25\ °C} = f(T_{mb})$; *conditions:* $V_{GS} \geq 10$ V

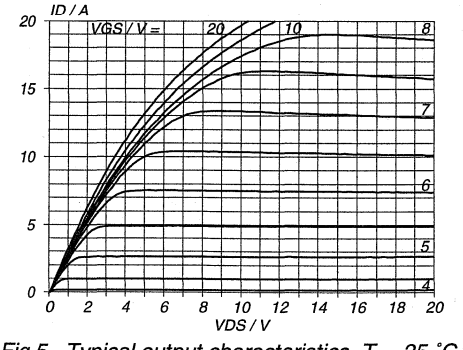


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; *parameter* V_{GS}

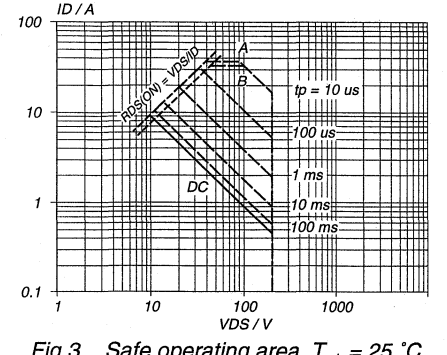


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

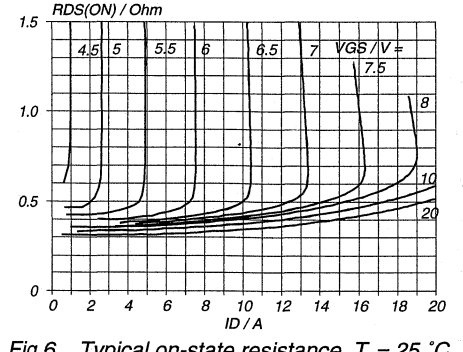


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; *parameter* V_{GS}

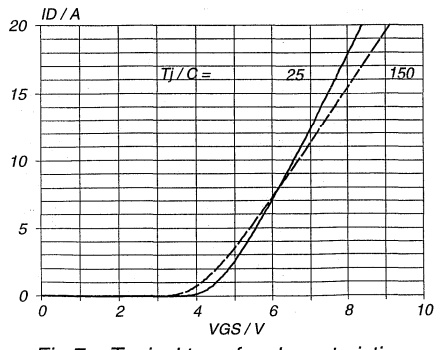


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

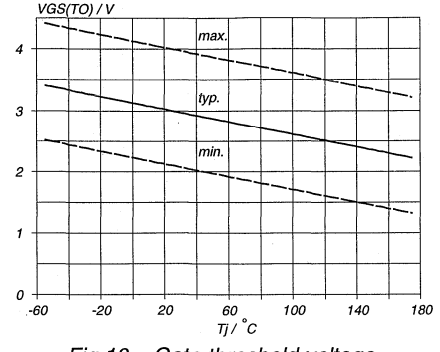


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

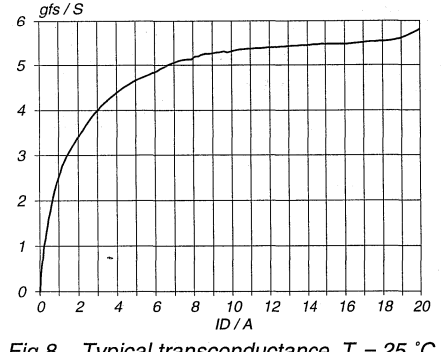


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

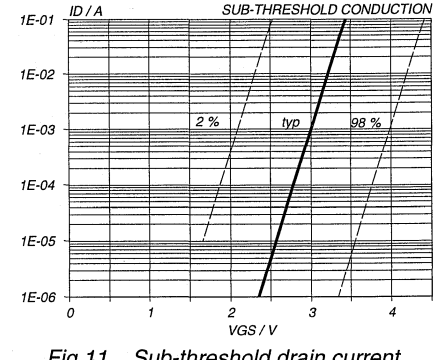


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

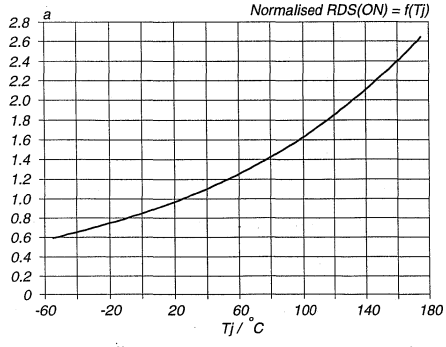


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 3.5$ A; $V_{GS} = 10$ V

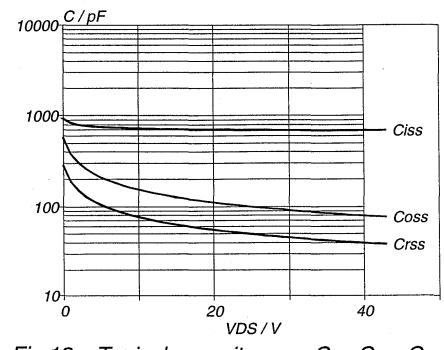


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

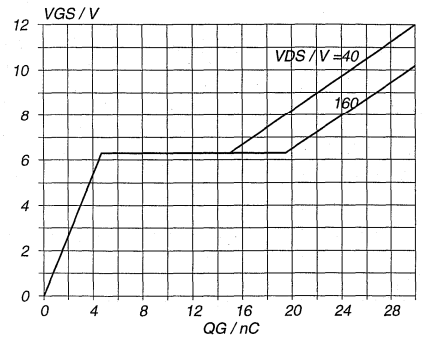


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 9$ *A; parameter* V_{DS}

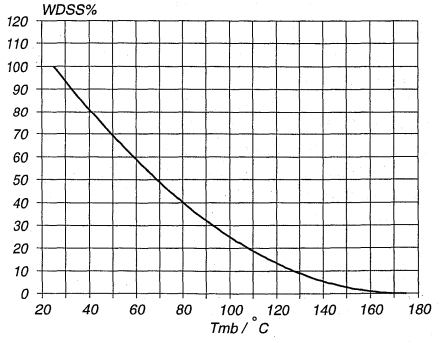


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 9$ *A*

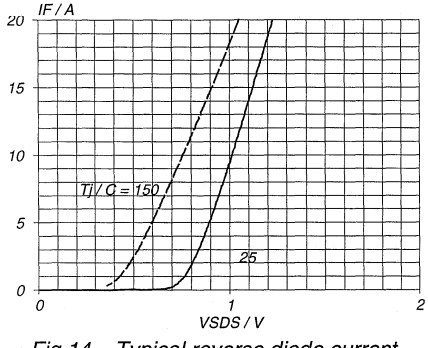


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ *V; parameter* T_j

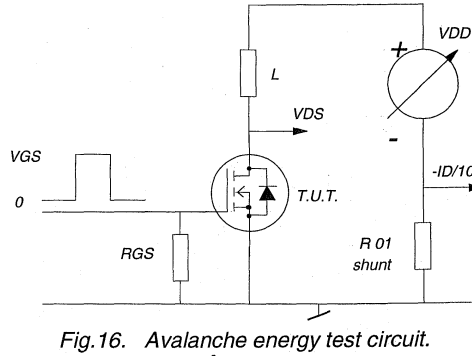


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

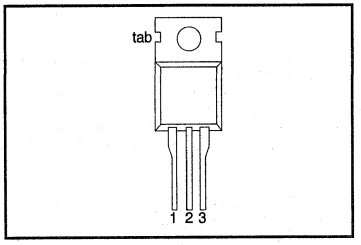
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK454	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	2.4	2.0	A
P_{tot}	Total power dissipation	85	85	W
$R_{DS(ON)}$	Drain-source on-state resistance	6	8	Ω

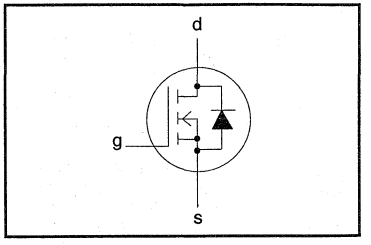
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	2.4	2.0	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	1.5	1.25	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	9.5	8	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.47	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK454-800A**	-	5	6	Ω
		I_D = 1.0 A **BUK454-800B**	-	6	8	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.0 A	1.0	2.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	450	750	pF
C_{oss}	Output capacitance		-	42	70	pF
C_{rss}	Feedback capacitance		-	15	30	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1.9 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	2.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	10	A
V_{SD}	Diode forward voltage	I_F = 2.6 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 2.6 A; -dI_F/dt = 100 A/µs;	-	230	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.9	-	µC

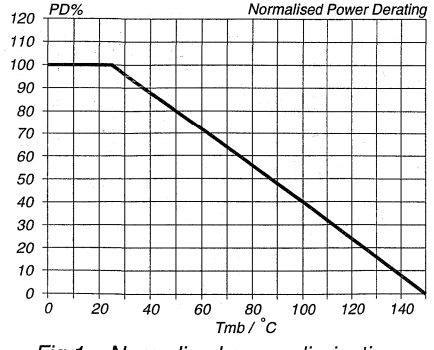


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

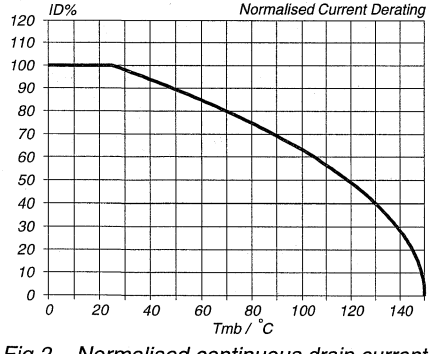


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

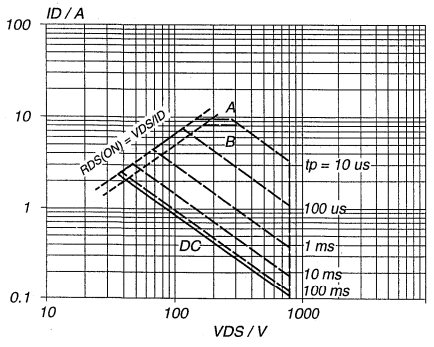


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

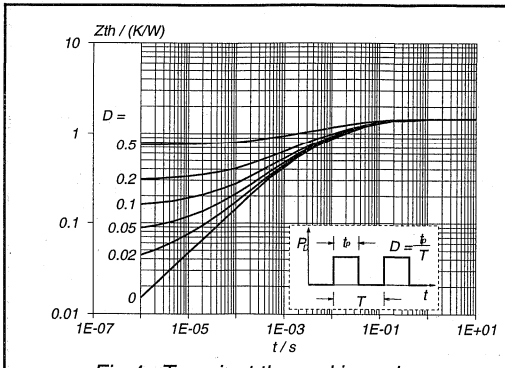


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

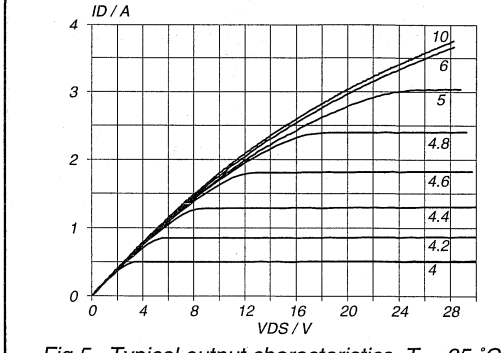


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

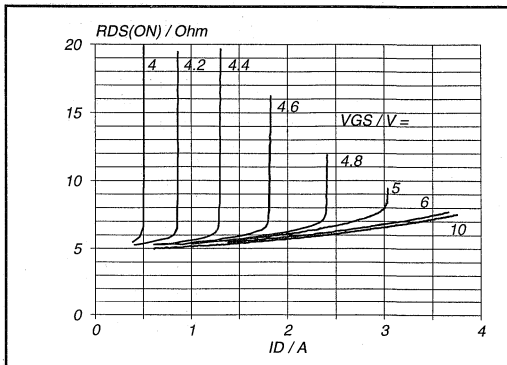


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

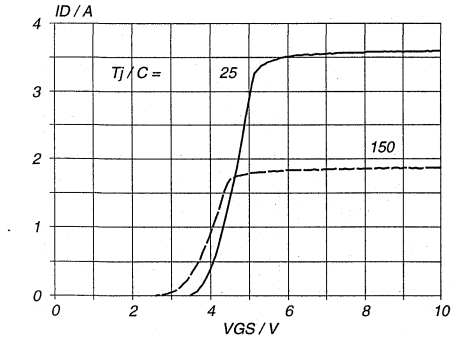


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

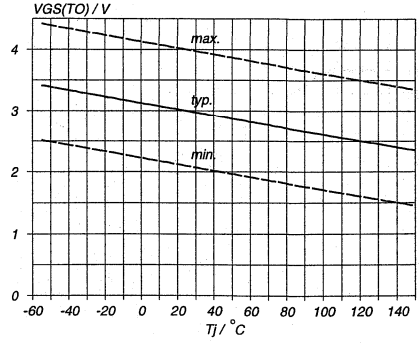


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

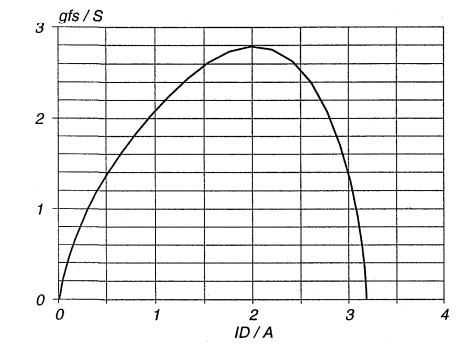


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

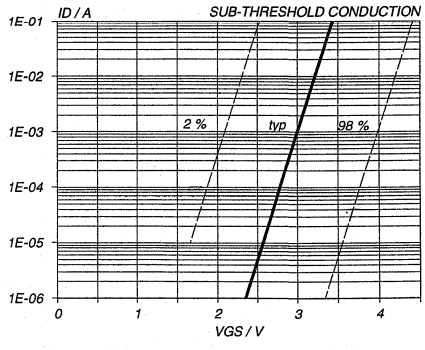


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

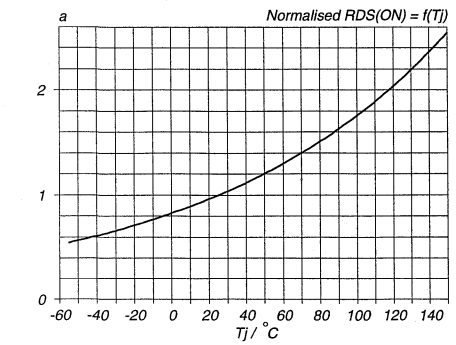


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 1.0 A; V_{GS} = 10 V

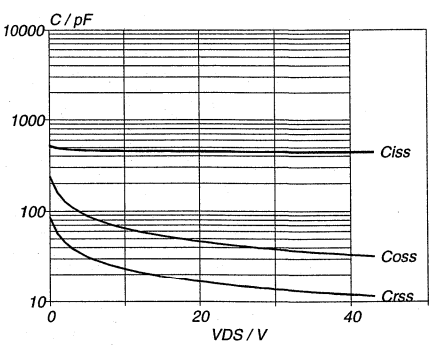


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

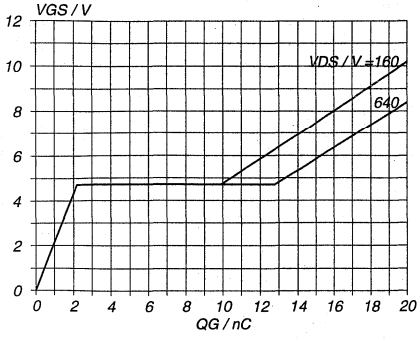


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2.4$ A; parameter V_{DS}

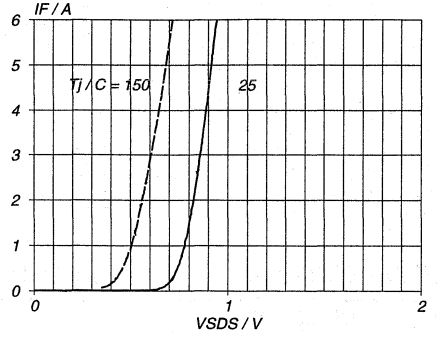


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

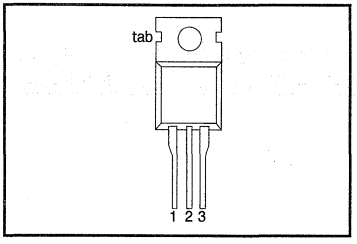
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK455	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	41	38	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.038	0.045	Ω

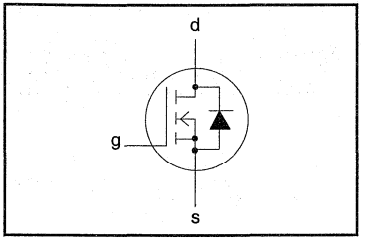
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	38	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	27	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	152	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK455-60A**	-	0.03	0.038	Ω
		I_D = 20 A **BUK455-60B**	-	0.04	0.045	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	8	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	560	750	pF
C_{rss}	Feedback capacitance		-	300	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	125	160	ns
t_f	Turn-off fall time		-	100	130	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	1.4	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

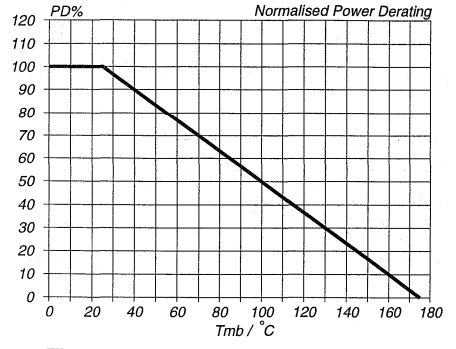


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

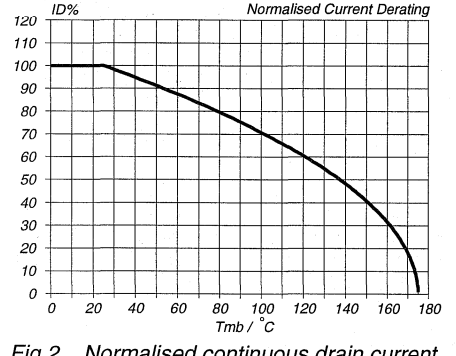


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

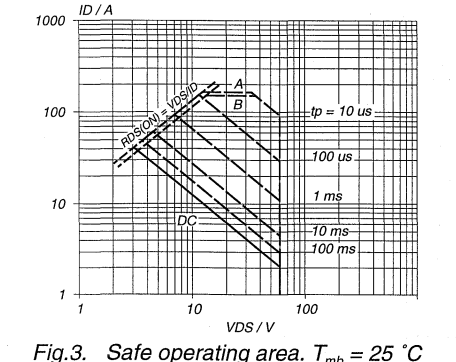


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

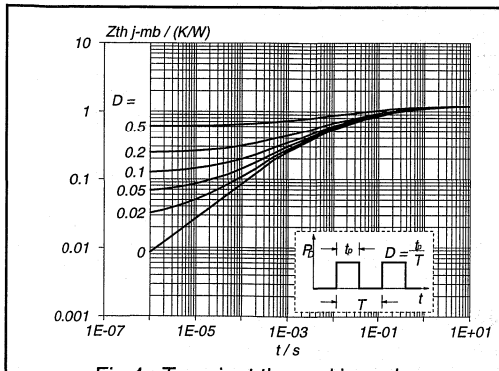


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

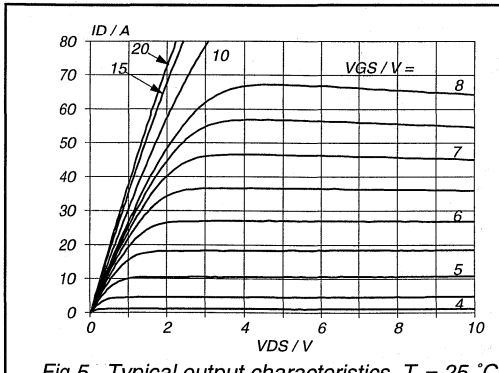


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

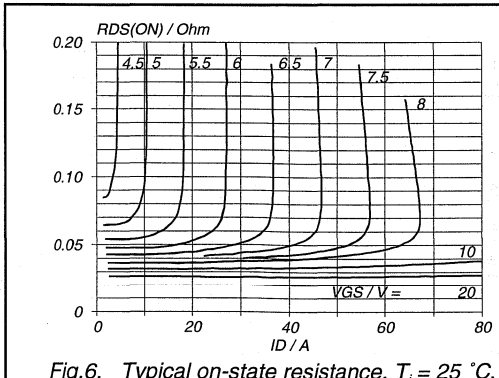


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

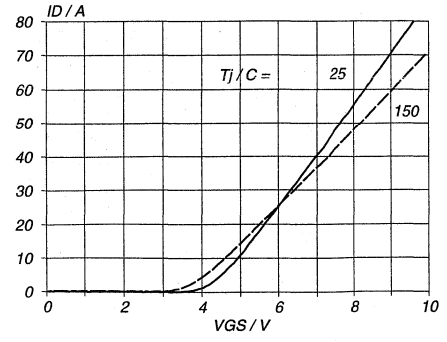


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

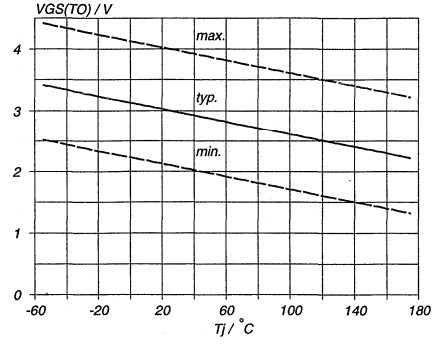


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

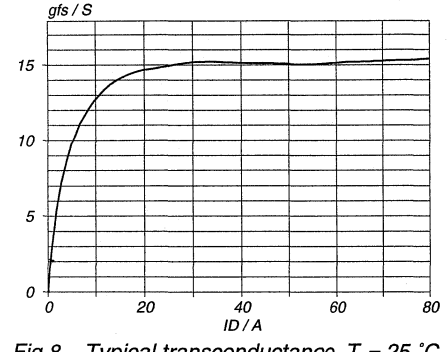


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

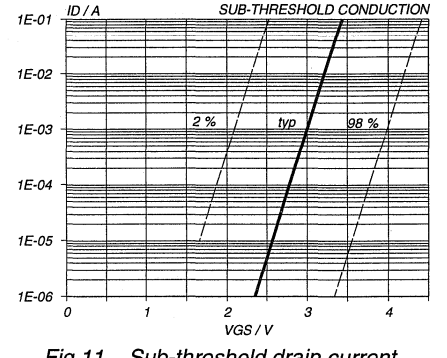


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

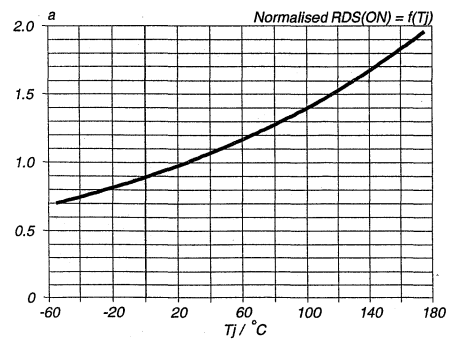


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

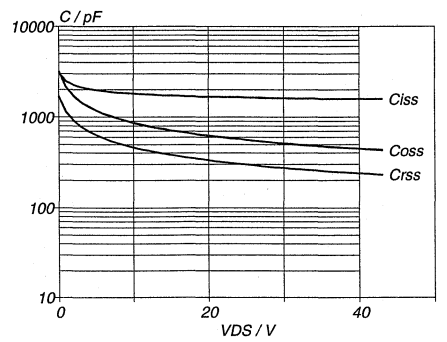


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

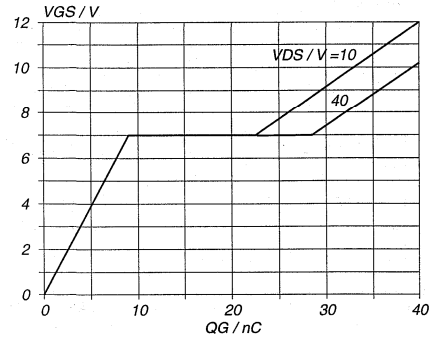


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

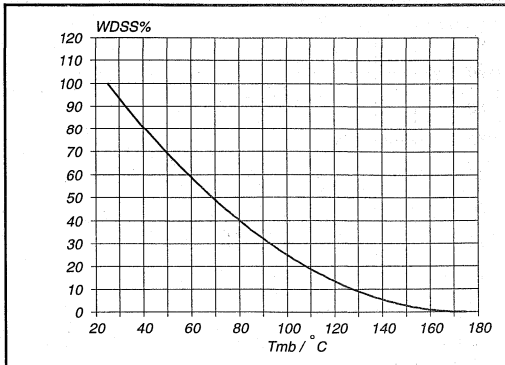


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

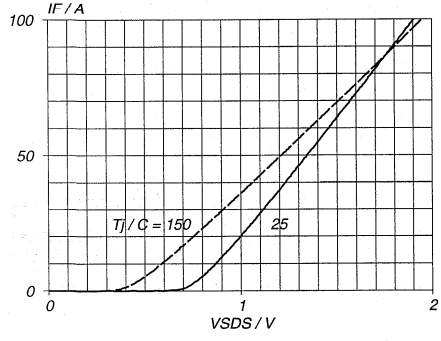


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

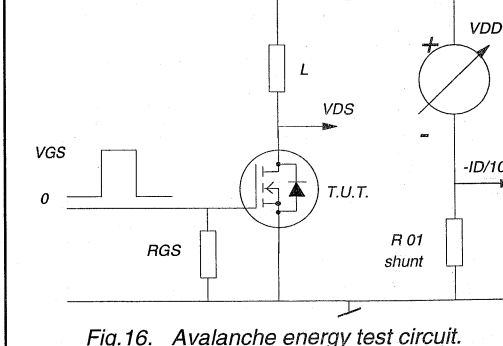


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — BUK455-60H

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

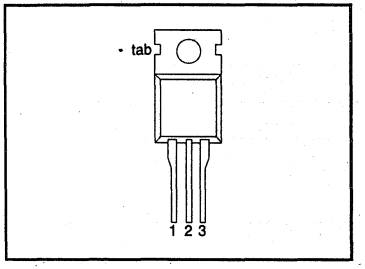
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	30	mΩ

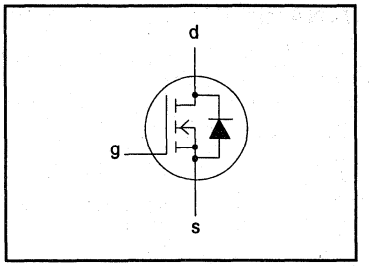
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	32	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	172	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	24	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	8	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1600	pF
C_{oss}	Output capacitance		-	470	600	pF
C_{rss}	Feedback capacitance		-	180	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	125	160	ns
t_f	Turn-off fall time		-	100	130	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	45	A
I_{DRM}	Pulsed reverse drain current	-	-	-	172	A
V_{SD}	Diode forward voltage	I_F = 43 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 43 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 43 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

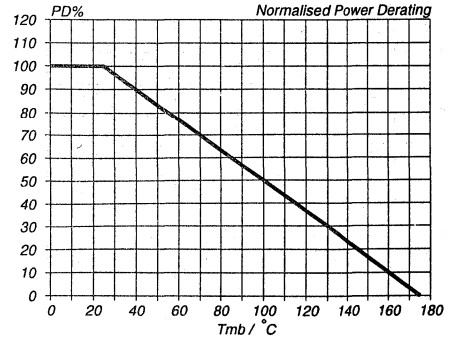


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

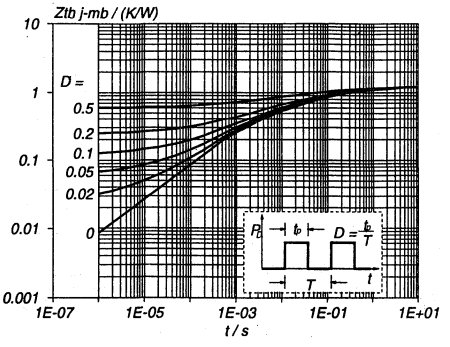


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

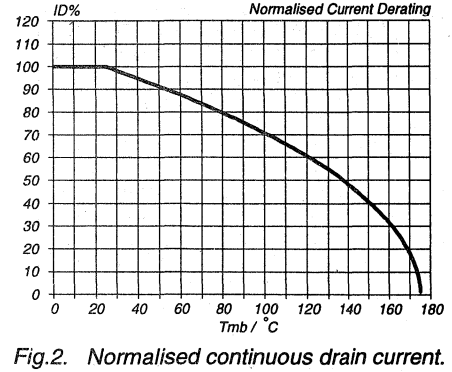


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

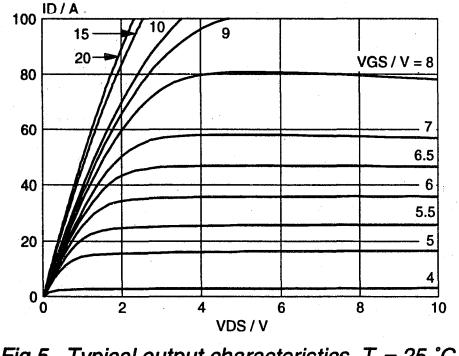


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

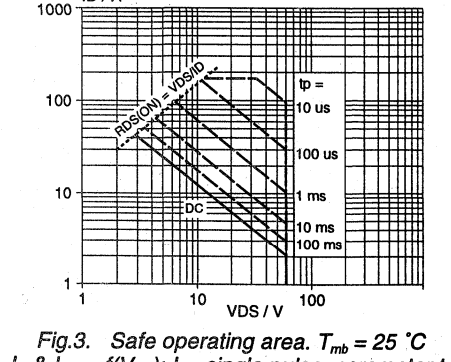


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

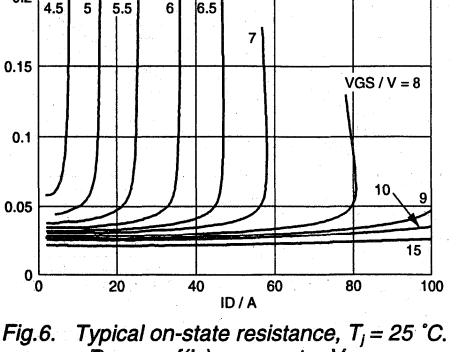


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

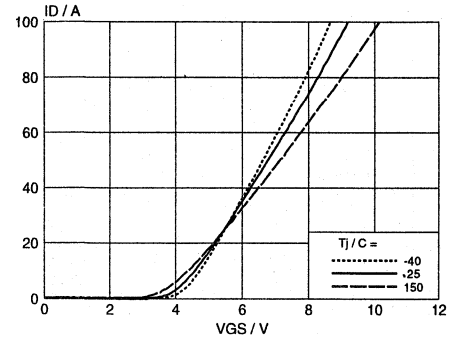


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

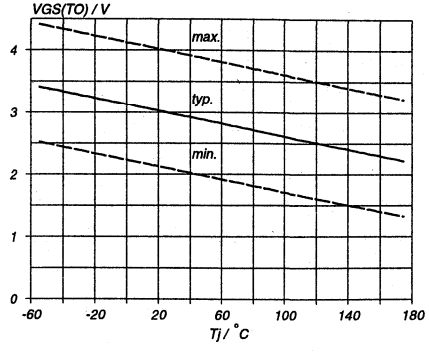


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

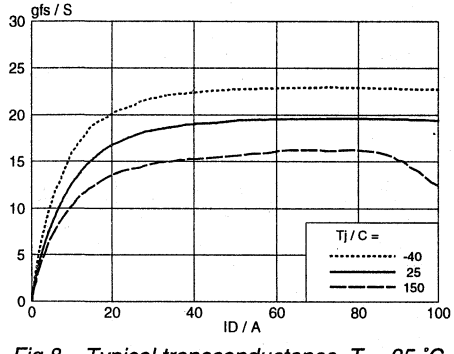


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V

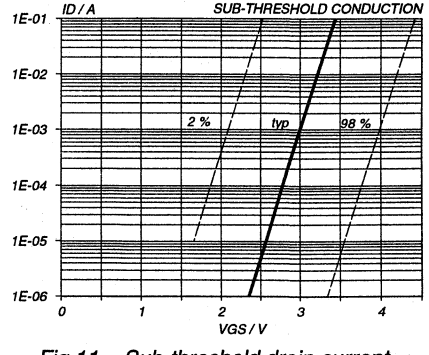


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

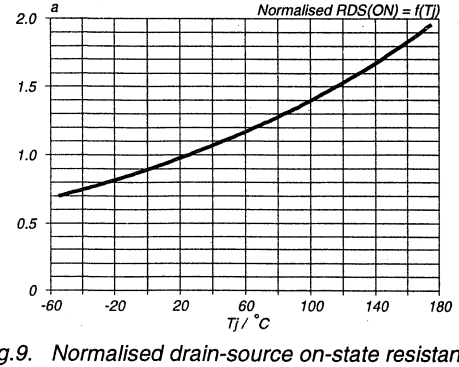


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

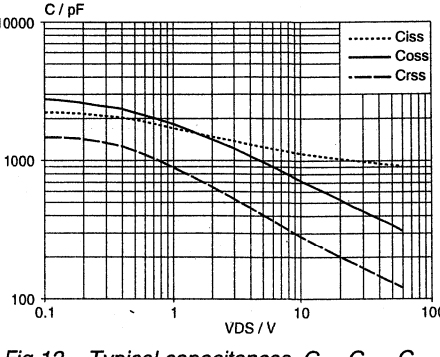


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

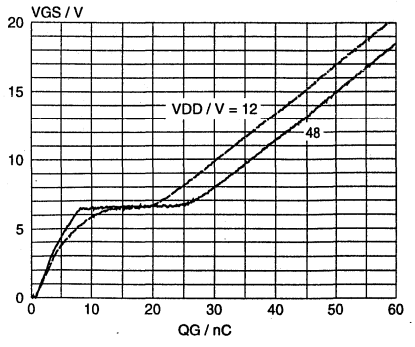


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 43$ A; parameter V_{DS}

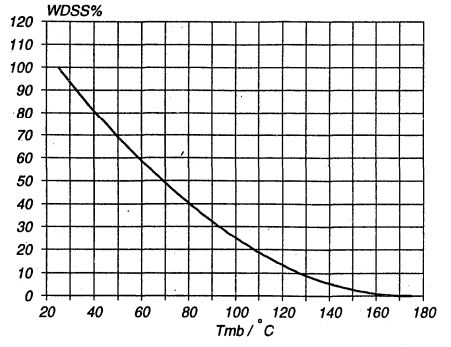


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 43$ A

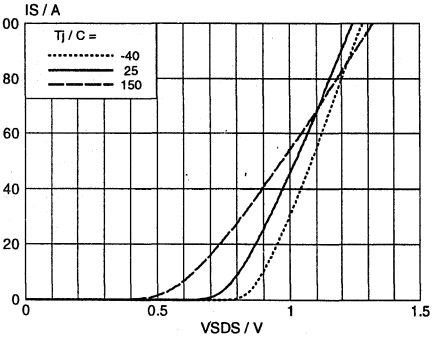


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

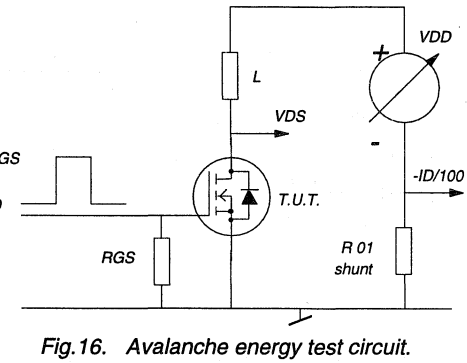


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor — BUK455-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

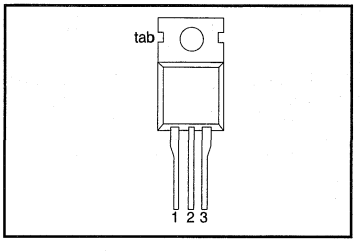
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK455	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	26	23	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	0.1	Ω

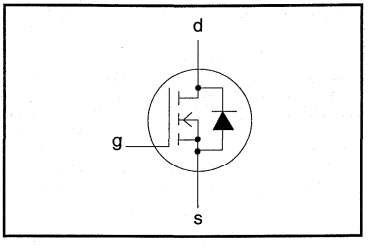
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	26	23	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	16	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	104	92	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK455-100A**	-	0.07	0.08	Ω
		I_D = 13 A **BUK455-100B**	-	0.08	0.1	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	7.0	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	350	500	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	100	160	ns
t_f	Turn-off fall time		-	50	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	26	A
I_{DRM}	Pulsed reverse drain current	-	-	-	104	A
V_{SD}	Diode forward voltage	I_F = 26 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 26 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 26 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

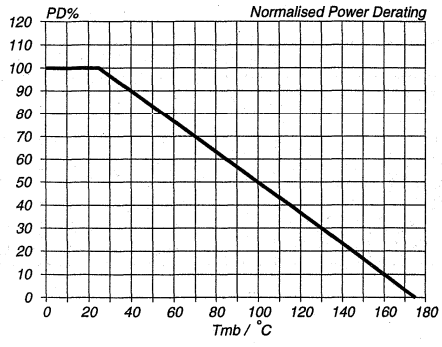


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

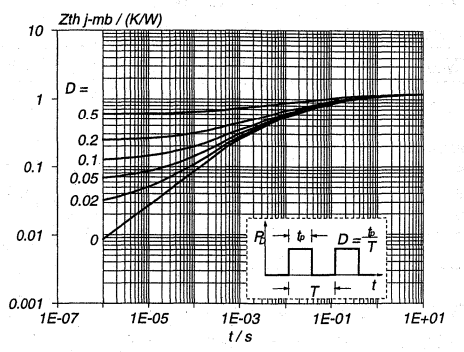


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

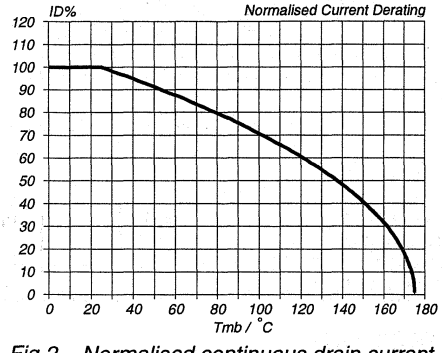


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

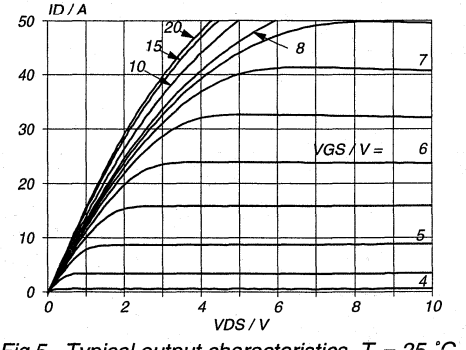


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

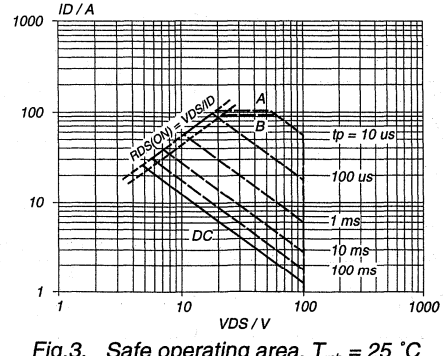


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

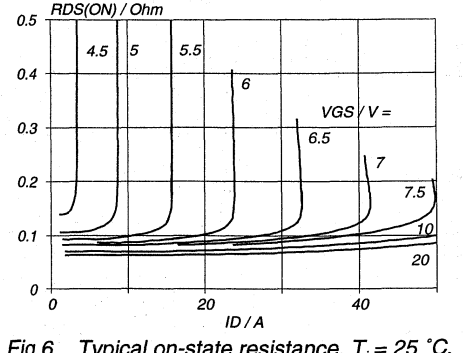


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

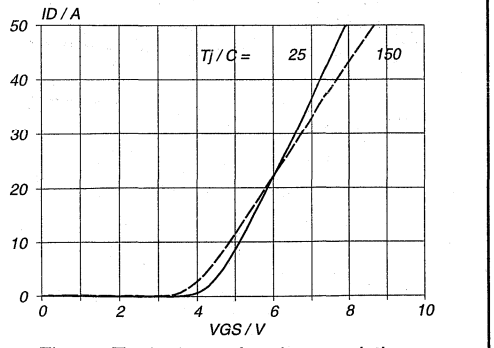


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

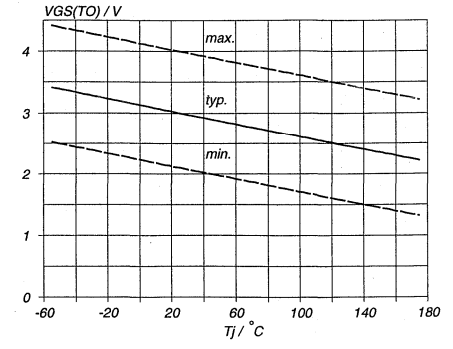


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

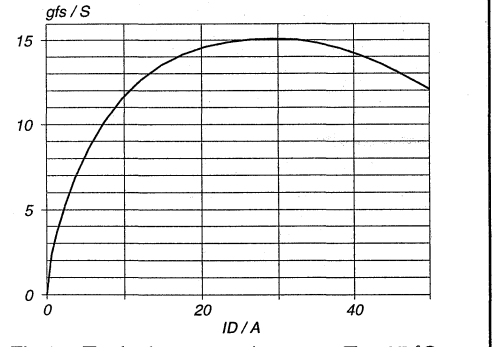


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

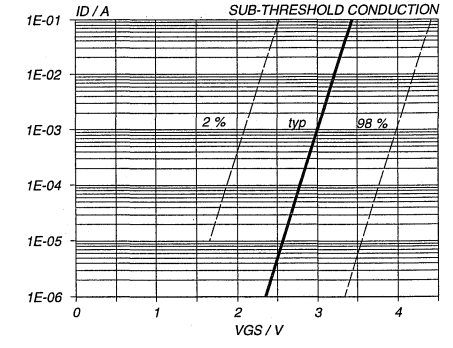


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

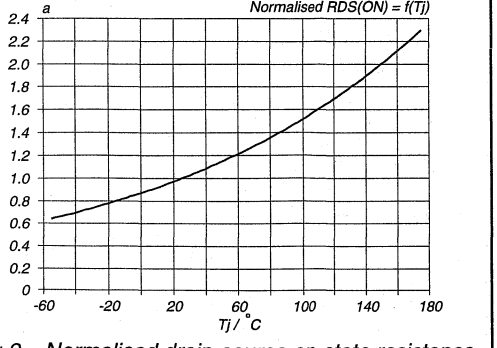


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 13 A; V_{GS} = 10 V

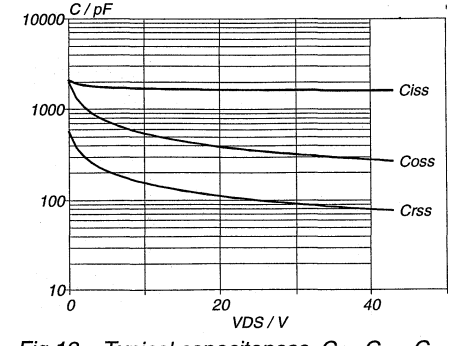


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

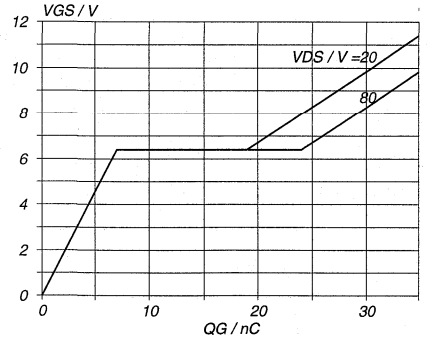


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 26 A; parameter V_{DS}

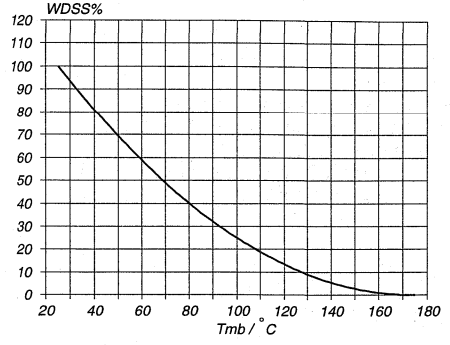


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 26 A

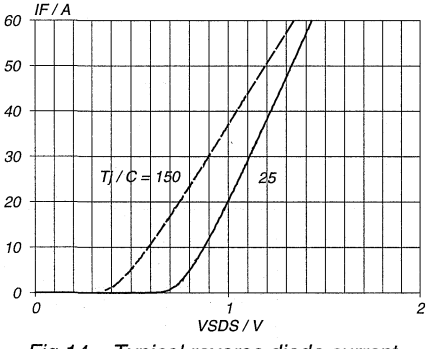


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

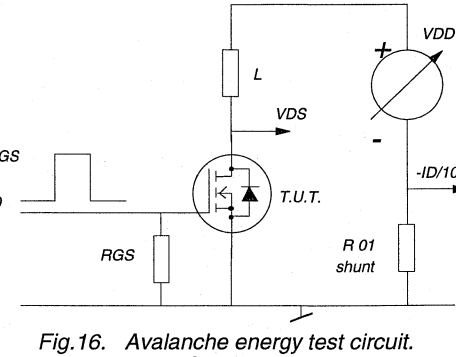


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

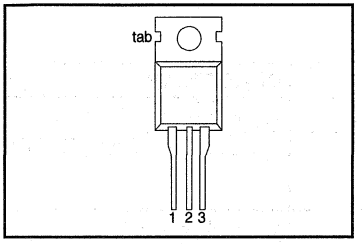
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK455	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance;	0.23	0.28	Ω

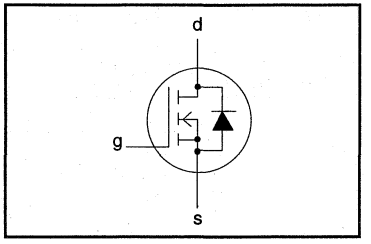
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK455-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK455-200B**	-	0.22	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6.0	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 30 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

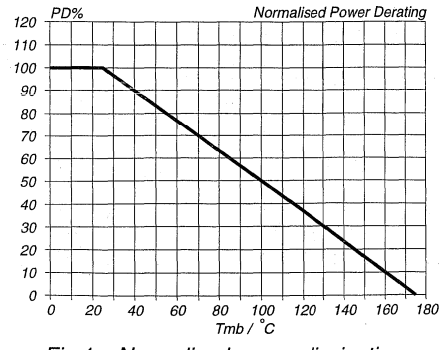


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

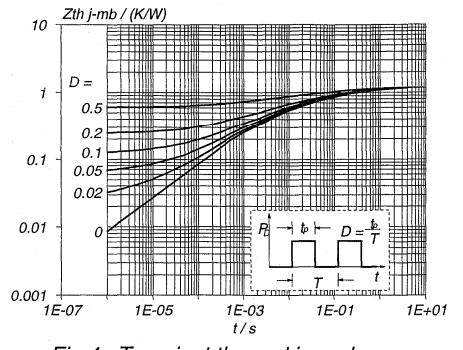


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

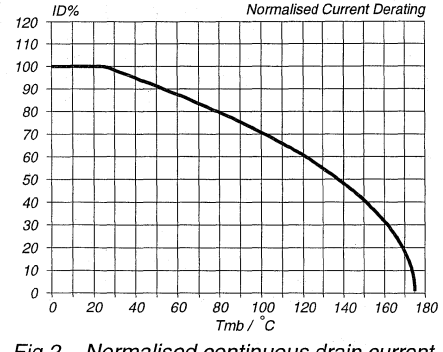


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

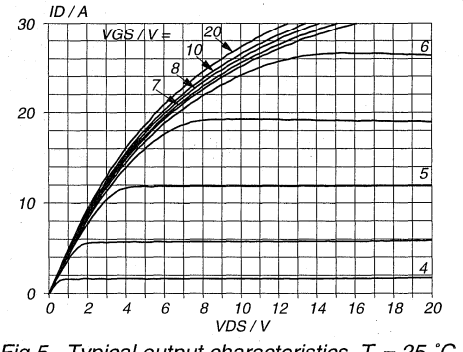


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

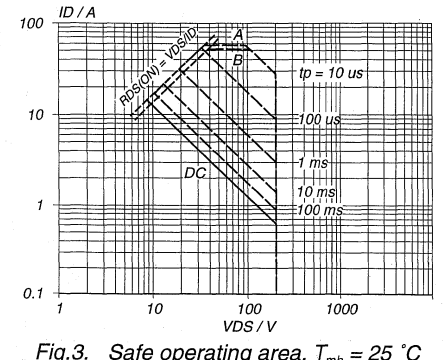


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

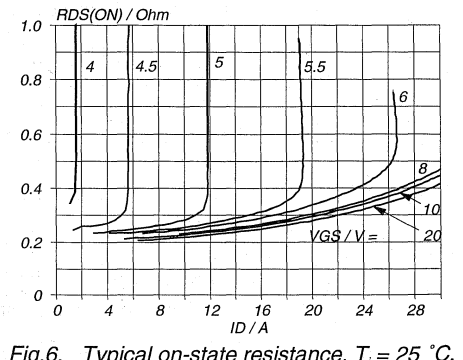


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

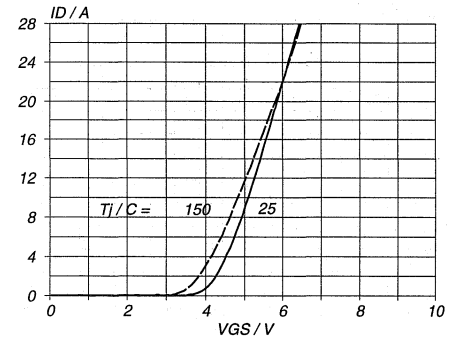


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

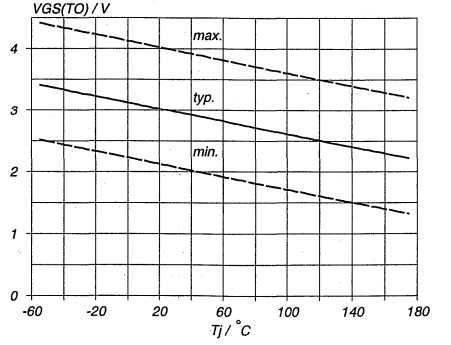


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

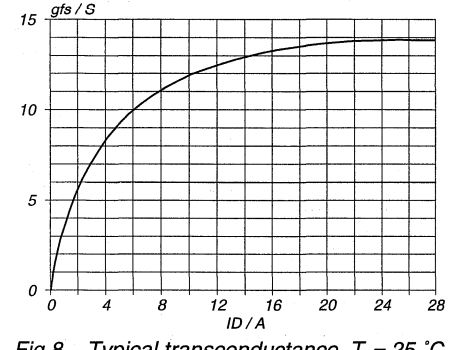


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

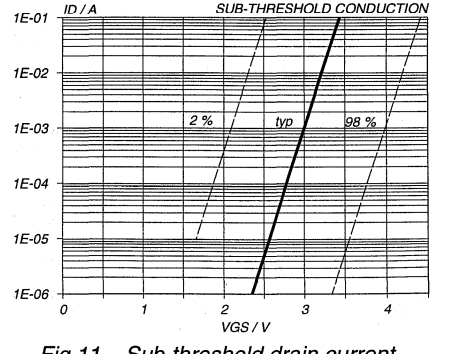


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

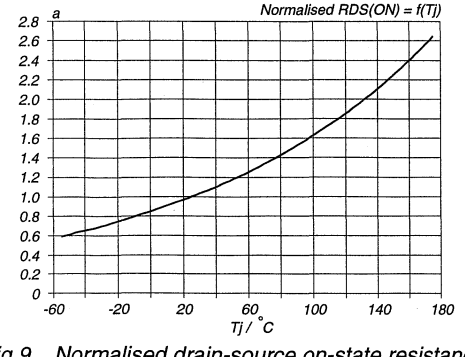


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 7 A; V_{GS} = 10 V

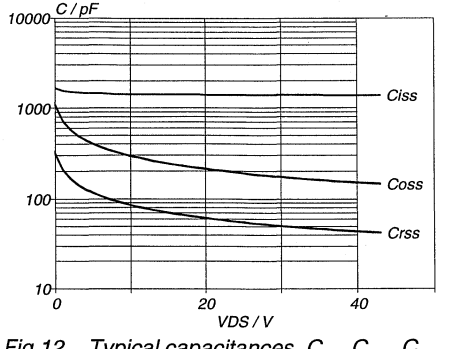


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

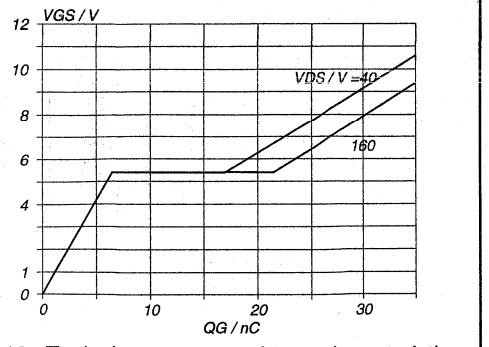


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

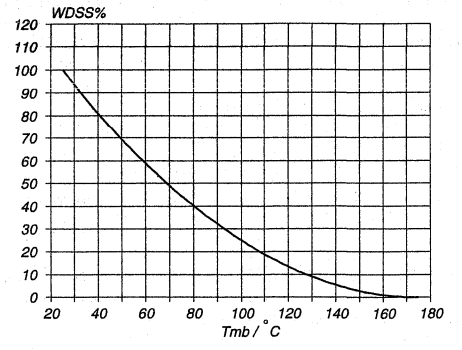


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

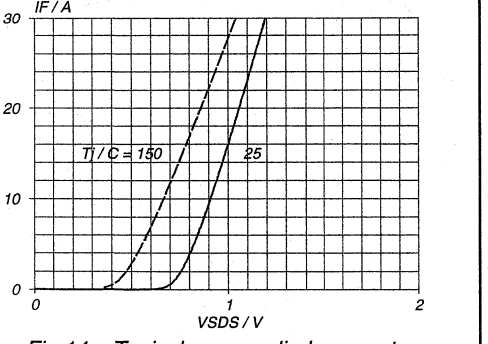


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

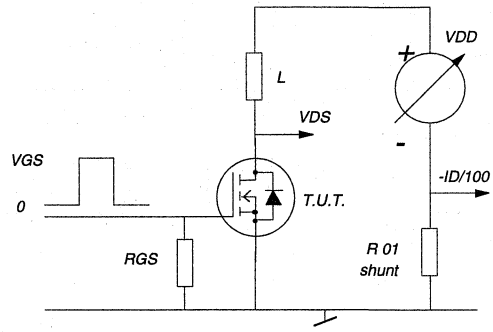


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

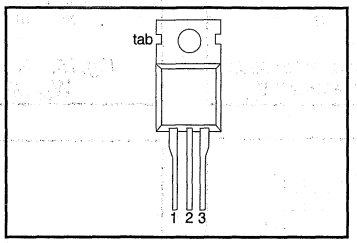
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK456	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	52	51	A
P_{tot}	Total power dissipation	150	150	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.028	0.03	Ω

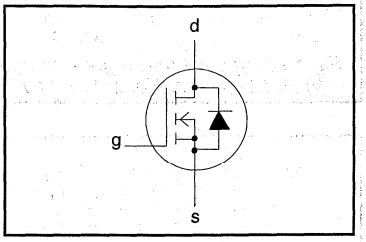
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	51	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	36	36	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	200	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK456-60A**	-	0.024	0.028	Ω
		I_D = 29 A **BUK456-60B**	-	0.027	0.030	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 29 A	17	22	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	800	1000	pF
C_{rss}	Feedback capacitance		-	270	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	70	100	ns
$t_{d\,off}$	Turn-off delay time	R_{GS} = 50 Ω;	-	170	220	ns
t_f	Turn-off fall time	R_{gen} = 50 Ω	-	120	160	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	52	A
I_{DRM}	Pulsed reverse drain current	-	-	-	208	A
V_{SD}	Diode forward voltage	I_F = 52 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 52 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.4	-	µC

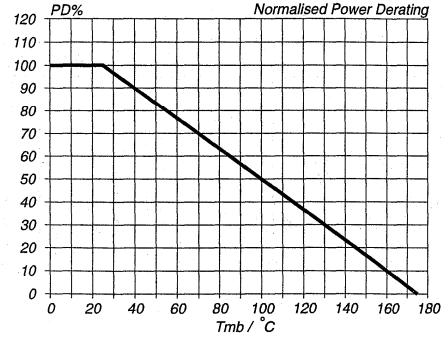


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

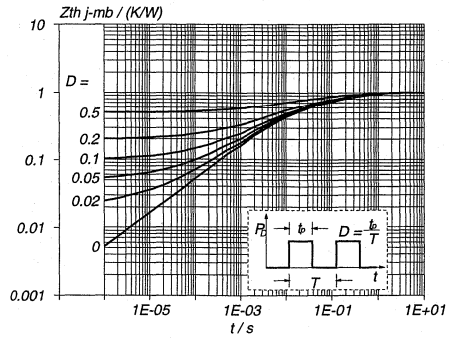


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

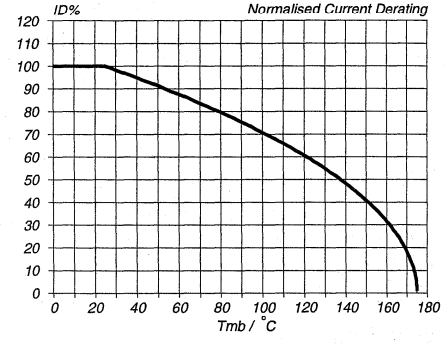


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

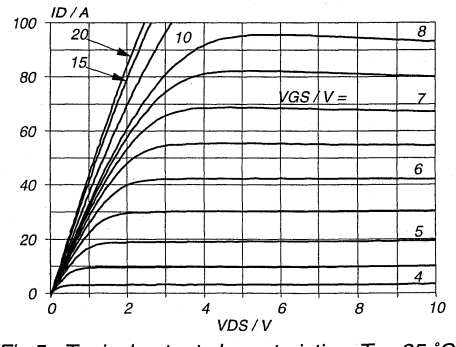


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

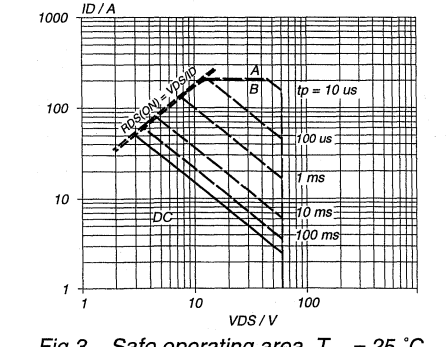


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

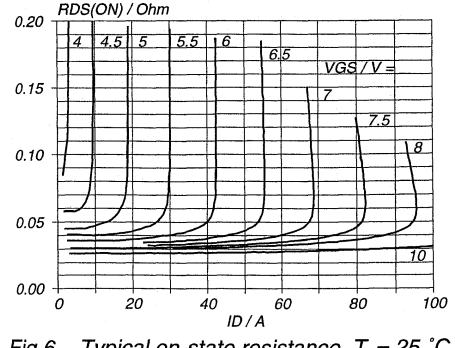


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

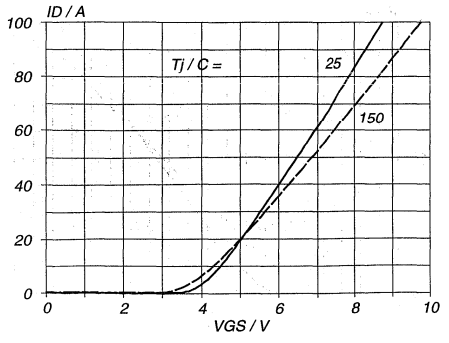


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

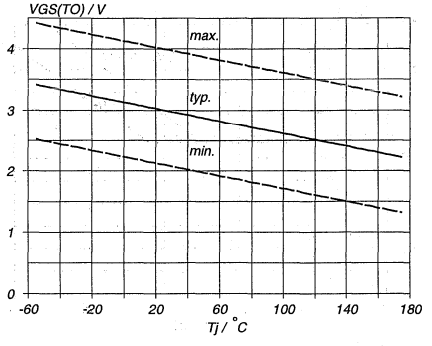


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

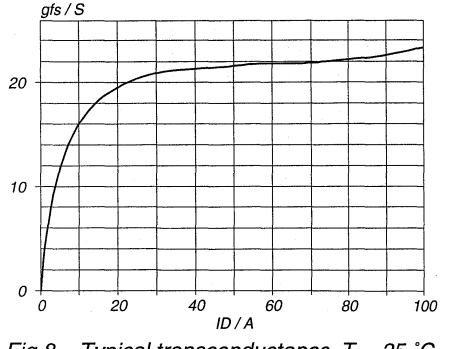


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

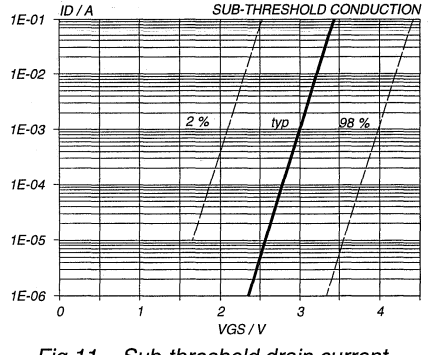


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

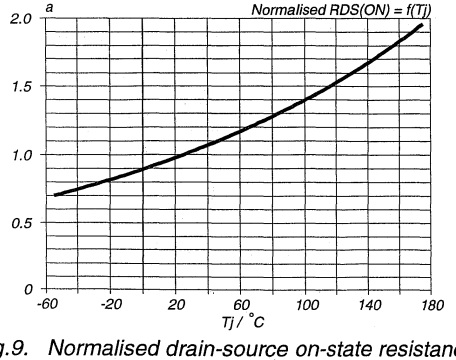


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 29 A; V_{GS} = 10 V

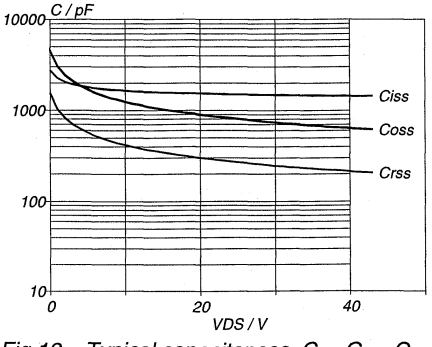


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

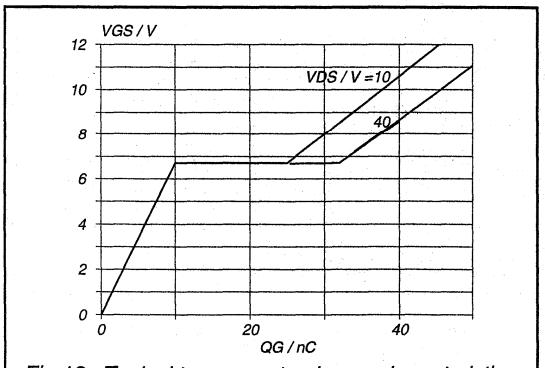


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 52$ A; parameter V_{DS}

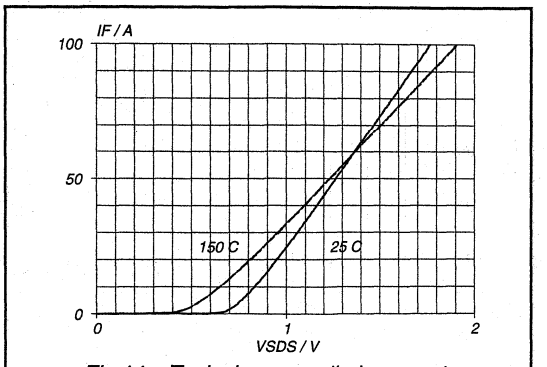


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Automotive and general purpose switching applications.

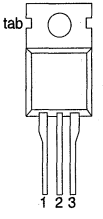
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	60	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	20	mΩ

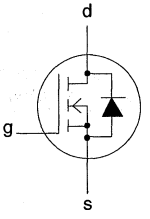
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	60	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	46	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	-	-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	17	20	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	17	22	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1600	2200	pF
C_{oss}	Output capacitance		-	800	1000	pF
C_{rss}	Feedback capacitance		-	310	450	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	30	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	90	120	ns
$t_{d\,off}$	Turn-off delay time	R_{GS} = 50 Ω;	-	190	250	ns
t_f	Turn-off fall time	R_{gen} = 50 Ω	-	140	180	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	50	A
I_{DRM}	Pulsed reverse drain current	-	-	-	200	A
V_{SD}	Diode forward voltage	I_F = 50 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	80	250	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	150	mJ

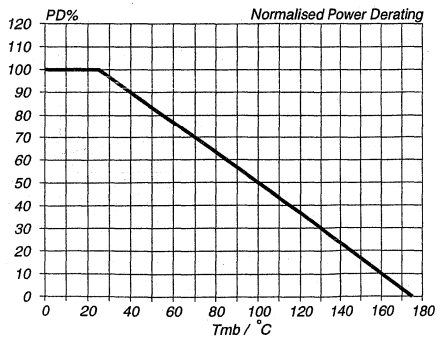


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

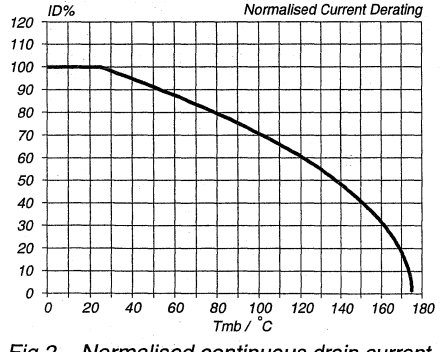


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

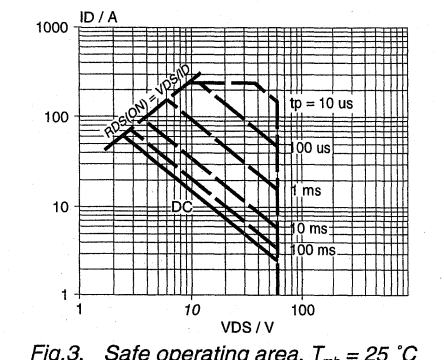


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

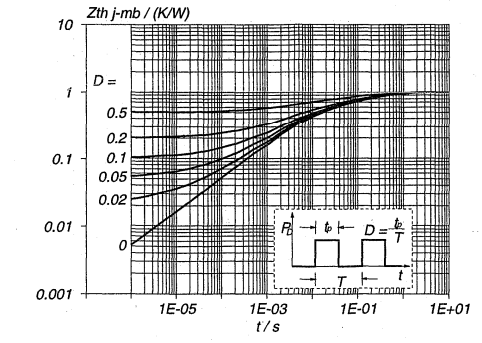


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

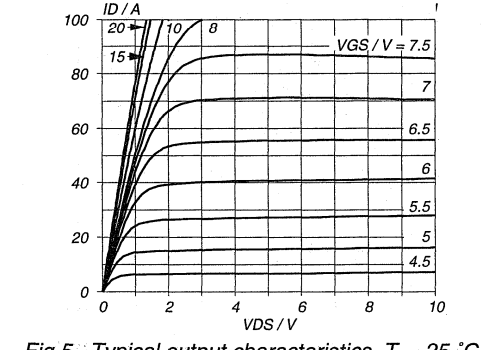


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

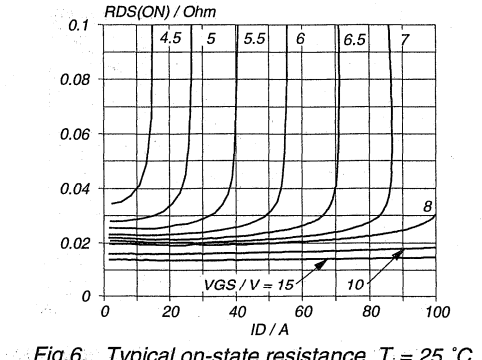


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

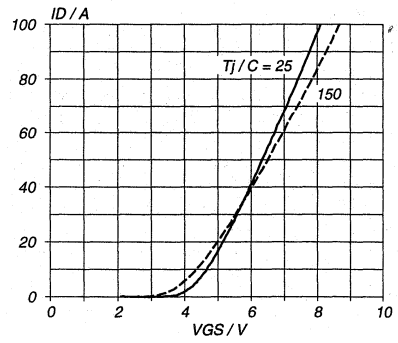


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

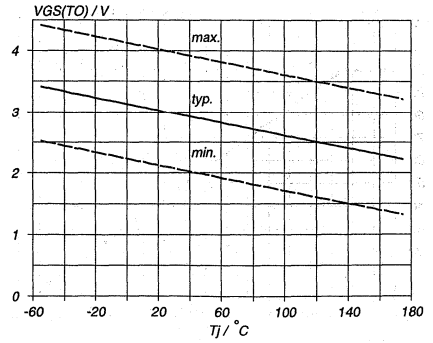


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

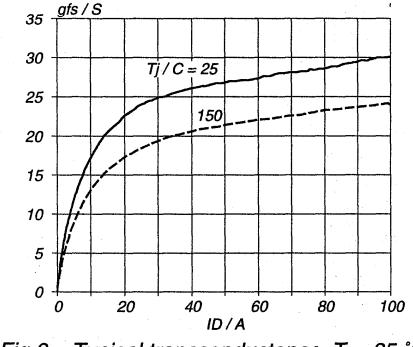


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

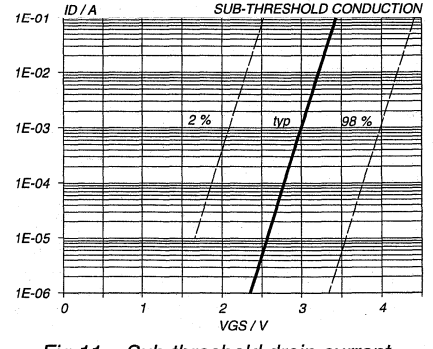


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

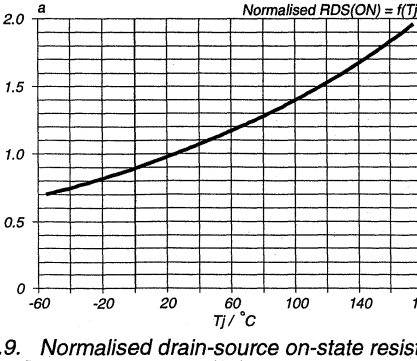


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

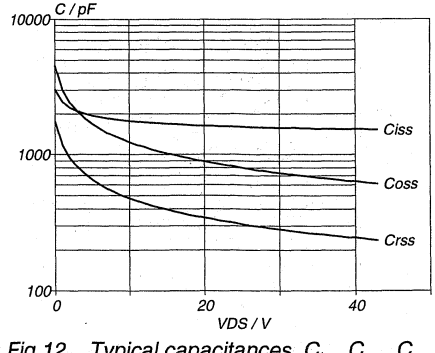


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

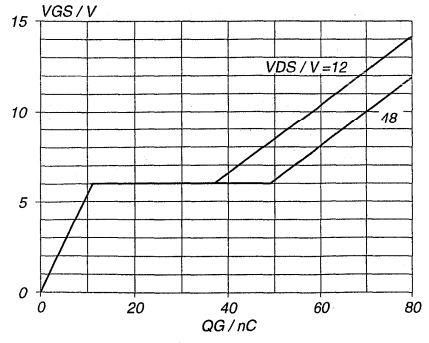


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

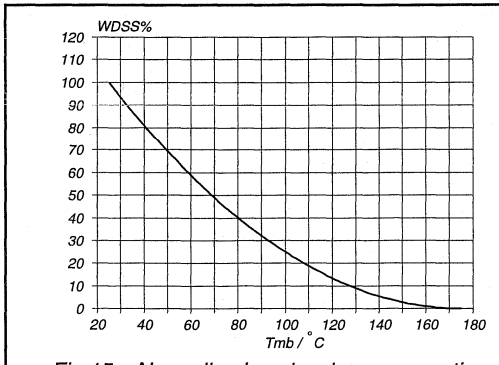


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 50$ A

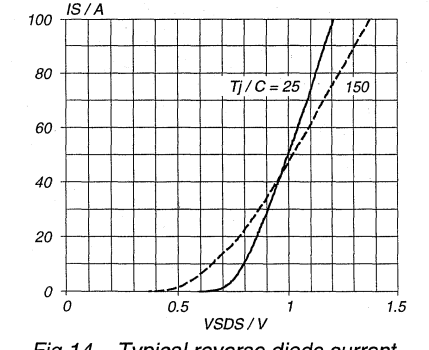


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

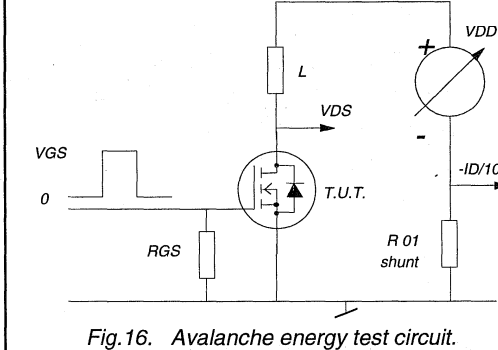


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

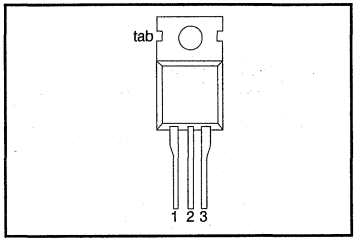
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK456	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	34	32	A
P_{tot}	Total power dissipation	150	150	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.057	0.065	Ω

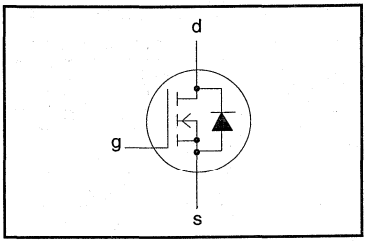
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	32	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	22	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	128	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK456-100A**	-	0.052	0.057	Ω
		I_D = 15 A **BUK456-100B**	-	0.06	0.065	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	450	600	pF
C_{rss}	Feedback capacitance		-	130	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	150	200	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	65	85	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	34	A
I_{DRM}	Pulsed reverse drain current	-	-	-	136	A
V_{SD}	Diode forward voltage	I_F = 34 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.0	-	µC

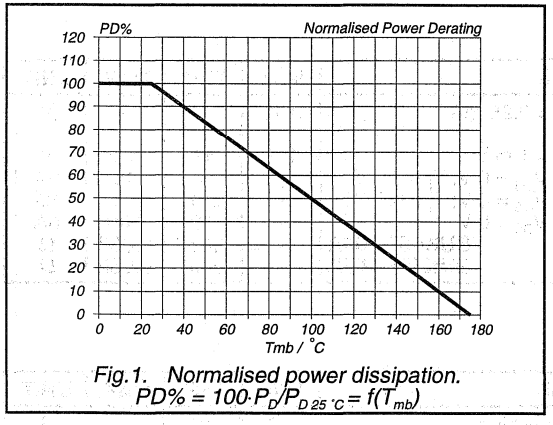


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

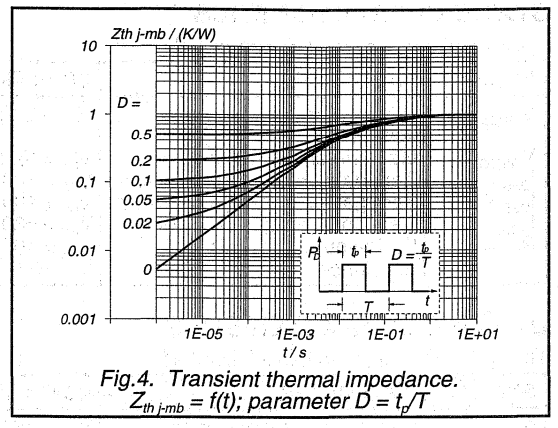


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

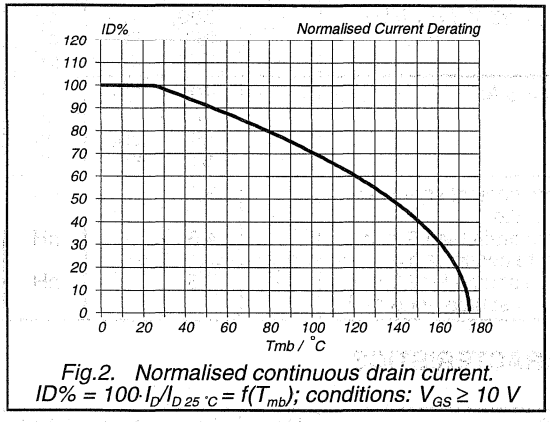


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

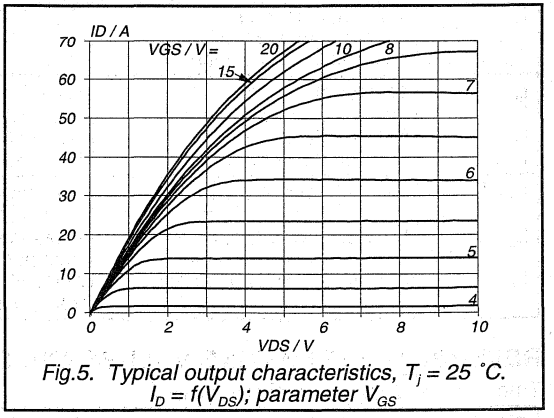


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

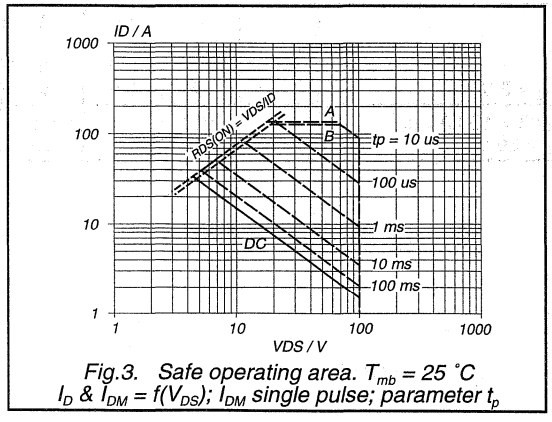


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

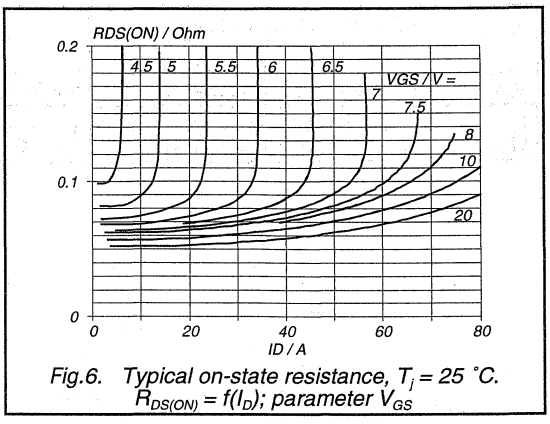


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

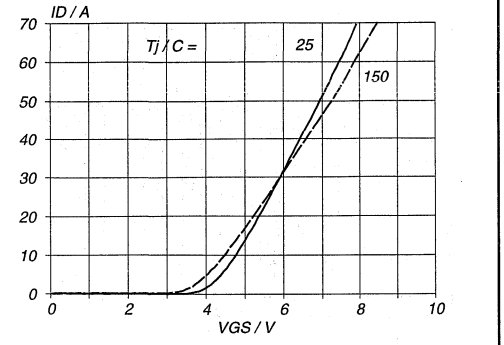


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

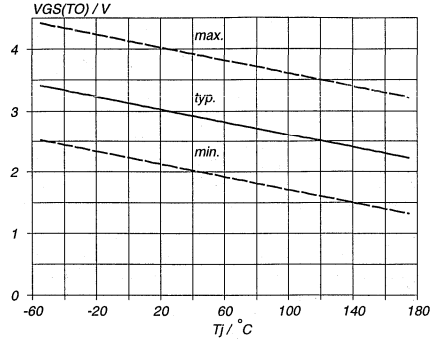


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

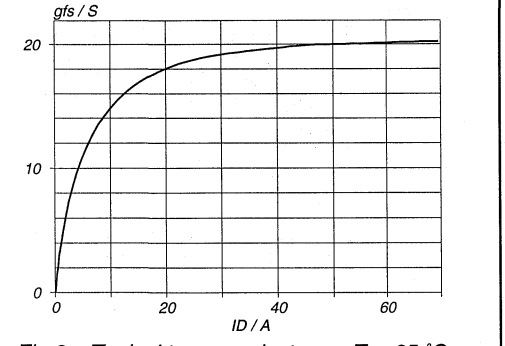


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

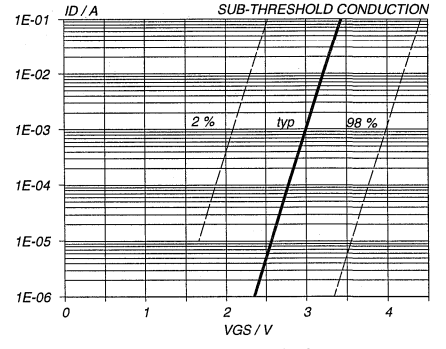


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

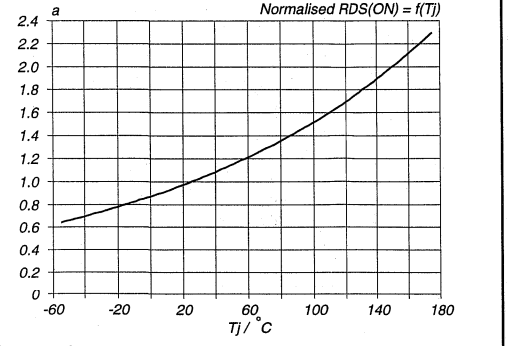


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 15 A; V_{GS} = 10 V

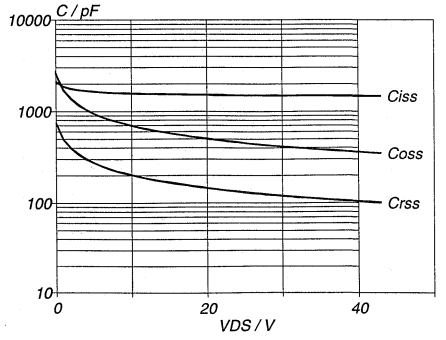


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

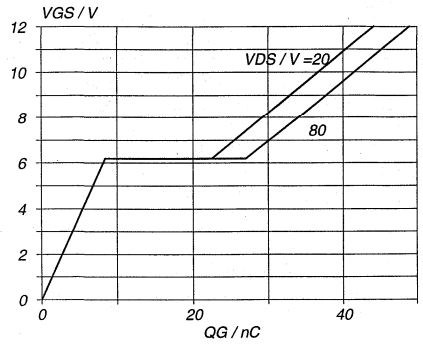


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 34$ A; parameter V_{DS}

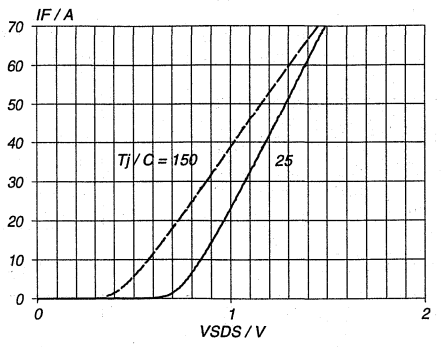


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

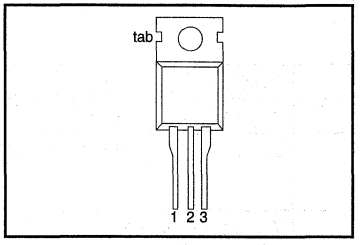
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK456	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	19	17	A
P_{tot}	Total power dissipation	150	150	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.2	Ω

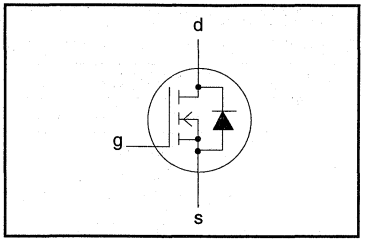
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19	17	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13	12	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	76	68	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK456-200A**	-	0.15	0.16	Ω
		I_D = 10 A **BUK456-200B**	-	0.18	0.20	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	8.5	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	400	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	145	185	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	50	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	19	A
I_{DRM}	Pulsed reverse drain current	-	-	-	76	A
V_{SD}	Diode forward voltage	I_F = 19 A ; V_{GS} = 0 V	-	1.0	1.7	V
t_{rr}	Reverse recovery time	I_F = 19 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	2.5	-	µC

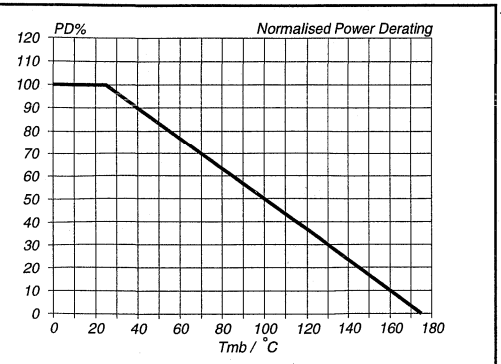


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

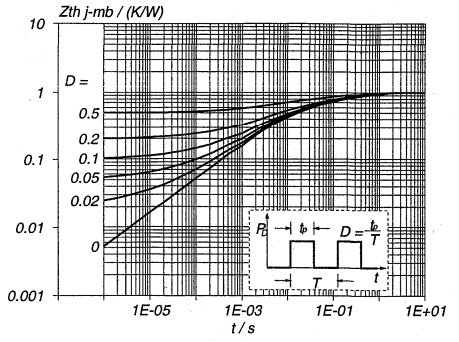


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

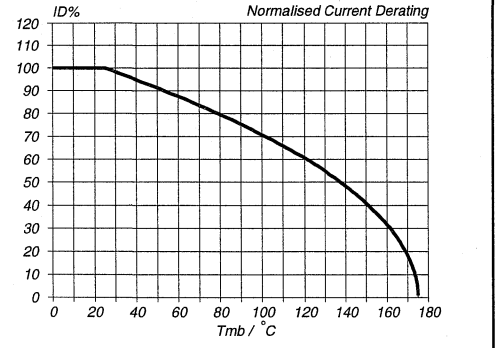


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

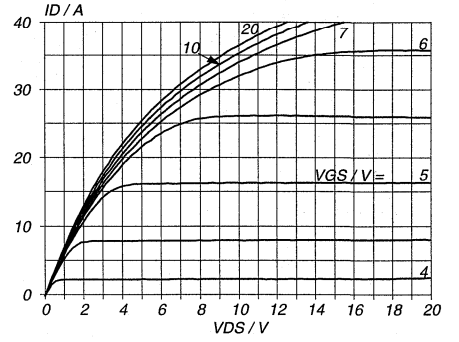


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

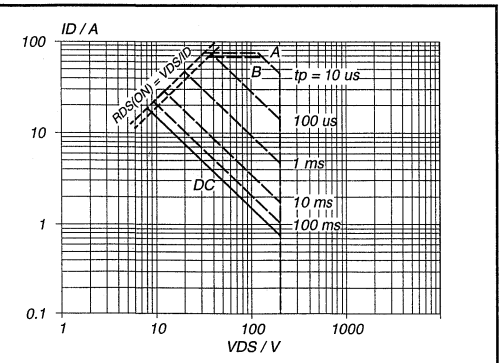


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

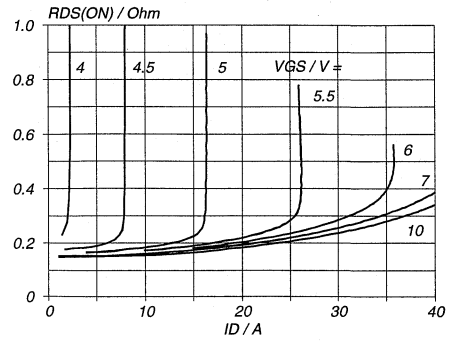


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

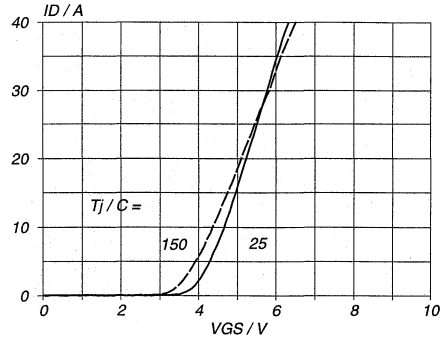


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

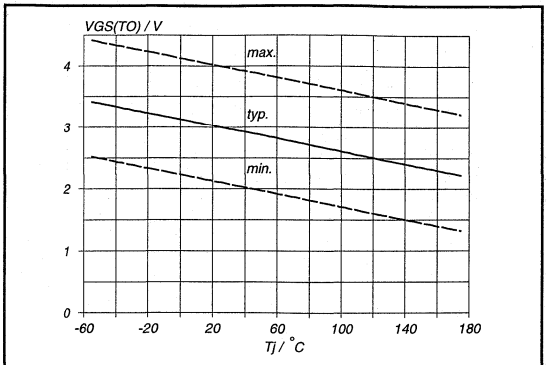


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

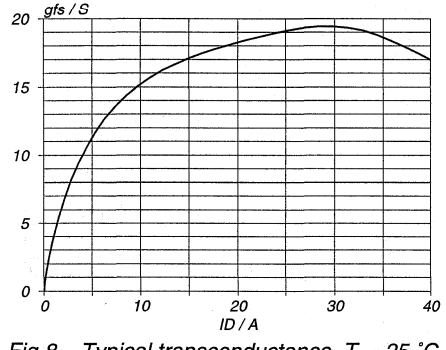


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

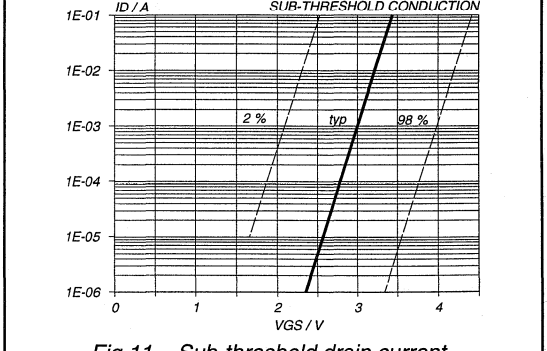


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

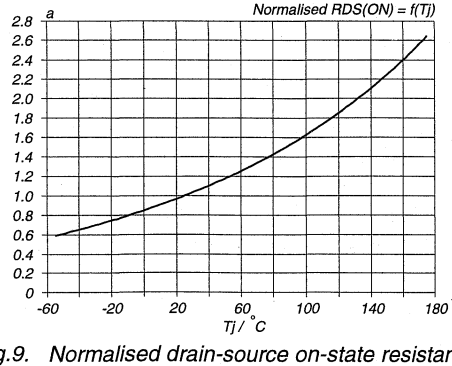


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

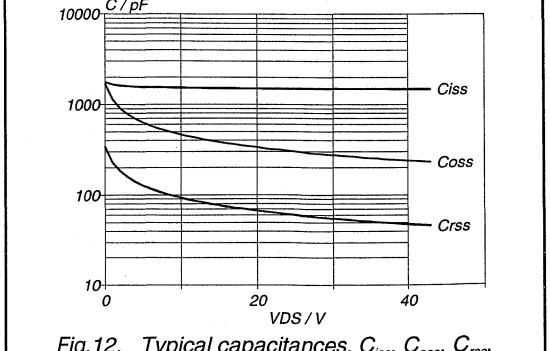


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

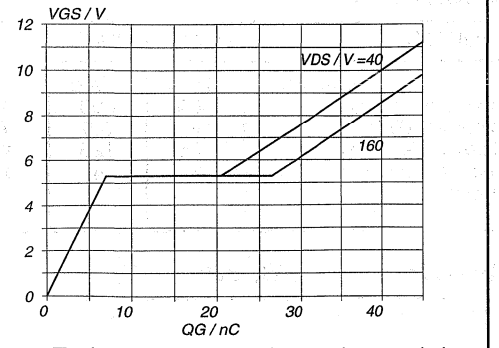


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 19 A; parameter V_{DS}

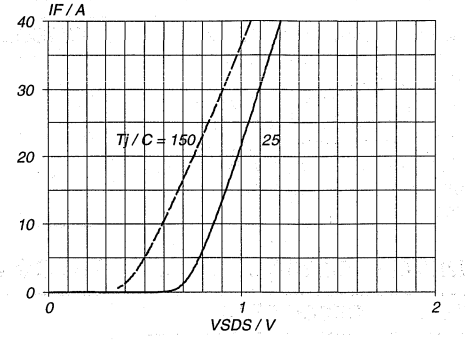


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

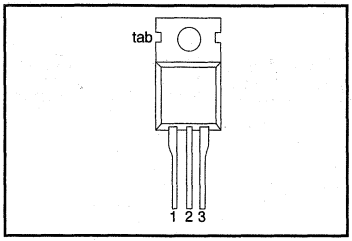
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK456	-800A	-800B	
V_{DS}	Drain-source voltage	800	800	V
I_D	Drain current (DC)	4	3.5	A
P_{tot}	Total power dissipation	125	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	3	4	Ω

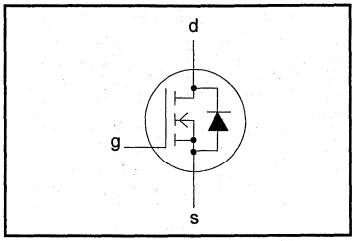
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	800		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	800		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-800A	-800B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	4.0	3.5	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	2.5	2.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	16	14	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	800	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK456-800A**	-	2.7	3.0	Ω
		I_D = 1.5 A **BUK456-800B**	-	3.5	4.0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	4.0	A
I_{DRM}	Pulsed reverse drain current	-	-	-	16	A
V_{SD}	Diode forward voltage	I_F = 4.0 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 4.0 A; -dI_F/dt = 100 A/µs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	µC

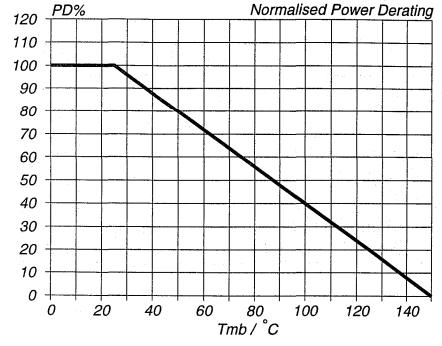


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

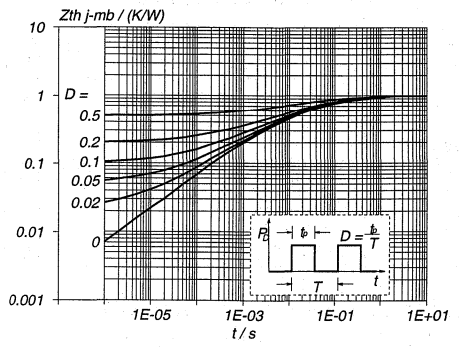


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

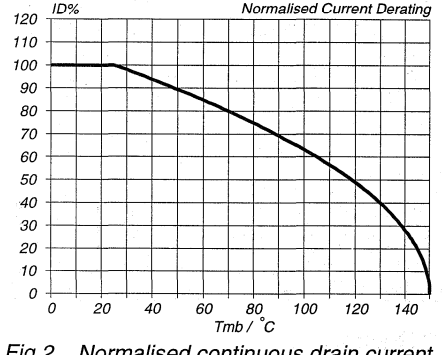


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

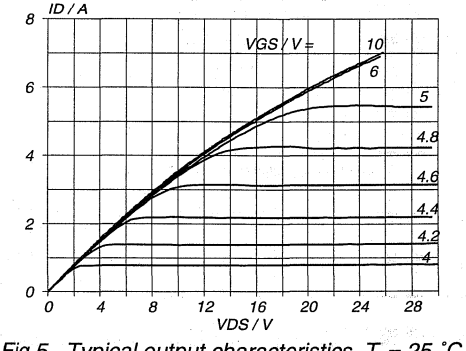


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

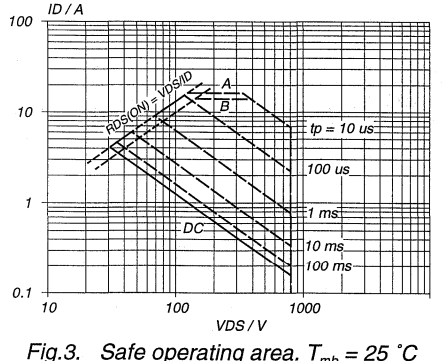


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

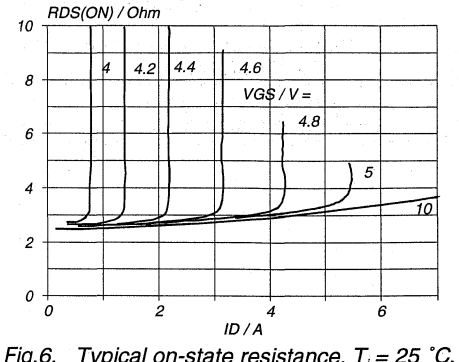


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

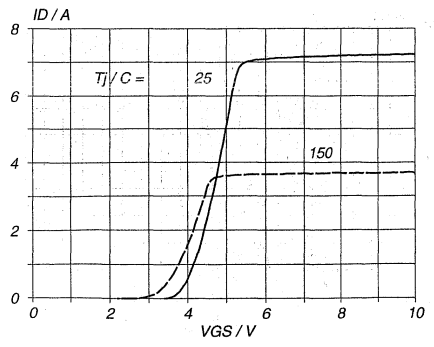


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

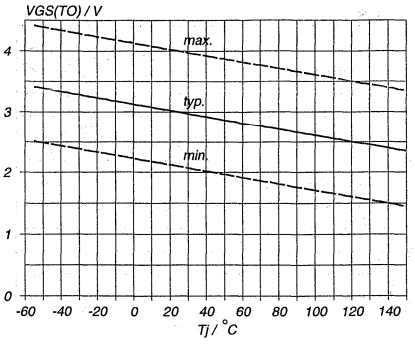


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

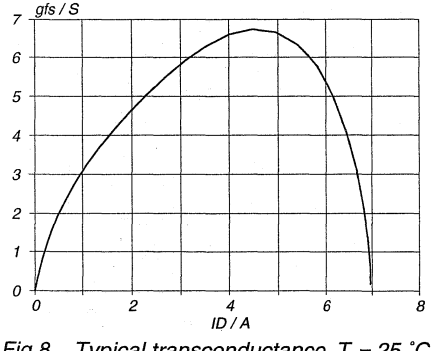


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

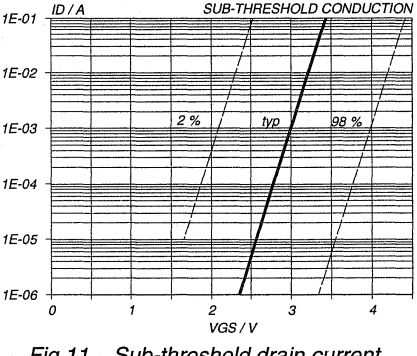


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

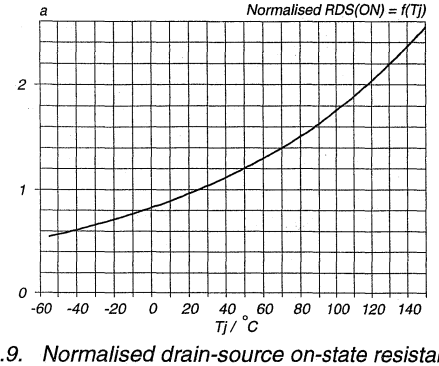


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.5 A; V_{GS} = 10 V

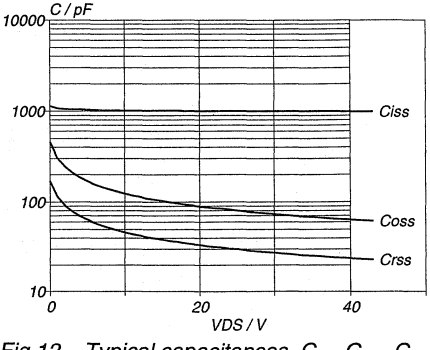


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

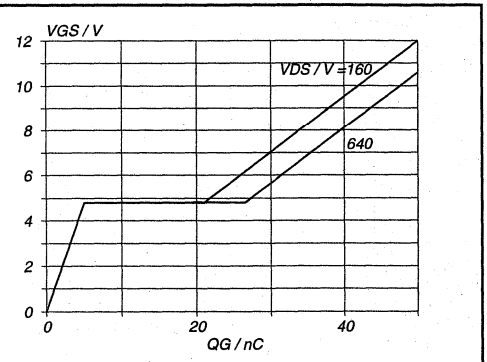


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 4$ A; parameter V_{DS}

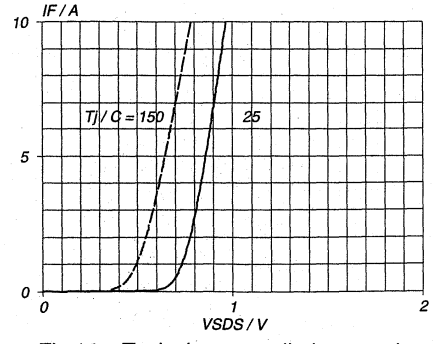


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

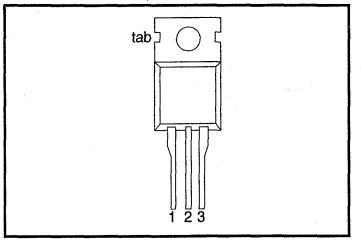
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (DC)	3.1	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	5	Ω

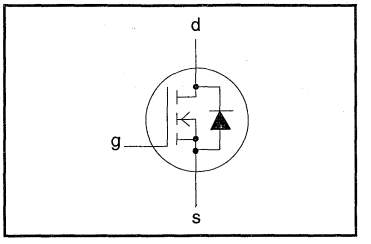
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	1000	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	3.1	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	2.0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	1000	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	-	2	20	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.5 A	-	4.5	5.0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	3.0	4.3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1250	pF
C_{oss}	Output capacitance		-	80	120	pF
C_{rss}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	50	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	130	150	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	3.5	A
I_{DRM}	Pulsed reverse drain current	-	-	-	14	A
V_{SD}	Diode forward voltage	I_F = 3.5 A ; V_{GS} = 0 V	-	1.0	1.3	V
t_{rr}	Reverse recovery time	I_F = 3.5 A; -dI_F/dt = 100 A/μs;	-	1800	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	12	-	μC

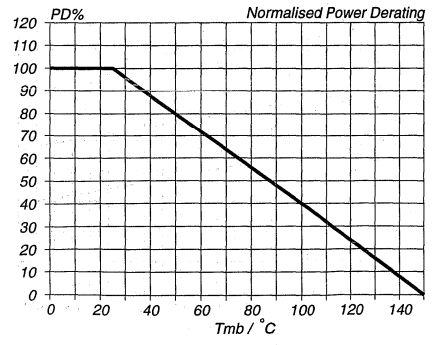


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

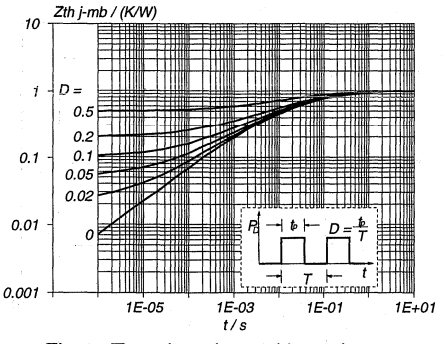


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

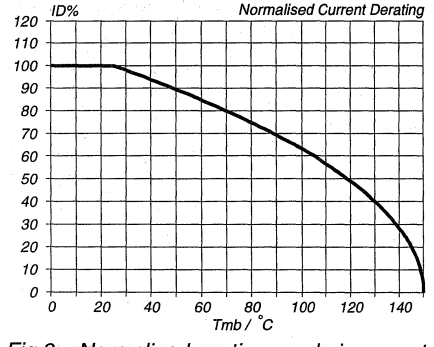


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

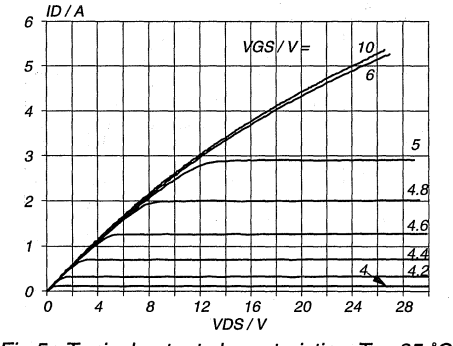


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

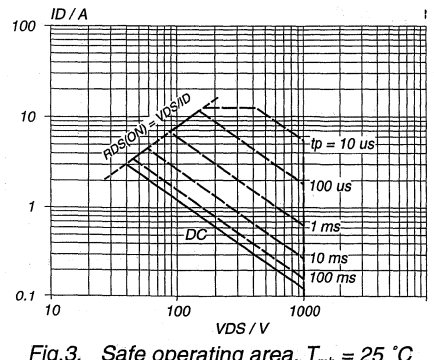


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

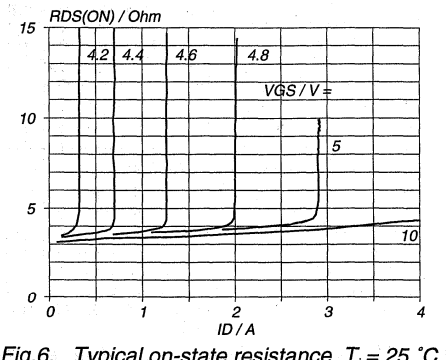


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

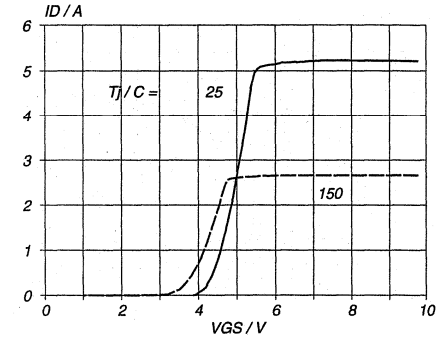


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

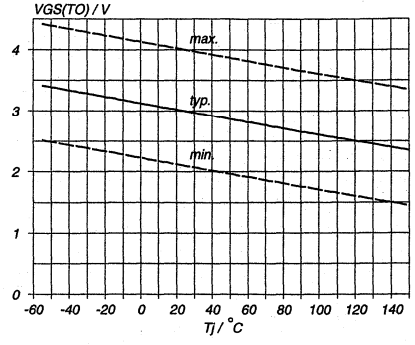


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

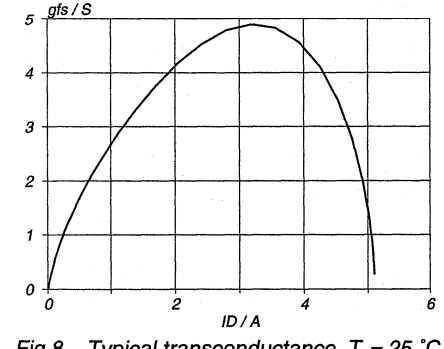


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

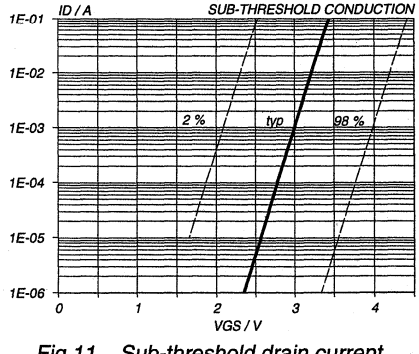


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

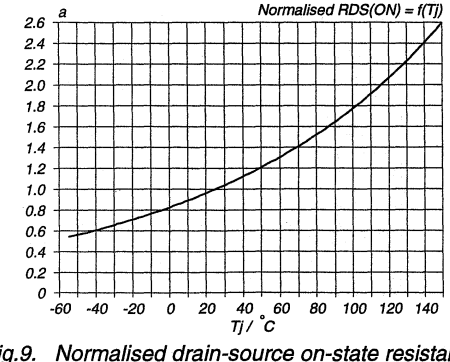


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 1.5$ A; $V_{GS} = 10$ V

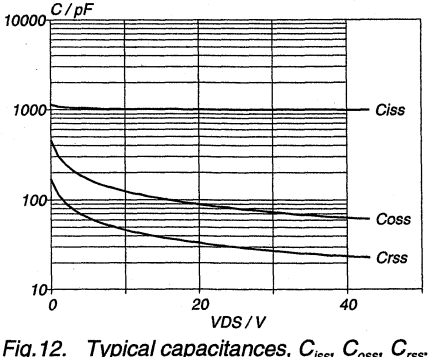


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

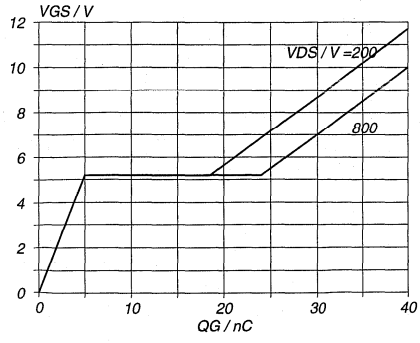


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3.5$ A; parameter V_{DS}

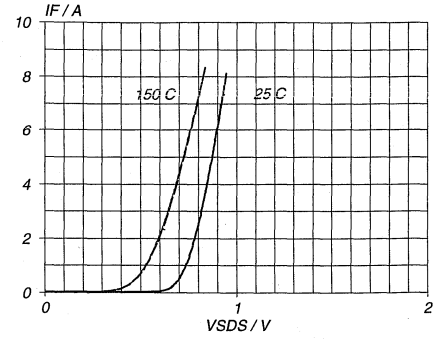


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

mGENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

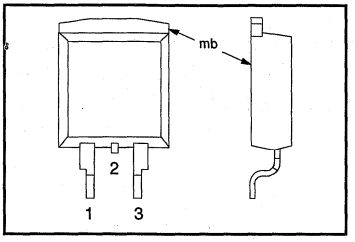
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	15	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.13	Ω

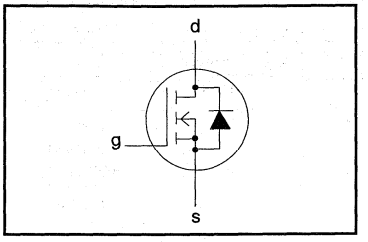
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	15	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	11	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	60	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 8.5 A	-	0.11	0.13	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	3.5	4.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	70	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	8	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	45	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	15	A
I_{DRM}	Pulsed reverse drain current	-	-	-	60	A
V_{SD}	Diode forward voltage	I_F = 15 A ; V_{GS} = 0 V	-	1.4	1.7	V
t_{rr}	Reverse recovery time	I_F = 15 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 15 A ; $V_{DD} \leq$ 30 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	30	mJ

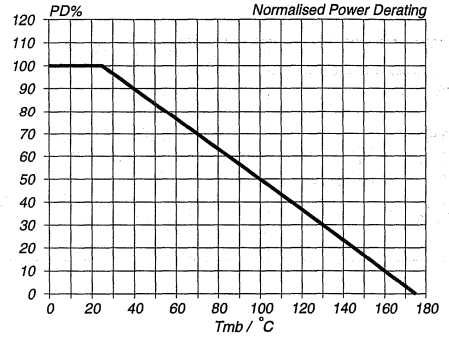


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

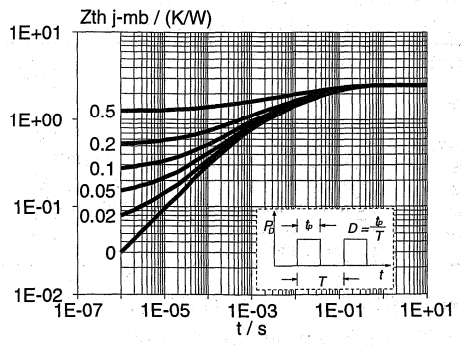


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

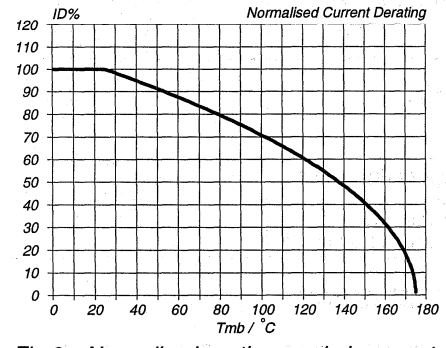


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

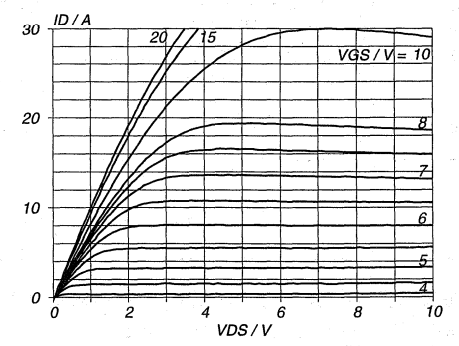


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

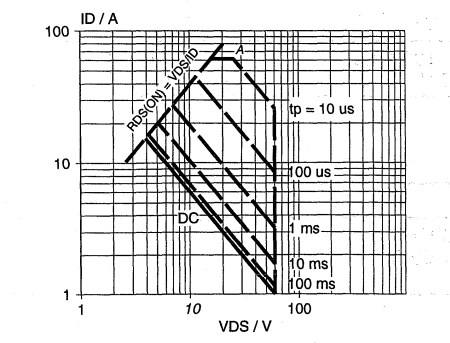


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

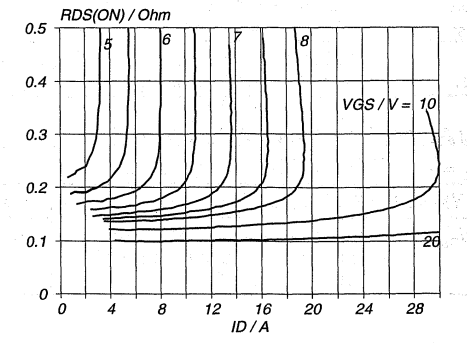


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

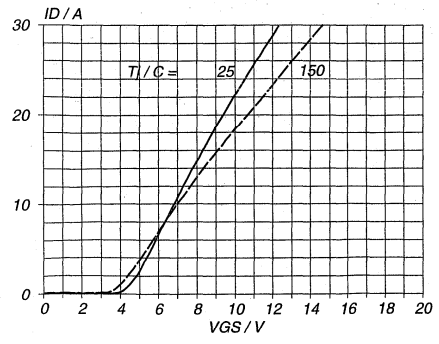


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

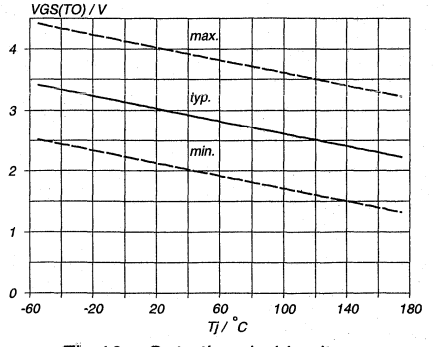


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

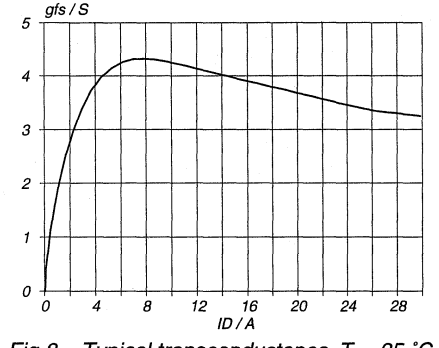


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

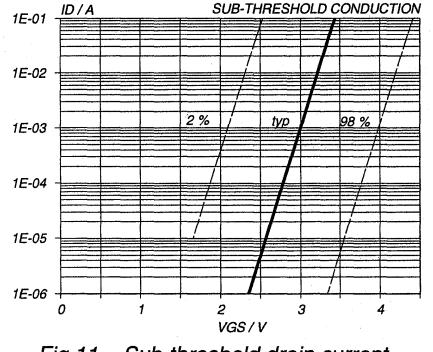


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

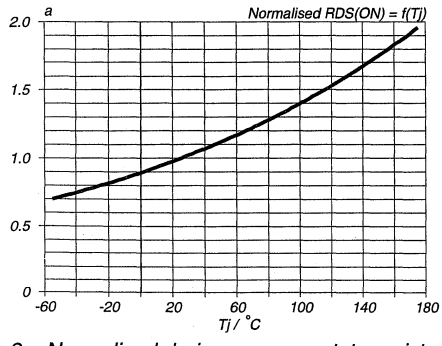


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 8.5 A; V_{GS} = 10 V

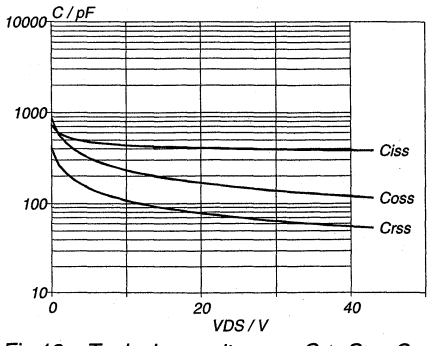


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

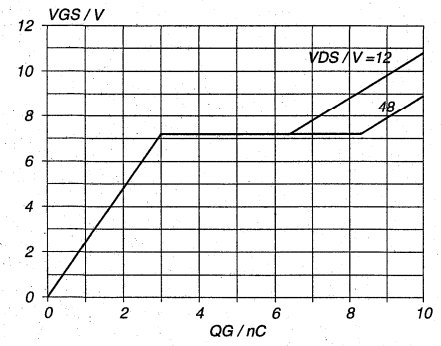


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 15 A; parameter V_{DS}

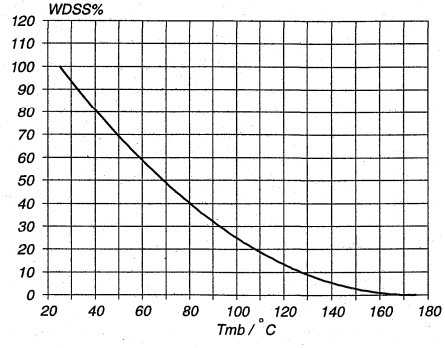


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: I_D = 15 A

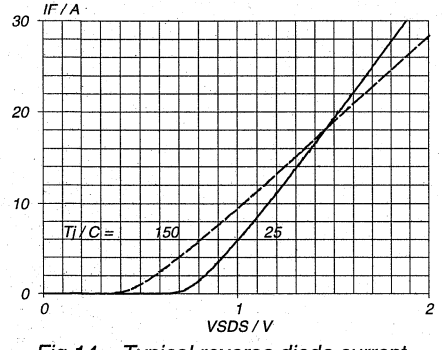


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

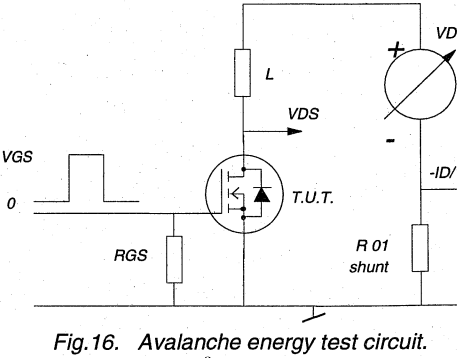


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

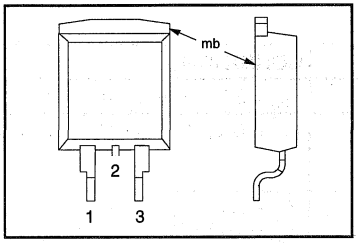
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	11	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	Ω

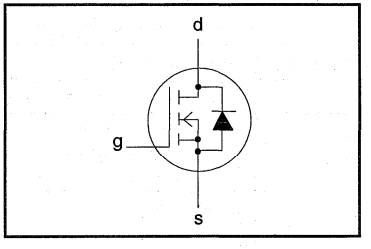
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	44	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint FR4 board (see fig. 18.)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A	-	0.22	0.25	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	11	A
I_{DRM}	Pulsed reverse drain current	-	-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

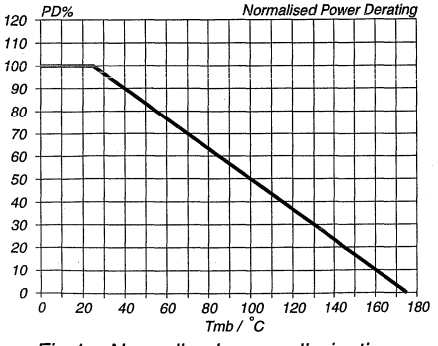


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

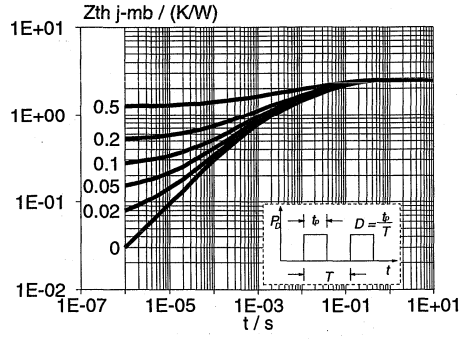


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

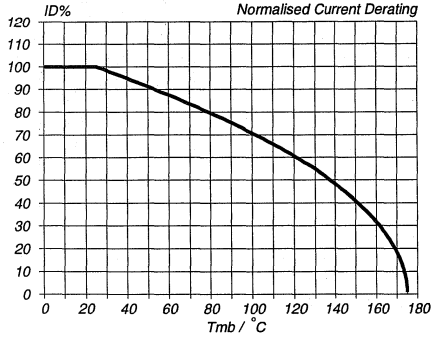


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

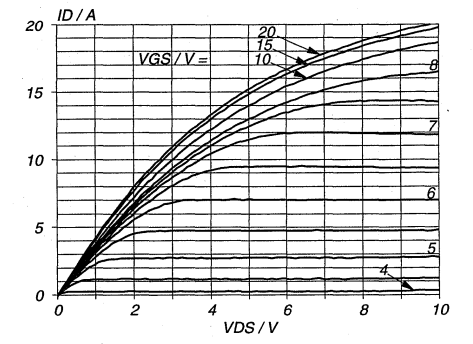


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

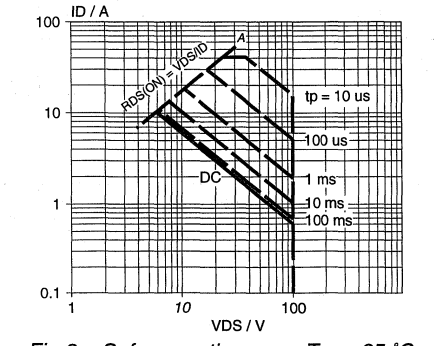


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

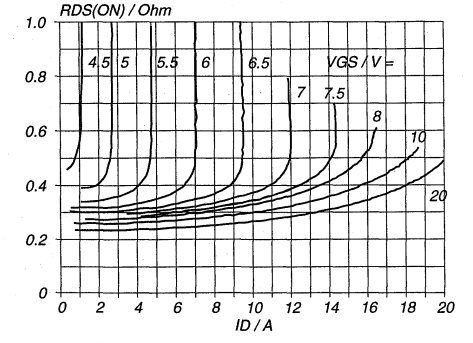


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

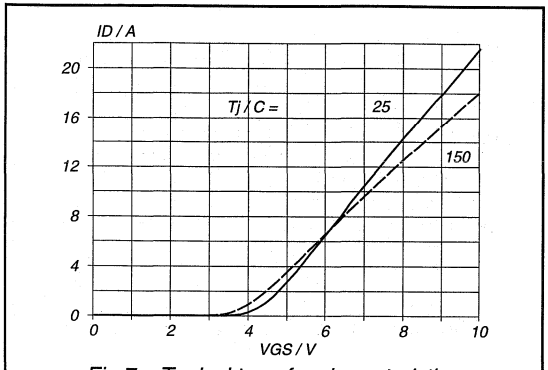


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

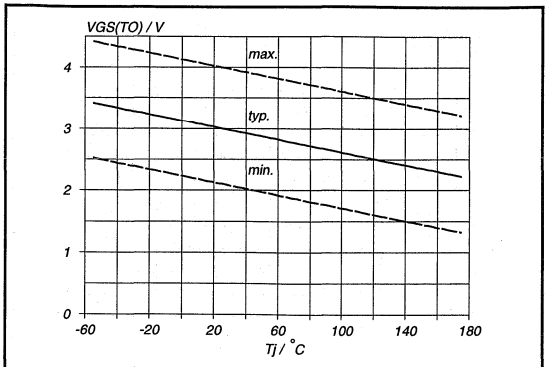


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

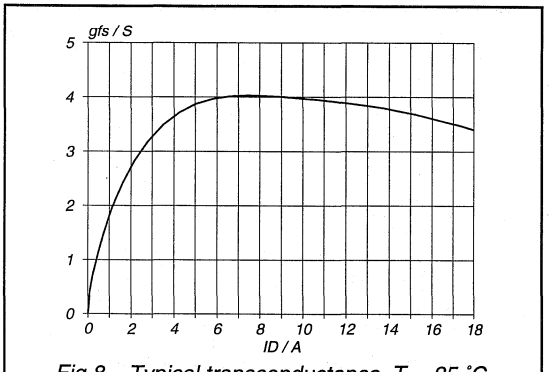


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

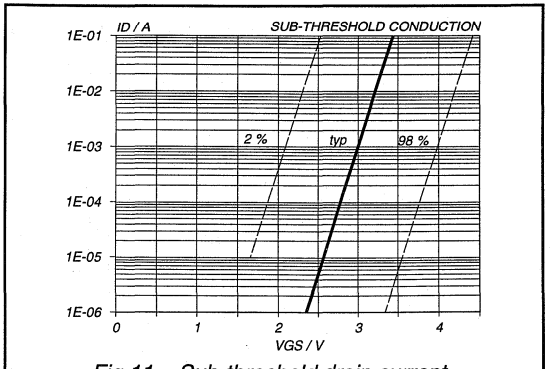


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

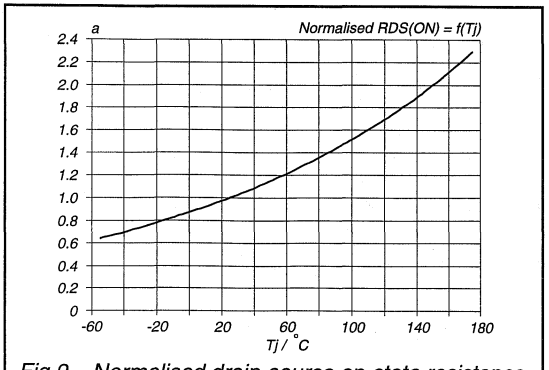


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

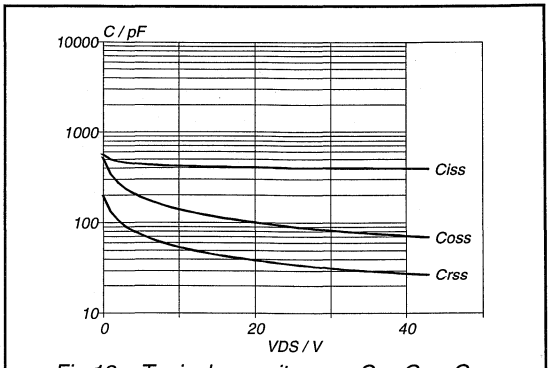


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

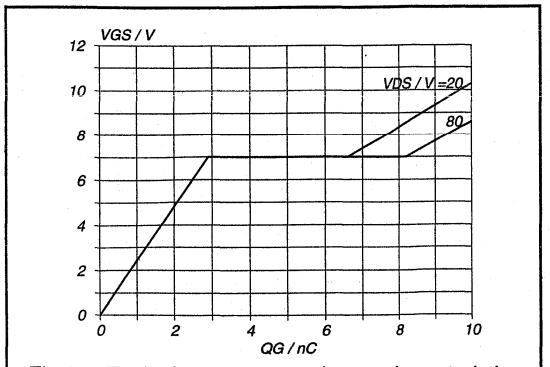


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 11 A; parameter V_{DS}

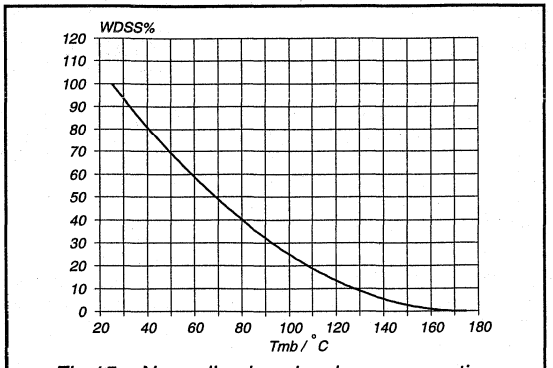


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 11 A

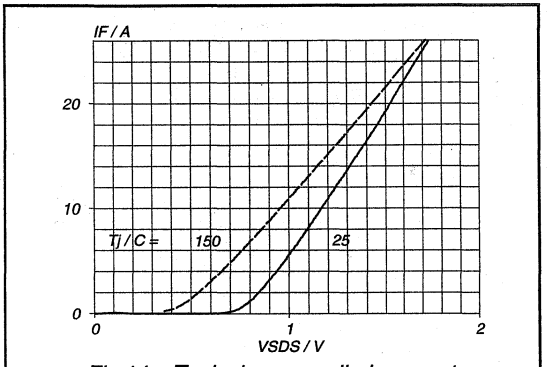


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

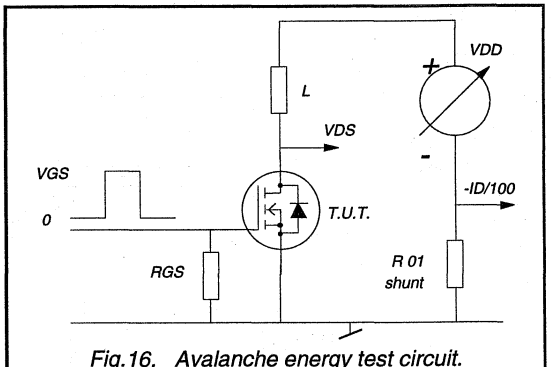


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

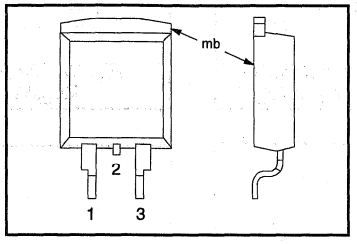
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK463	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	22	20	A
P_{tot}	Total power dissipation	75	75	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	0.10	Ω

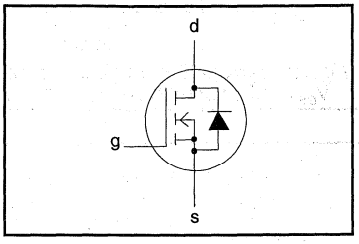
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	22	20	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	15	14	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	88	80	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A **BUK463-60A**	-	0.07	0.08	Ω
		BUK463-60B	-	0.08	0.10	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	4.5	6.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	120	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	55	80	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	22	A
I_{DRM}	Pulsed reverse drain current	-	-	-	88	A
V_{SD}	Diode forward voltage	I_F = 22 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 22 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 22 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

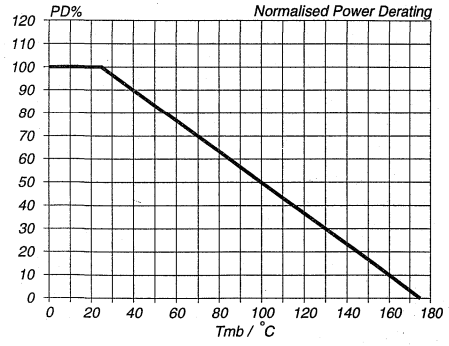


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

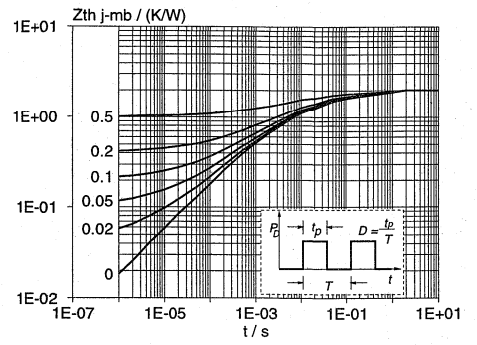


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

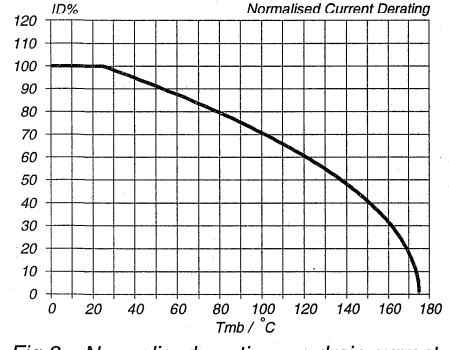


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

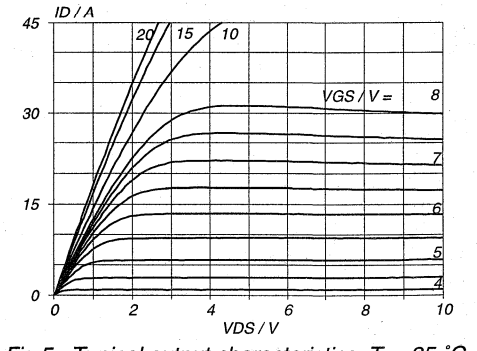


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

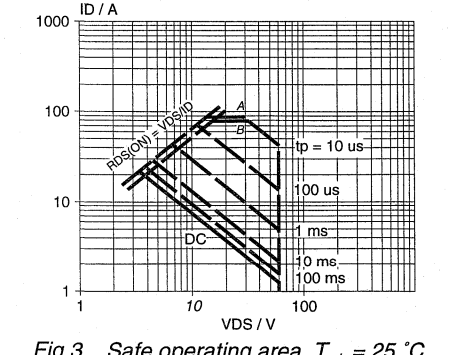


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

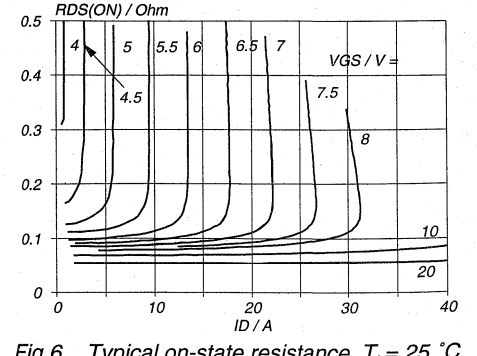


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

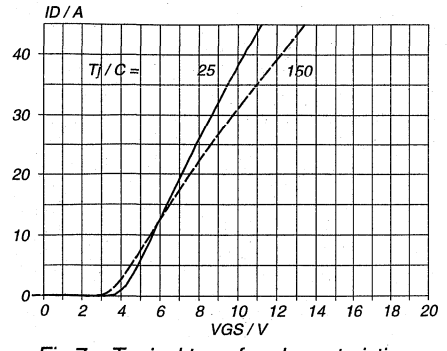


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

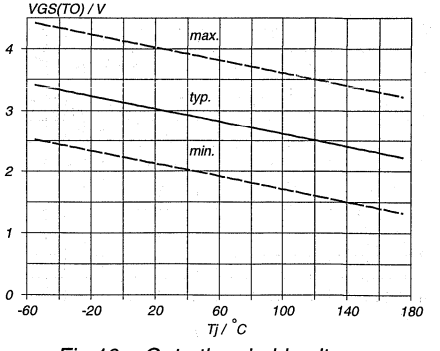


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

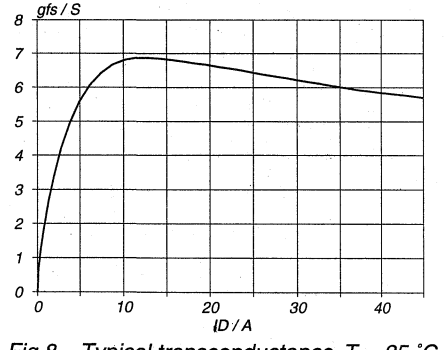


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

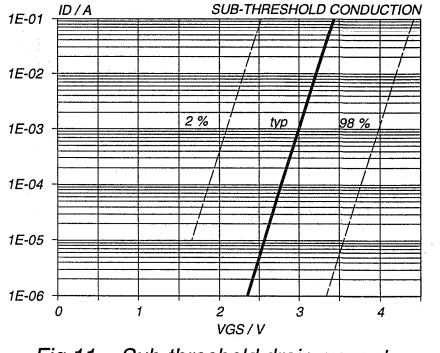


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

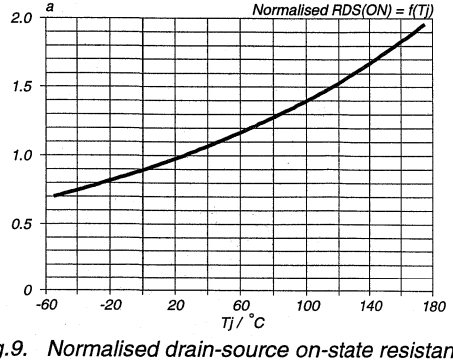


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

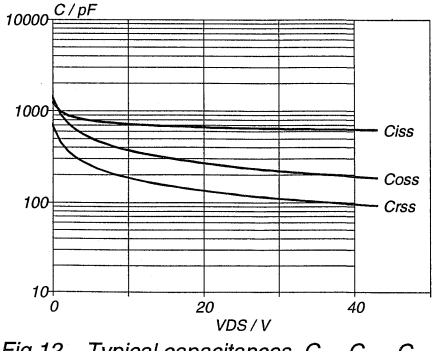


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

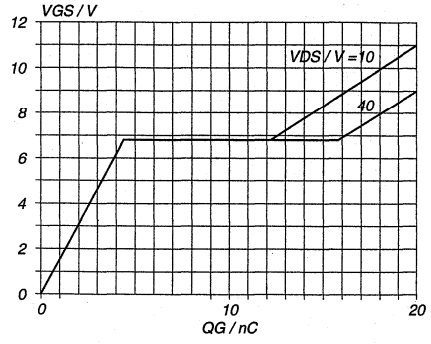


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 22$ A; parameter V_{DS}

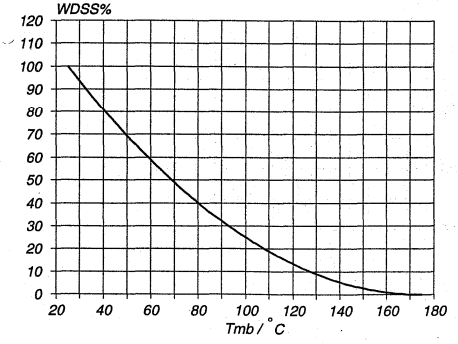


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 22$ A

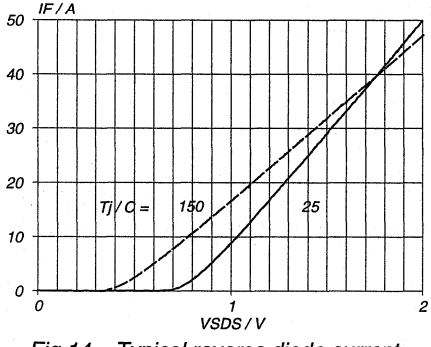


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

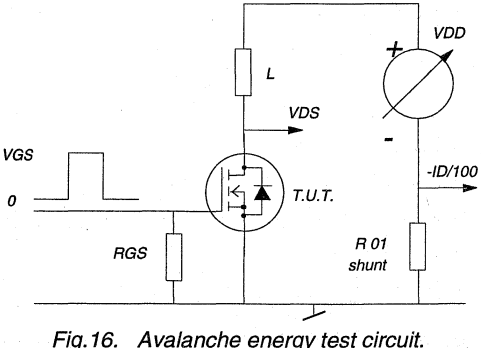


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor — BUK463-100A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

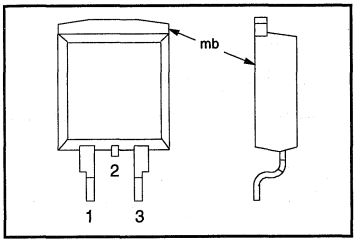
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	Ω

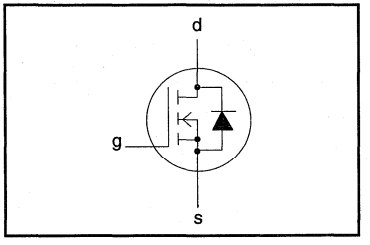
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint FR4 board (see fig. 18)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	70	mJ

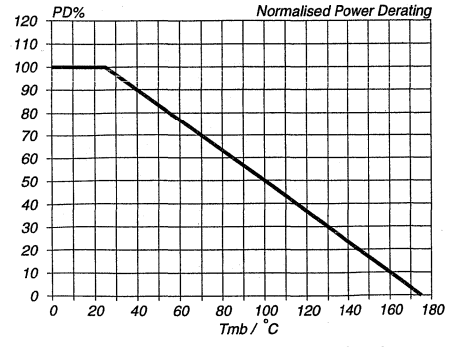


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

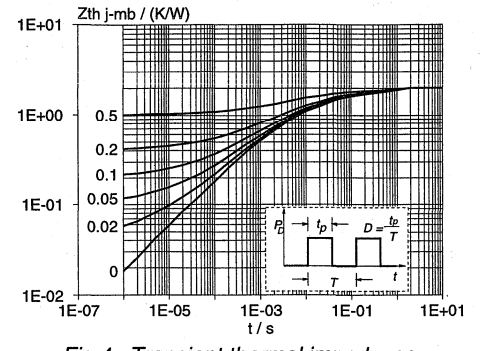


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

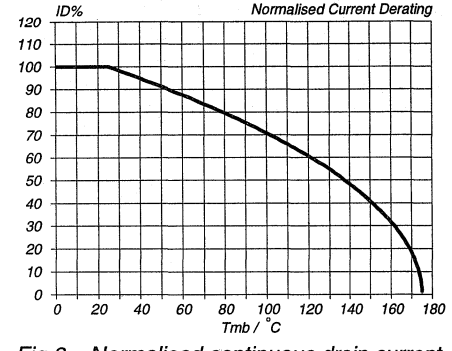


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

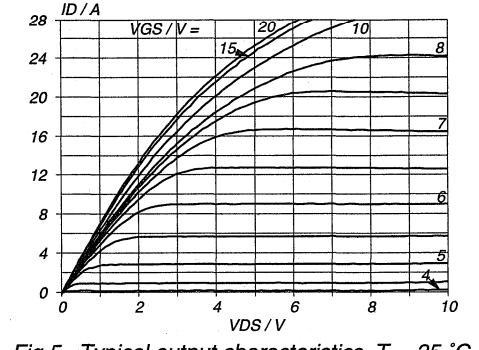


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

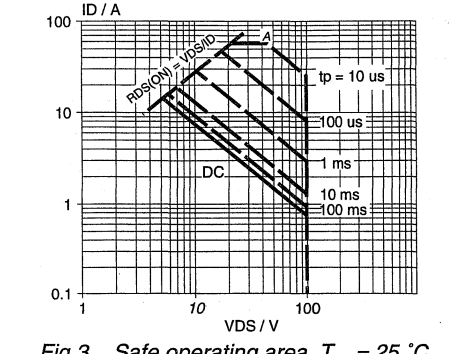


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

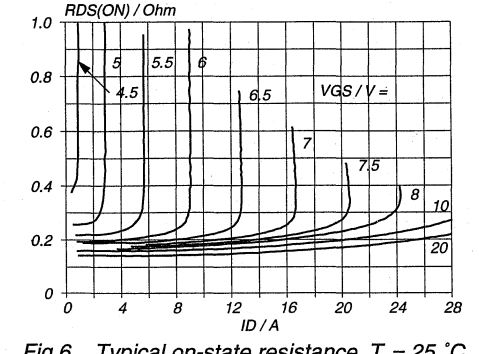


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

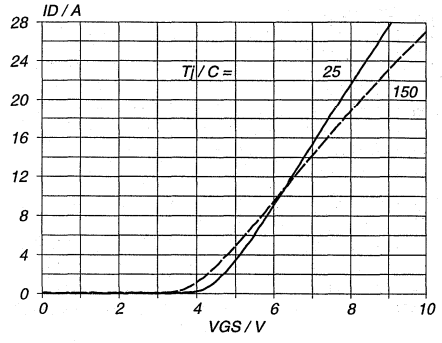


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

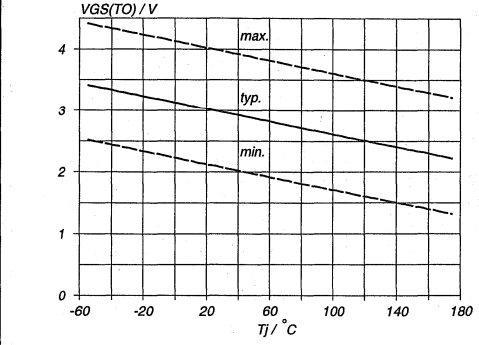


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

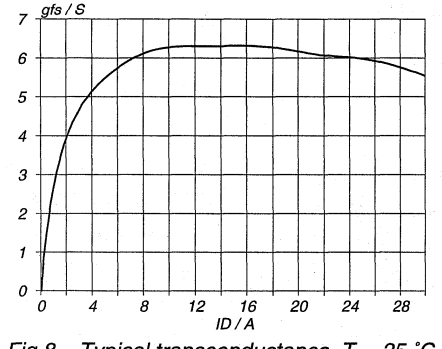


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

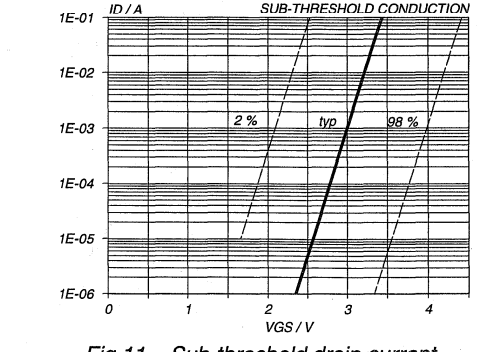


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

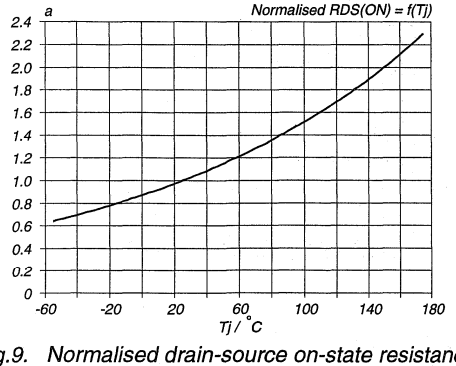


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

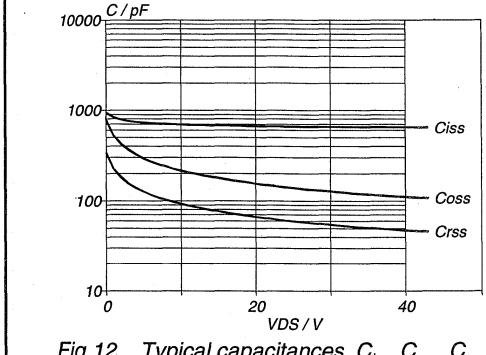


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

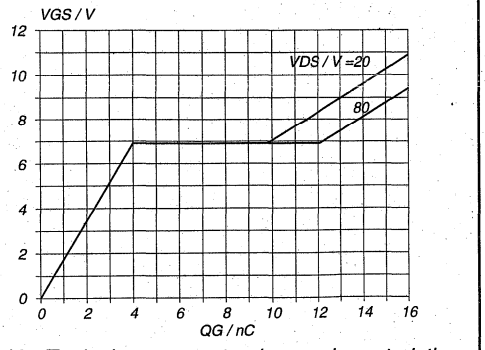


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

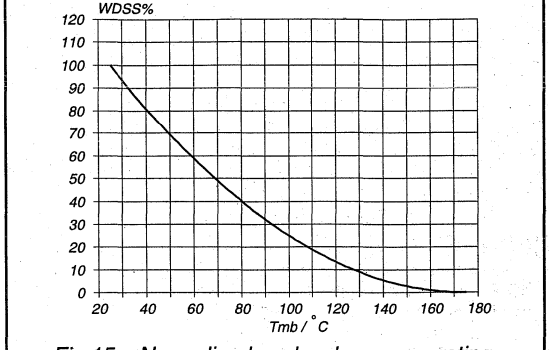


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

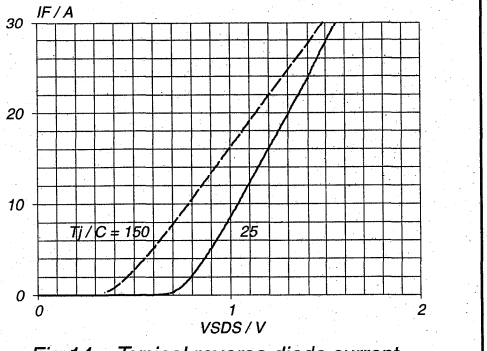


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

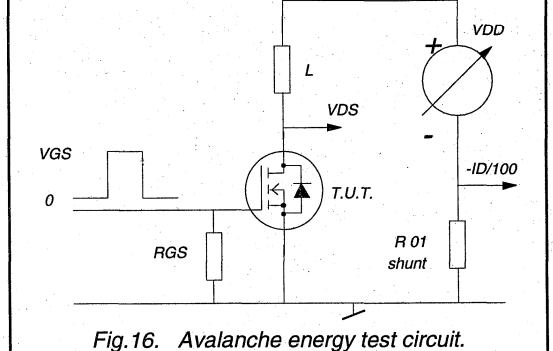


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor | BUK464-60H

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

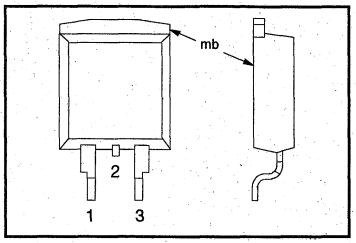
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	41	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	38	mΩ

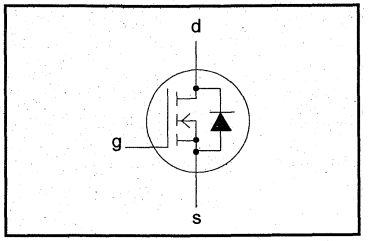
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	30	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	7	14	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	900	1600	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	55	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	75	125	ns
t_f	Turn-off fall time		-	60	100	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

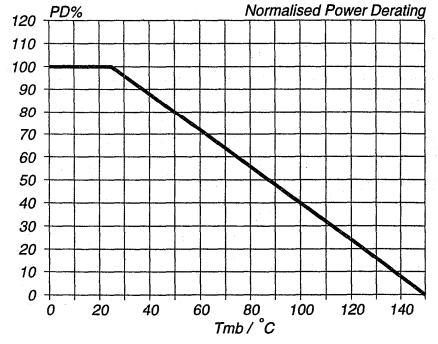


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

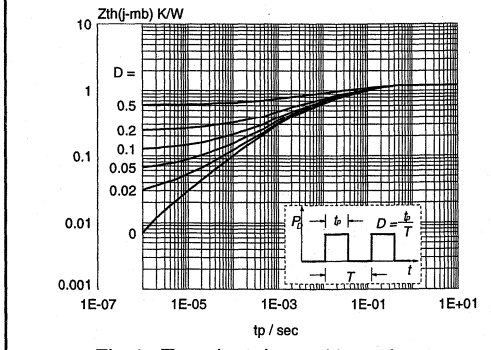


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

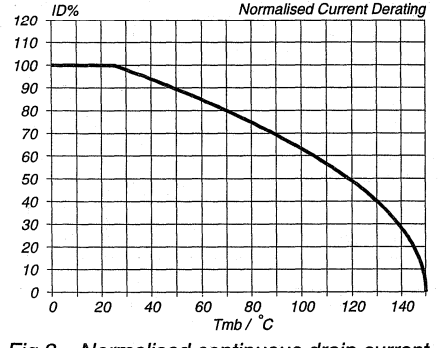


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

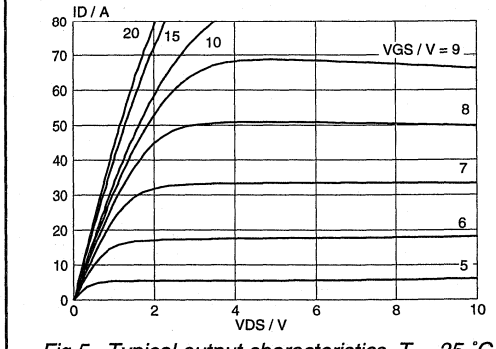


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

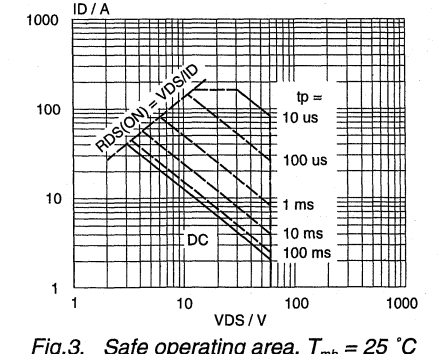


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

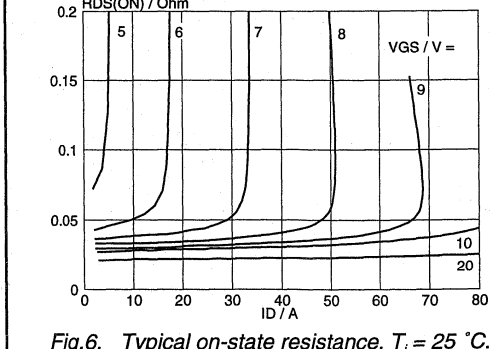


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

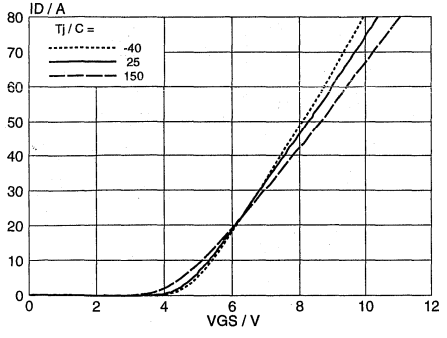


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 15 V; parameter T_j

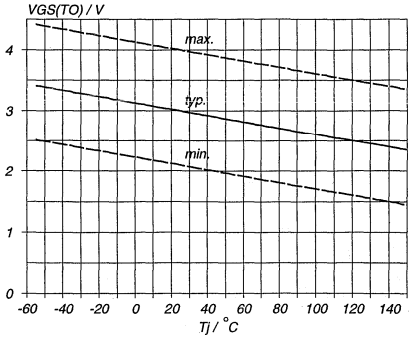


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

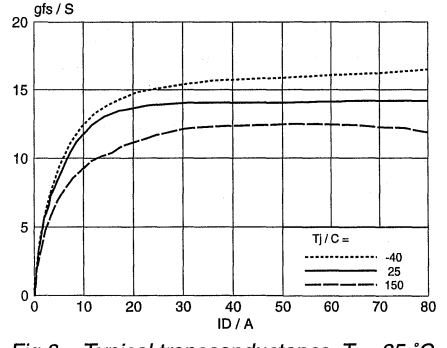


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

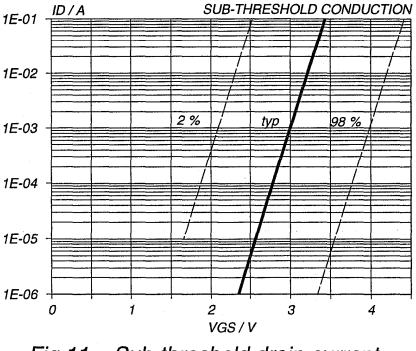


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

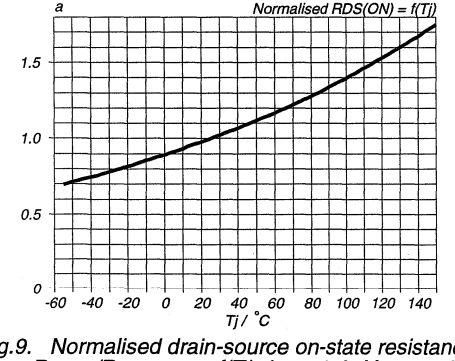


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

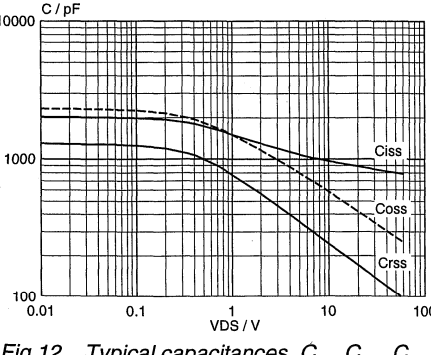


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

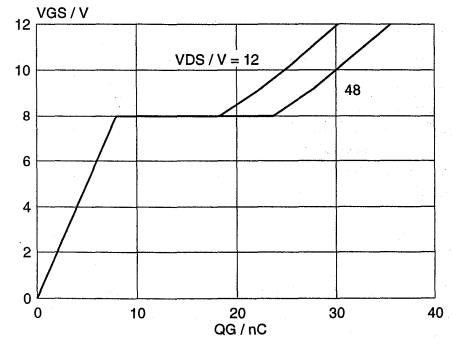


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

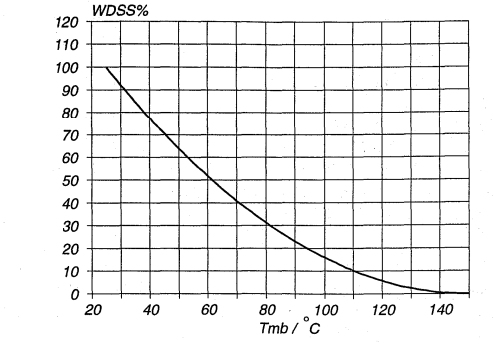


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

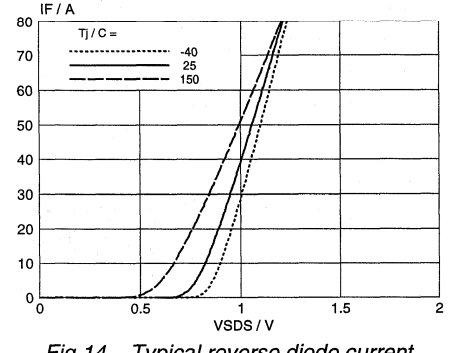


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

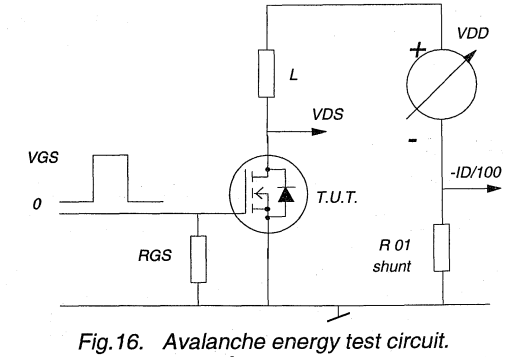


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor BUK464-200A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

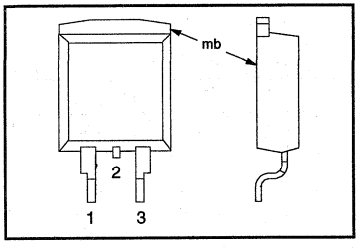
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	Ω

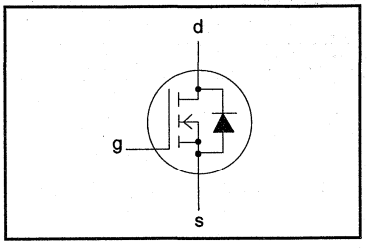
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.5 A	-	0.35	0.4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.2	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; V_{DD} ≤ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

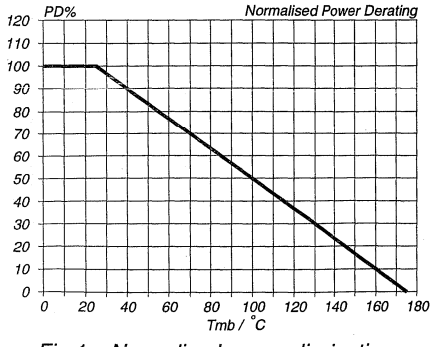


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

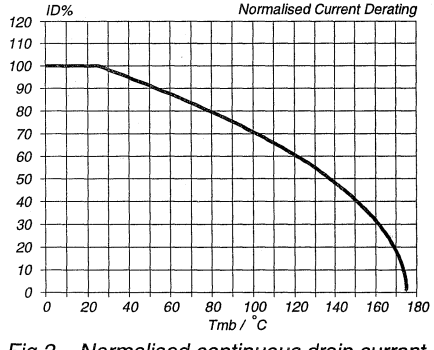


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

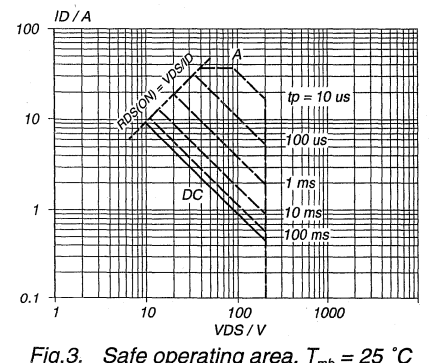


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

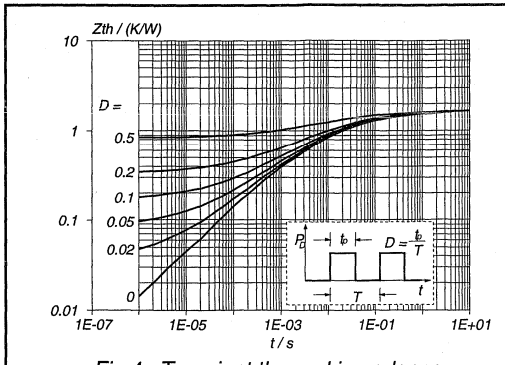


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

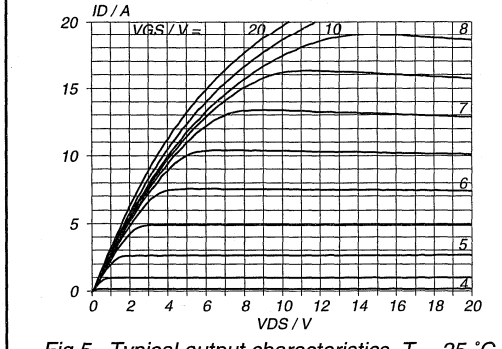


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

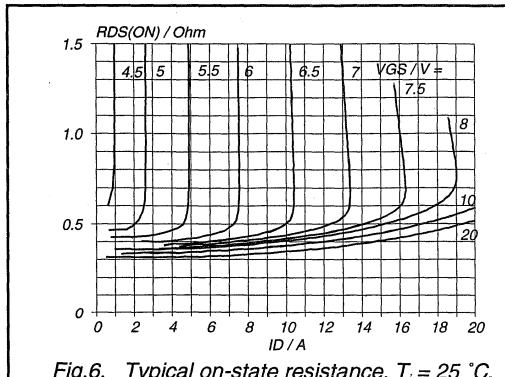


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

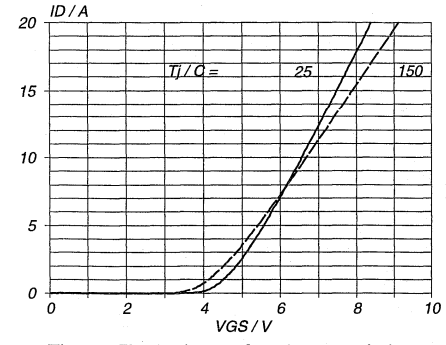


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

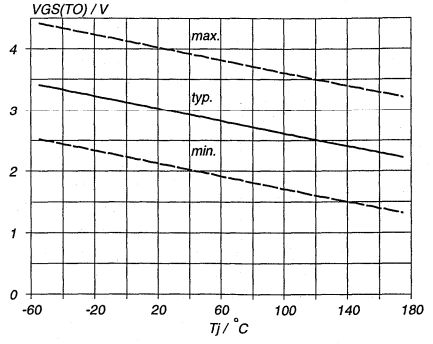


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

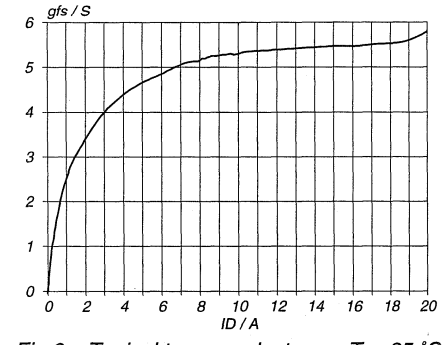


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

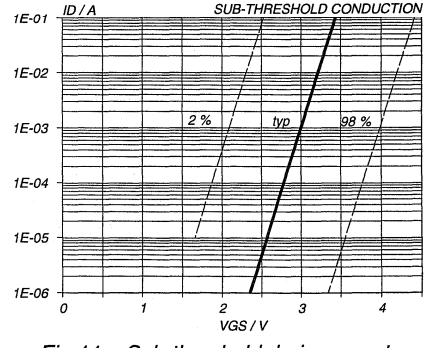


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

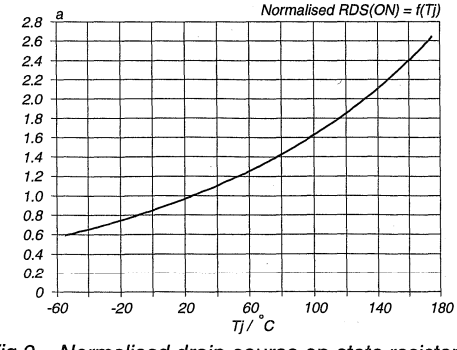


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

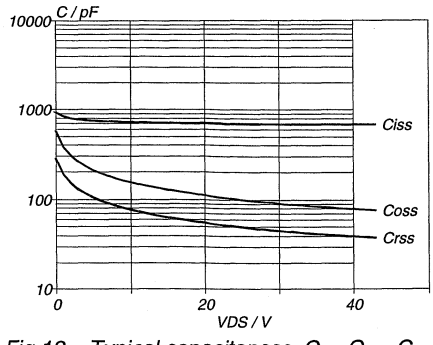


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

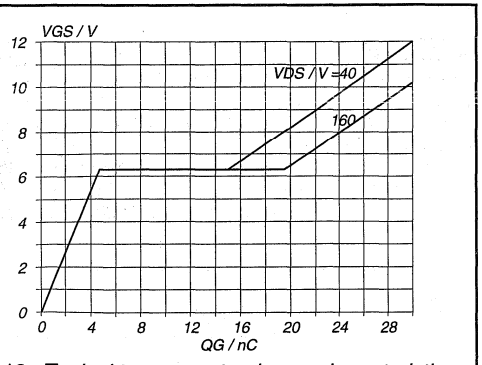


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9.2$ A; parameter V_{DS}

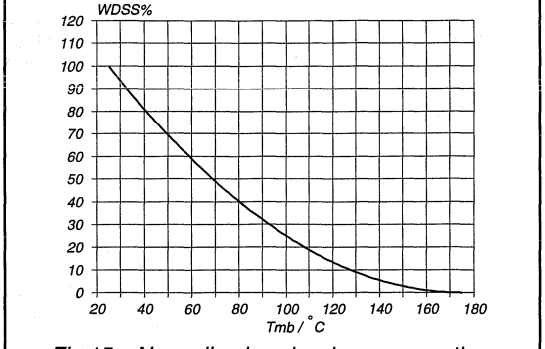


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

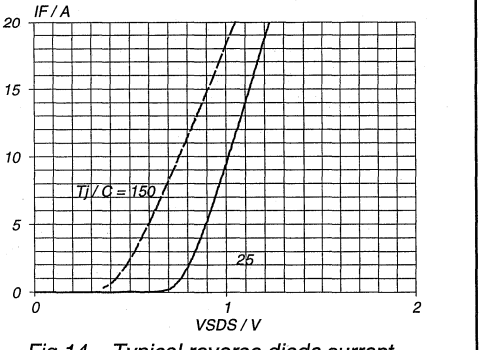


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

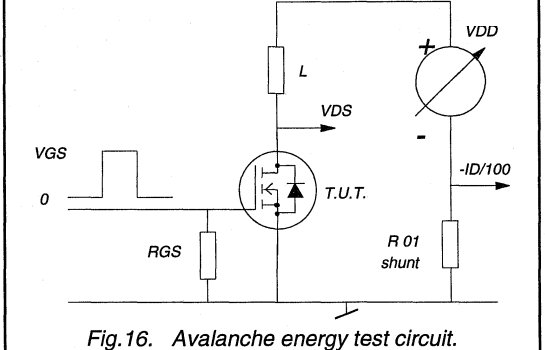


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

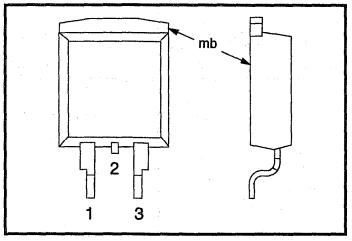
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	**-60A**	
I_D	Drain current (DC)	60	V
P_{tot}	Total power dissipation	41	A
T_j	Junction temperature	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	175	°C
		0.038	Ω

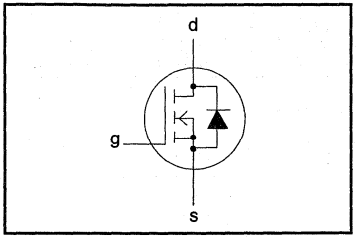
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 boards (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	0.03	0.038	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	8	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	560	750	pF
C_{rss}	Feedback capacitance		-	300	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	125	160	ns
t_f	Turn-off fall time		-	100	130	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	1.4	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

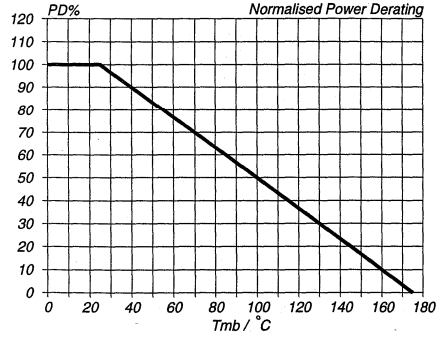


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

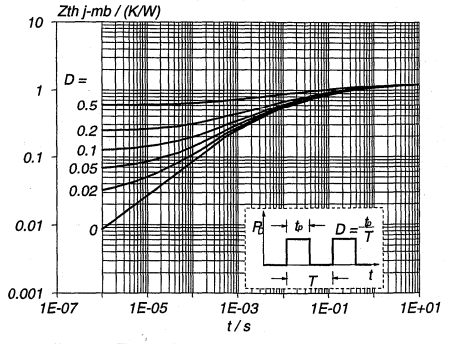


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

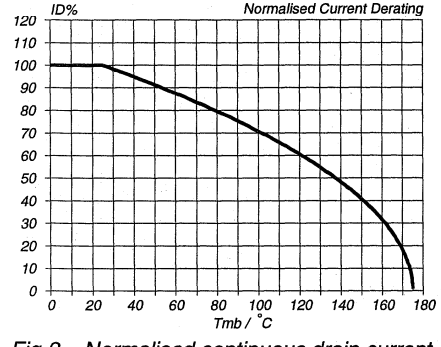


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

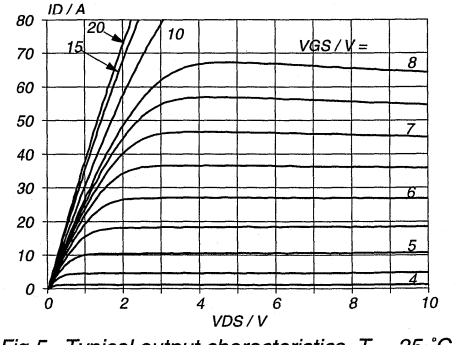


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

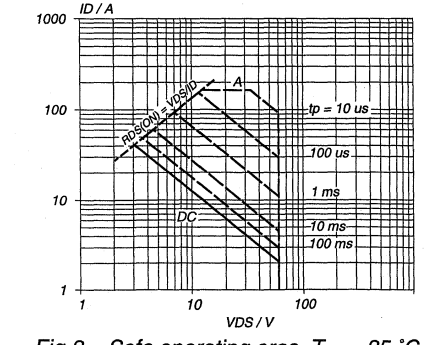


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

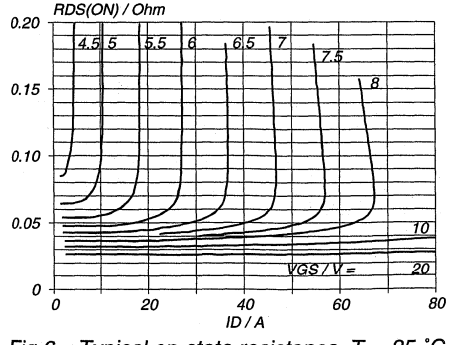


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

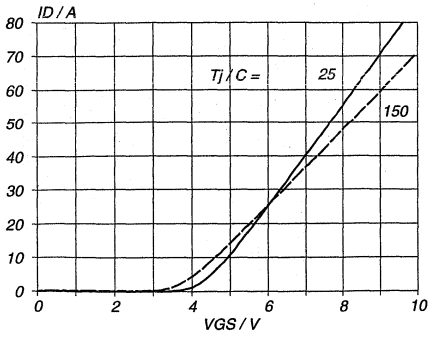


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

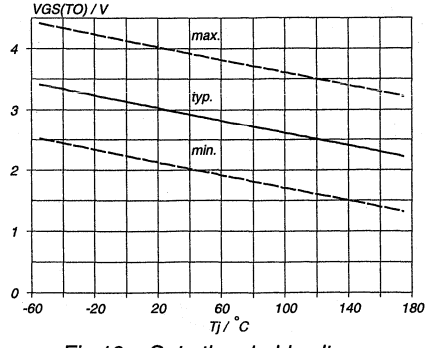


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

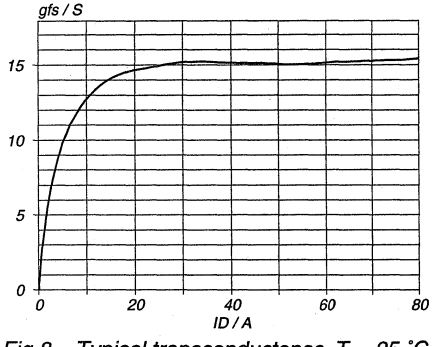


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

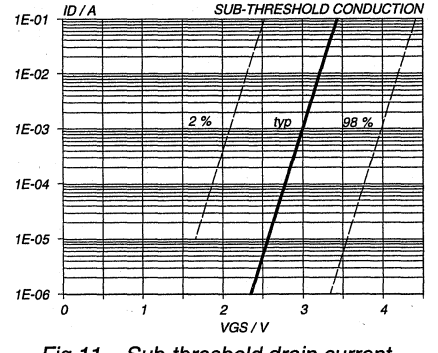


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

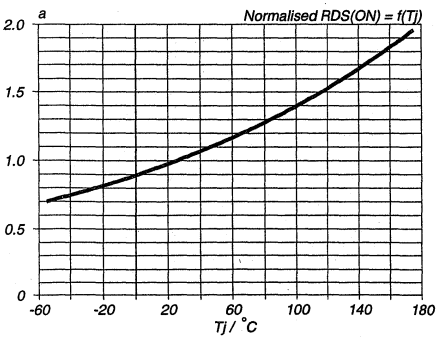


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

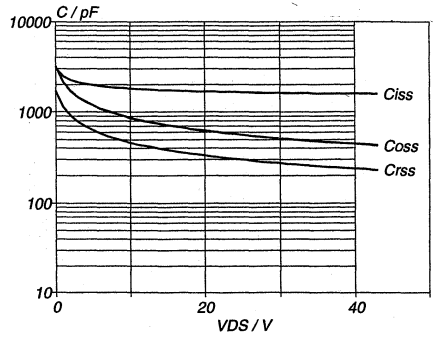


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

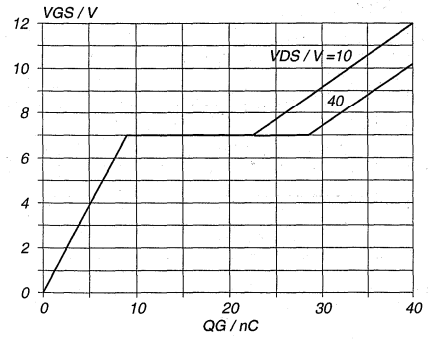


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

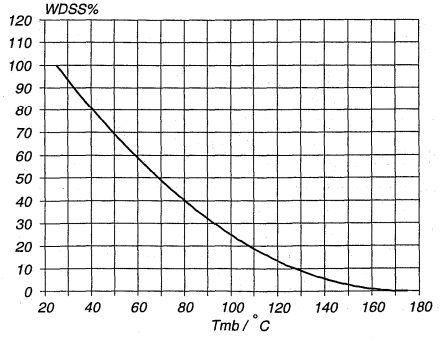


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

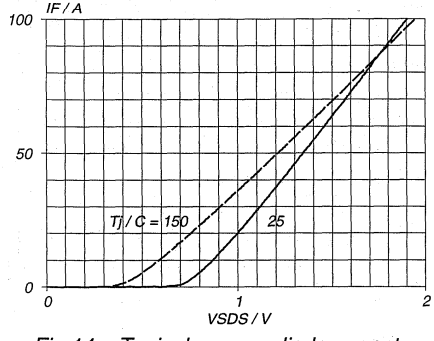


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

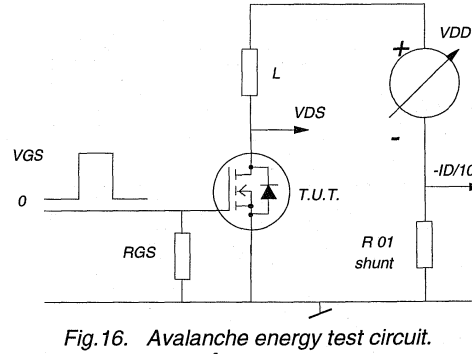


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

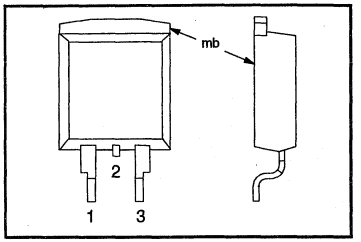
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	30	mΩ

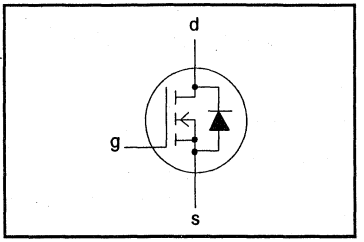
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	32	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	172	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	24	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	8	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1600	pF
C_{oss}	Output capacitance		-	470	600	pF
C_{rss}	Feedback capacitance		-	180	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	125	160	ns
t_f	Turn-off fall time		-	100	130	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	45	A
I_{DRM}	Pulsed reverse drain current	-	-	-	172	A
V_{SD}	Diode forward voltage	I_F = 43 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 43 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 43 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

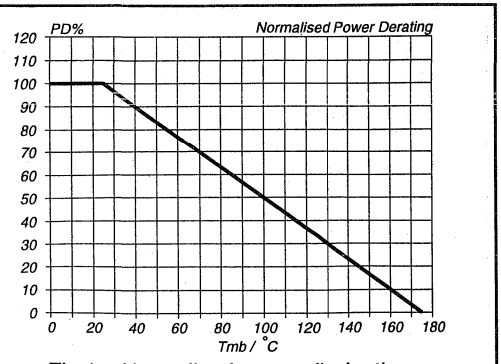


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

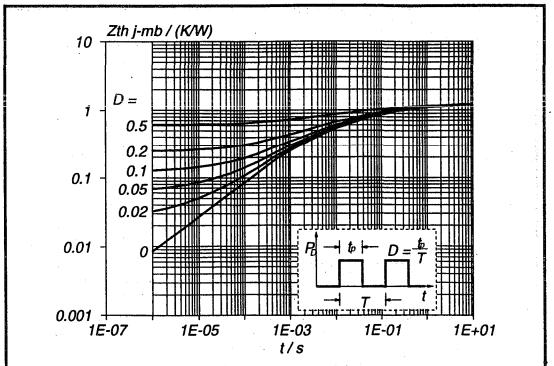


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

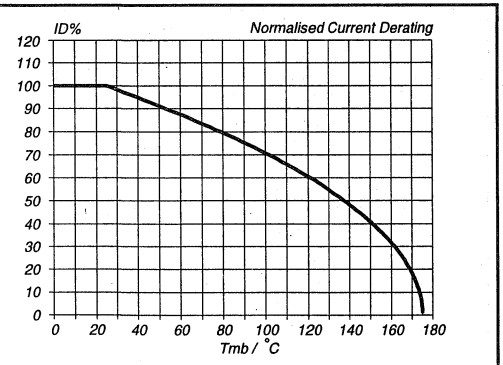


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; *conditions:* $V_{GS} \geq 5$ *V*

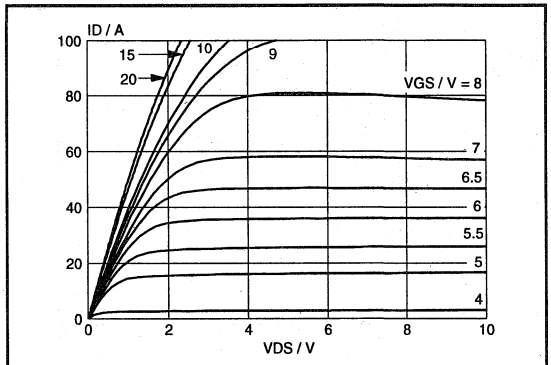


Fig.5. Typical output characteristics, $T_j = 25$ *°C.*
$I_D = f(V_{DS})$; *parameter* V_{GS}

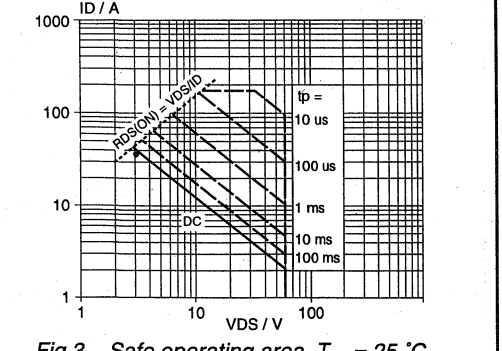


Fig.3. Safe operating area. $T_{mb} = 25$ *°C*
I_D & $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

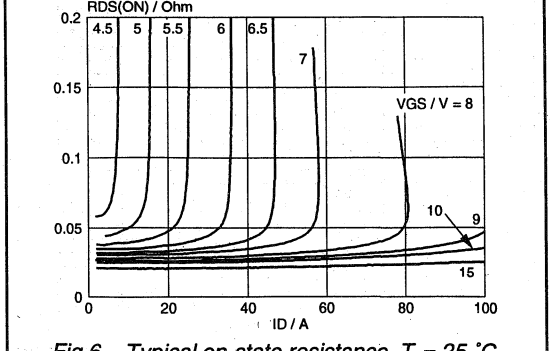


Fig.6. Typical on-state resistance, $T_j = 25$ *°C.*
$R_{DS(ON)} = f(I_D)$; *parameter* V_{GS}

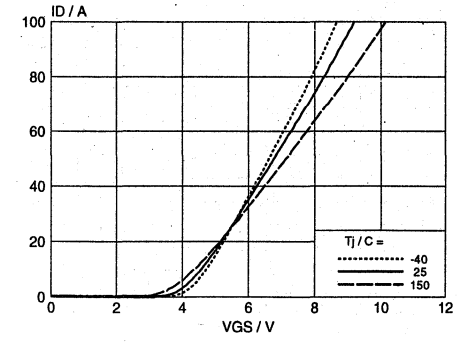


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

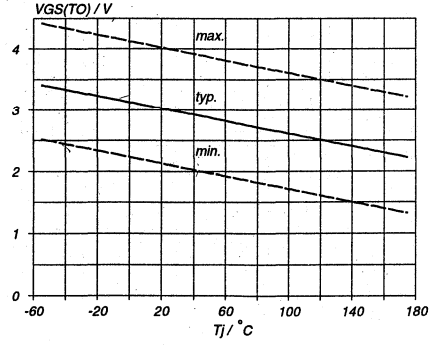


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

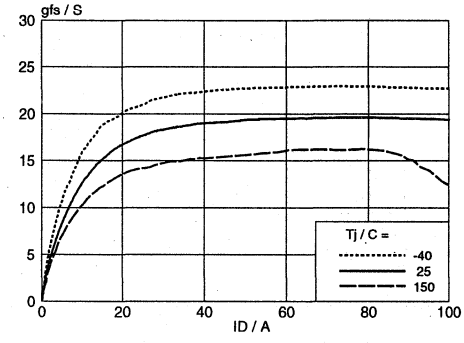


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V

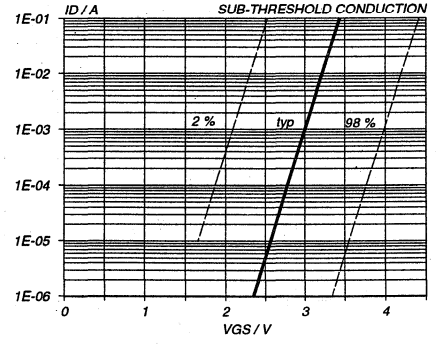


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

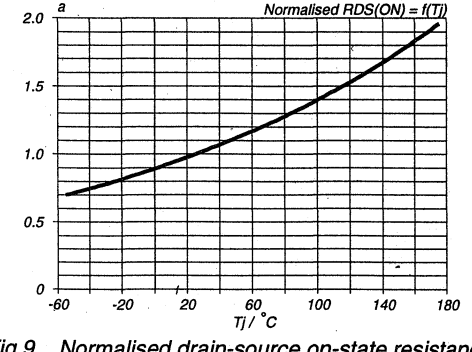


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

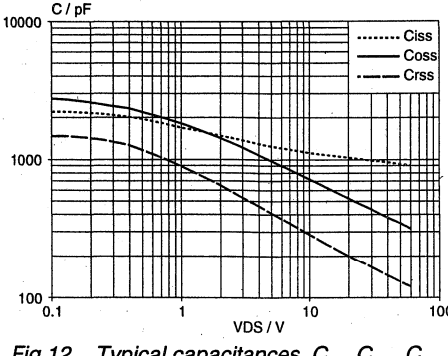


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

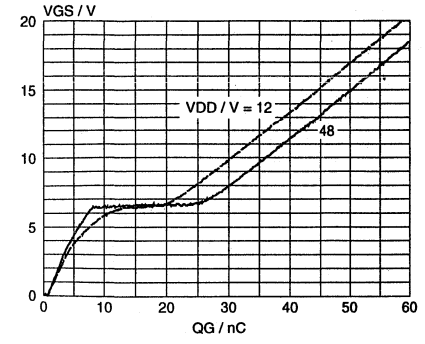


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 43$ A; parameter V_{DS}

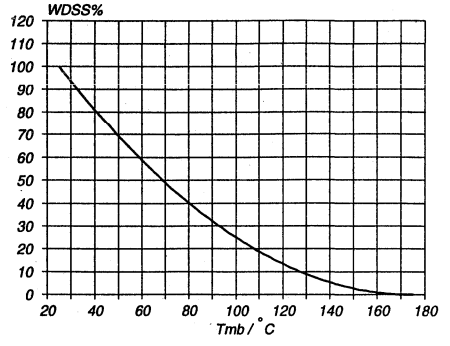


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 43$ A

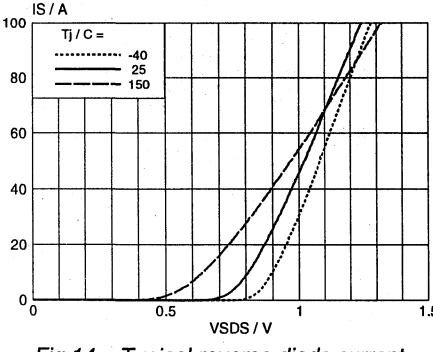


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

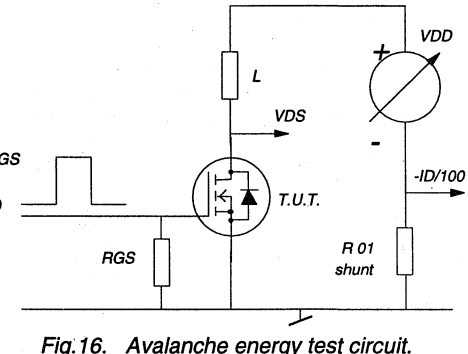


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

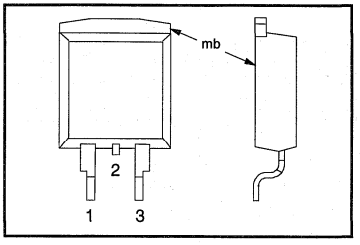
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	26	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	Ω

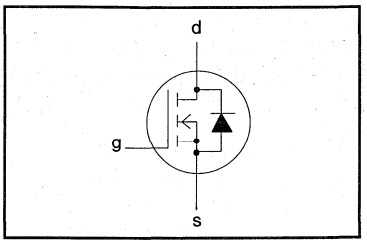
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	26	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	104	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint FR4 board (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 13 A	-	0.07	0.08	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	7.0	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	350	500	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	100	160	ns
t_f	Turn-off fall time		-	50	80	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	26	A
I_{DRM}	Pulsed reverse drain current	-	-	-	104	A
V_{SD}	Diode forward voltage	I_F = 26 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 26 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 26 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

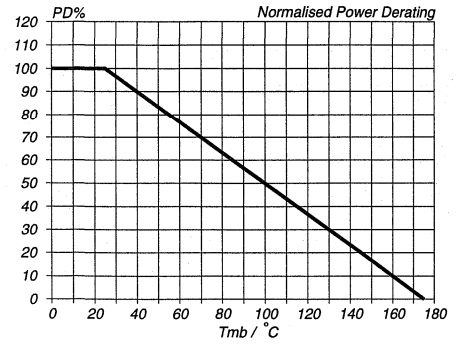


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

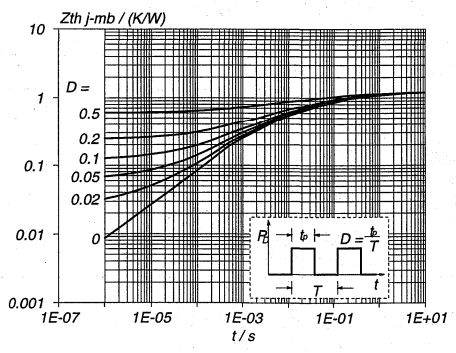


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

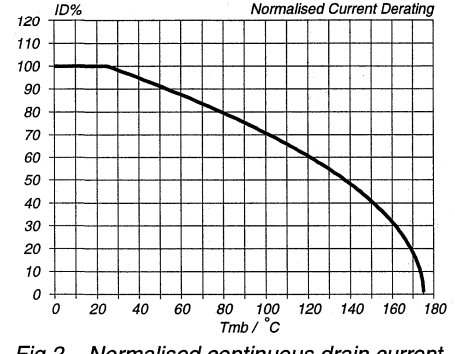


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

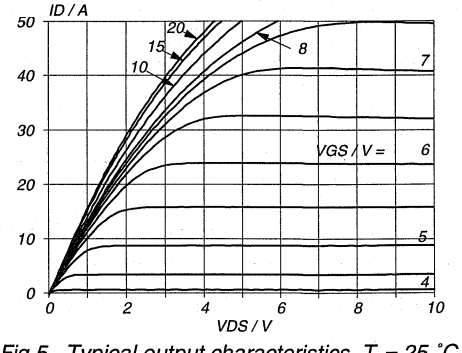


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

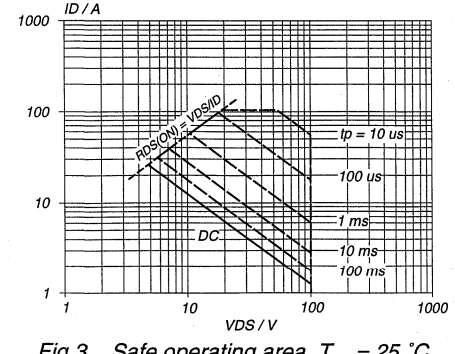


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

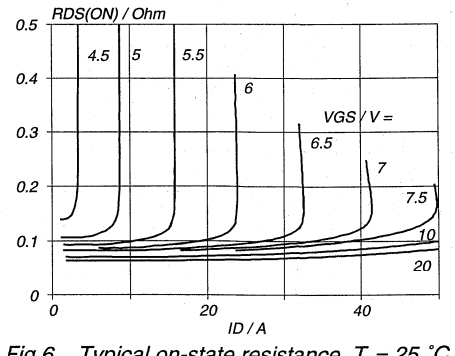


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

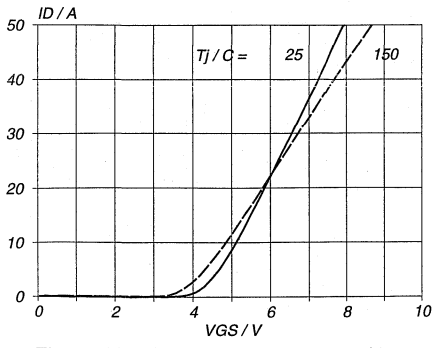


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

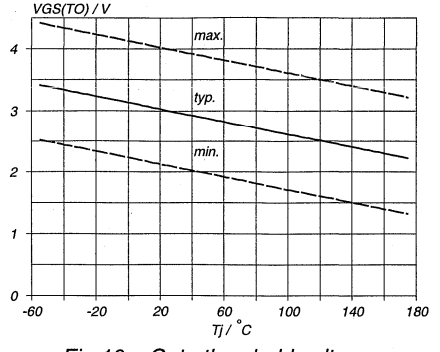


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

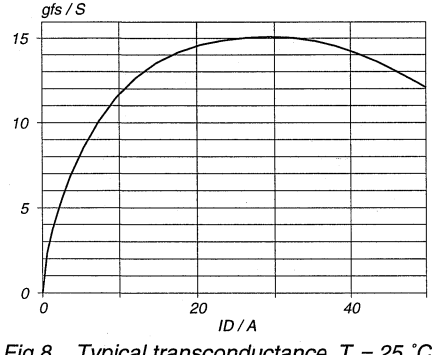


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

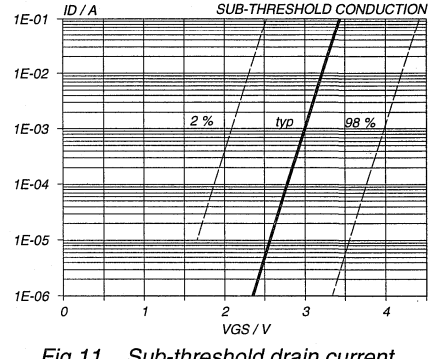


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

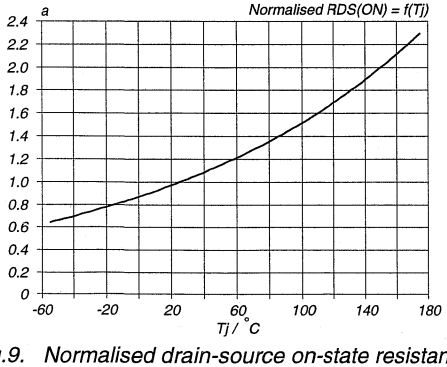


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 13$ A; $V_{GS} = 10$ V

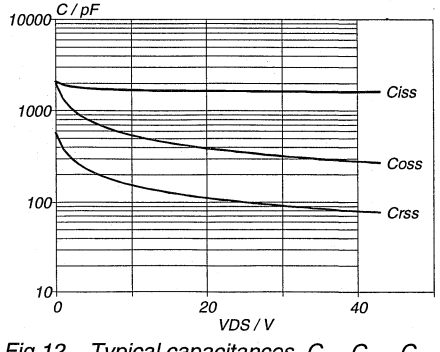


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

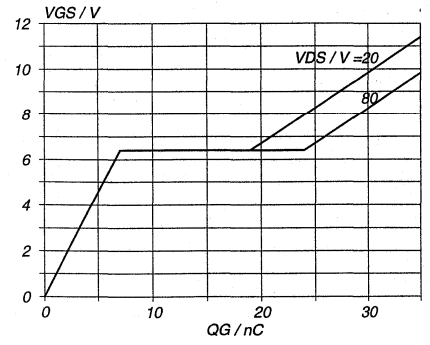


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 26$ A; parameter V_{DS}

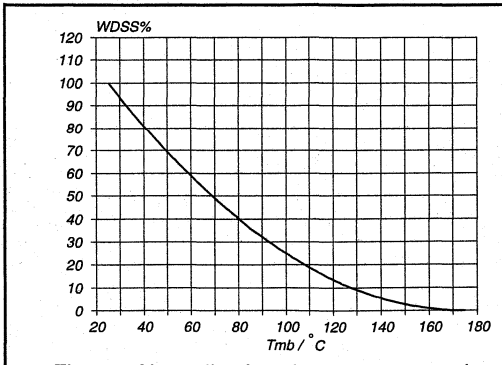


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 26$ A

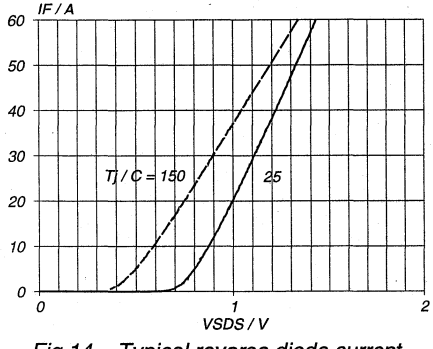


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

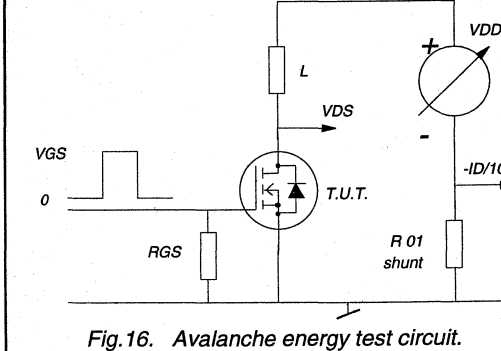


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor BUK465-200A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

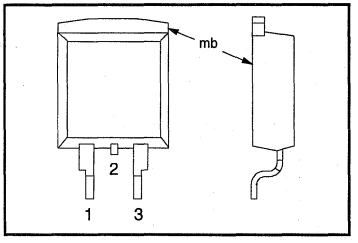
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.23	Ω

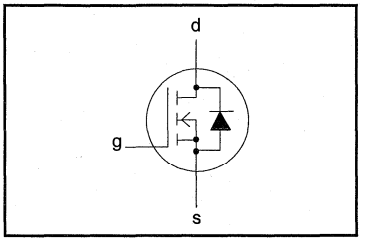
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18.)	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 7 A	-	0.2	0.23	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

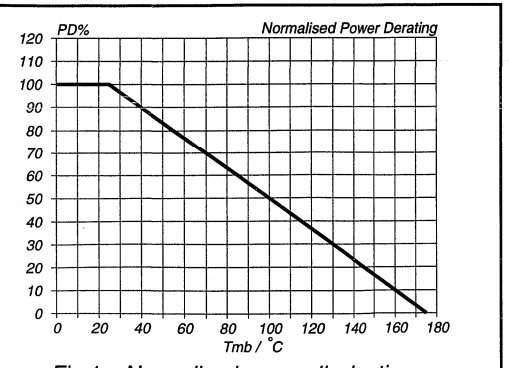


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

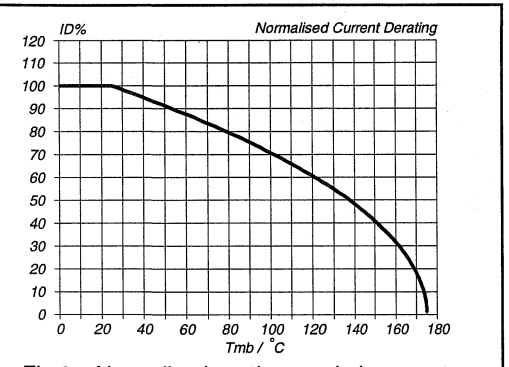


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 10$ V

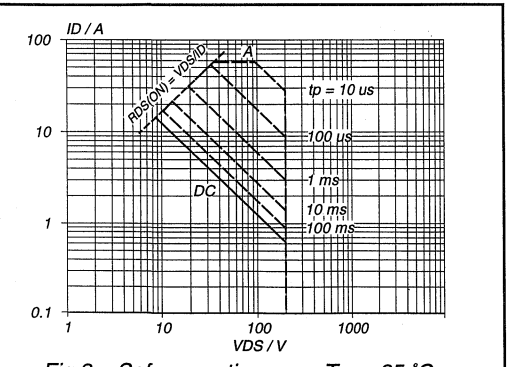


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

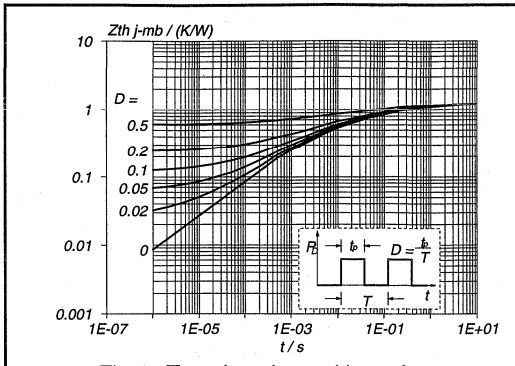


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

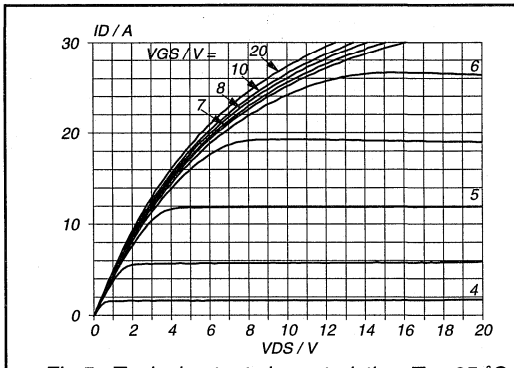


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

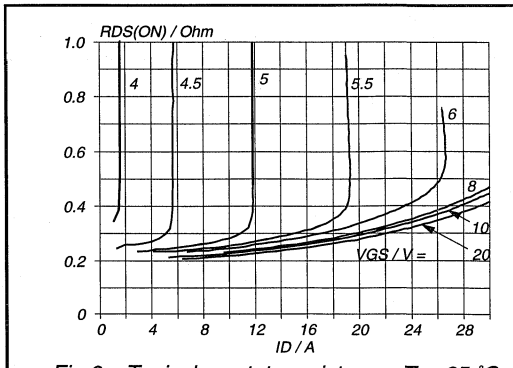


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

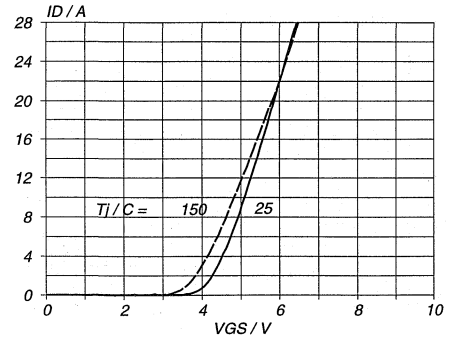


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

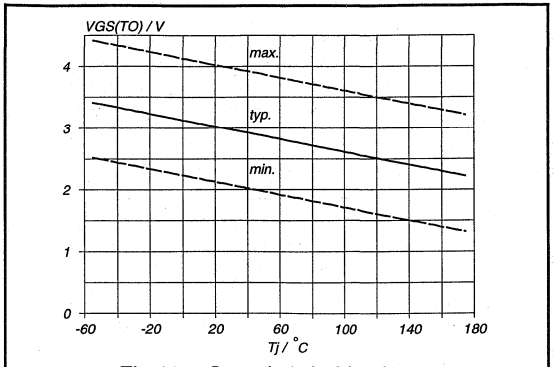


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

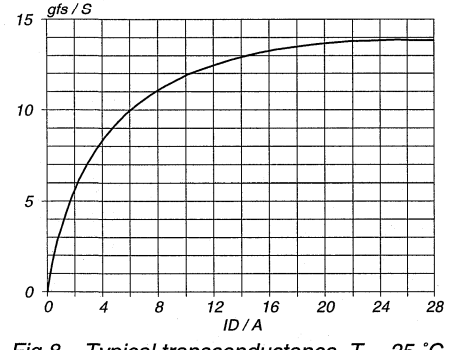


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

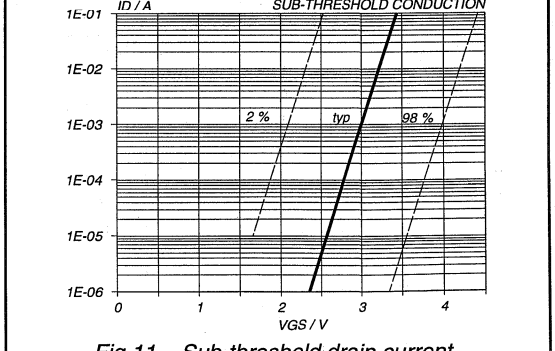


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

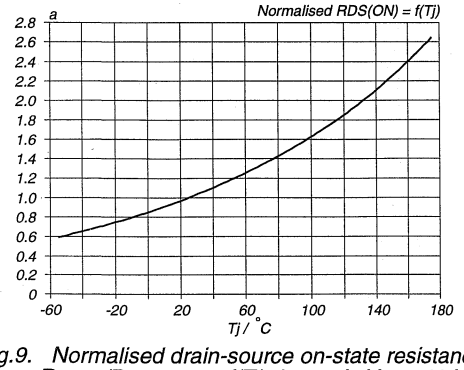


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 10 V

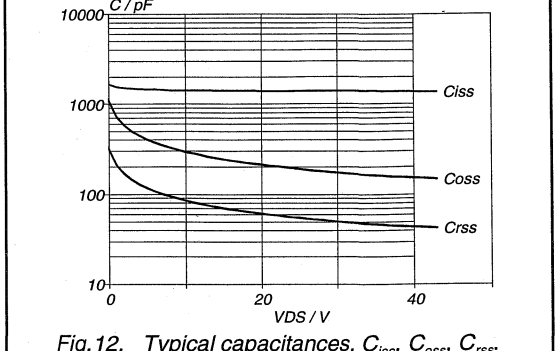


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

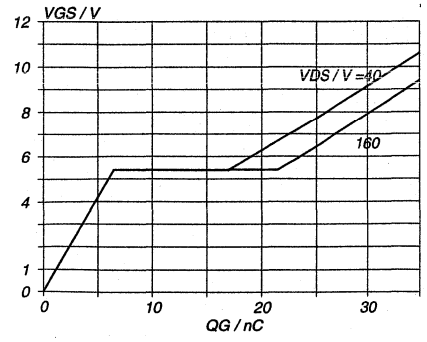


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

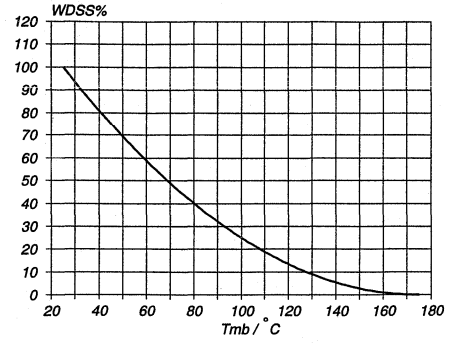


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 14 A

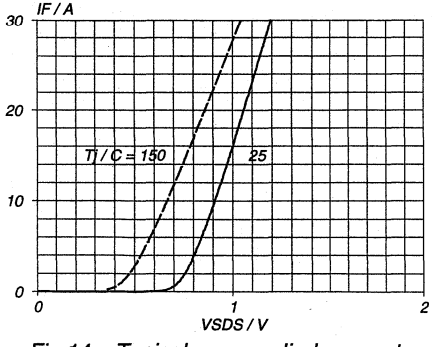


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

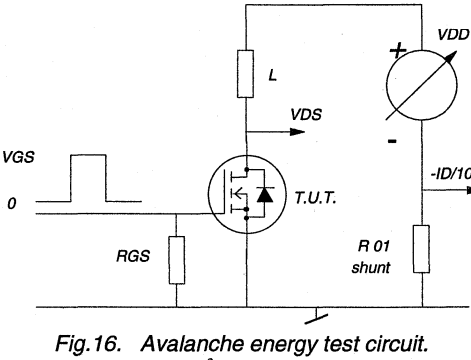


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

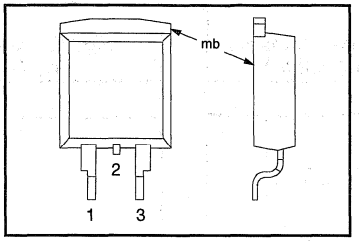
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.028	Ω

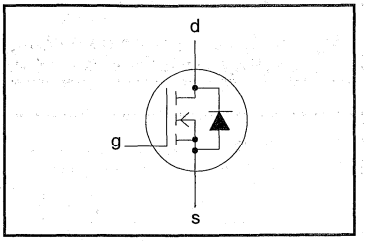
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	36	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 29 A	-	0.024	0.028	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 29 A	17	22	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	800	1000	pF
C_{rss}	Feedback capacitance		-	270	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	70	100	ns
$t_{d\,off}$	Turn-off delay time	R_{GS} = 50 Ω;	-	170	220	ns
t_f	Turn-off fall time	R_{gen} = 50 Ω	-	120	160	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	52	A
I_{DRM}	Pulsed reverse drain current	-	-	-	208	A
V_{SD}	Diode forward voltage	I_F = 52 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 52 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.4	-	µC

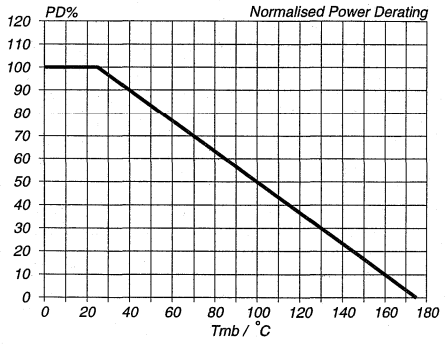


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

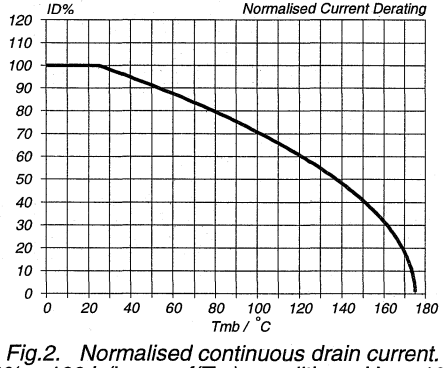


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

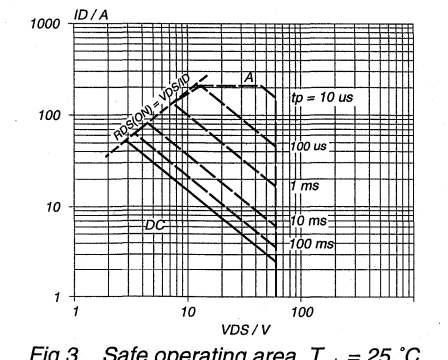


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

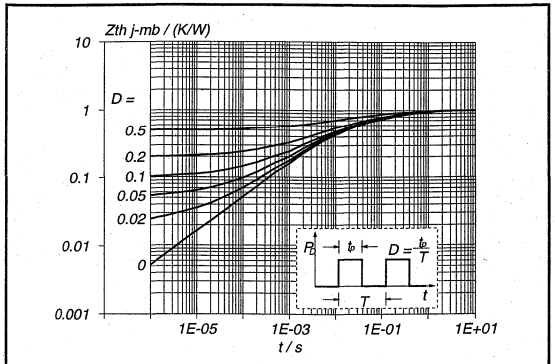


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

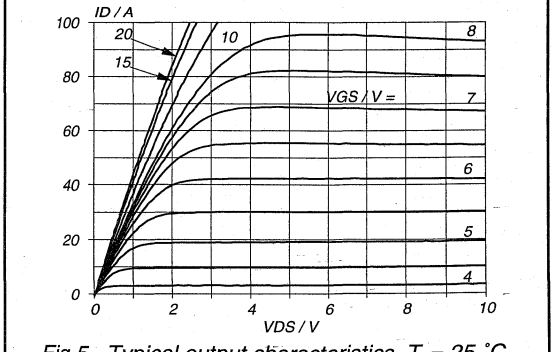


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

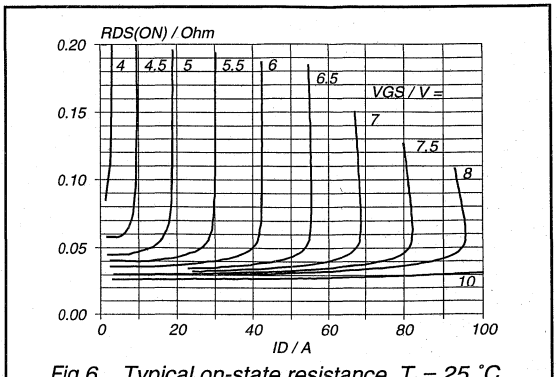


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

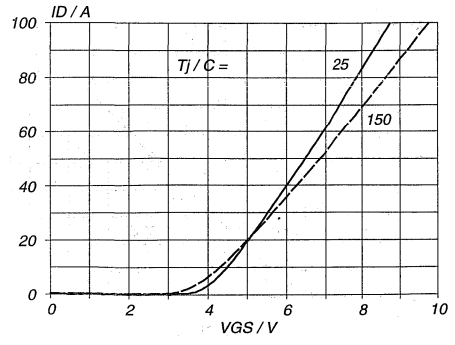


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

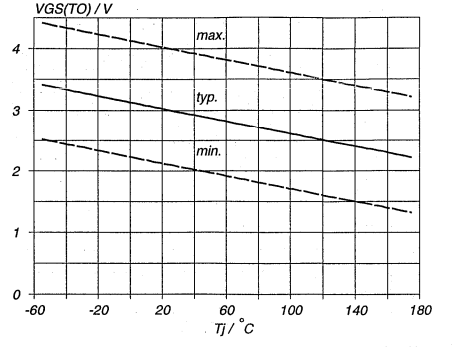


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

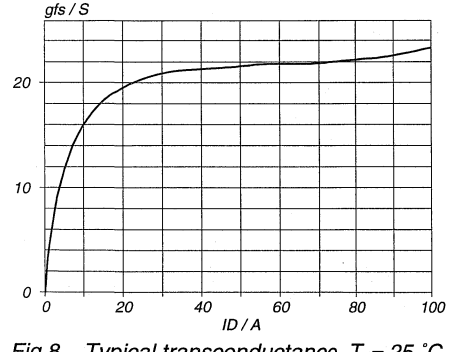


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

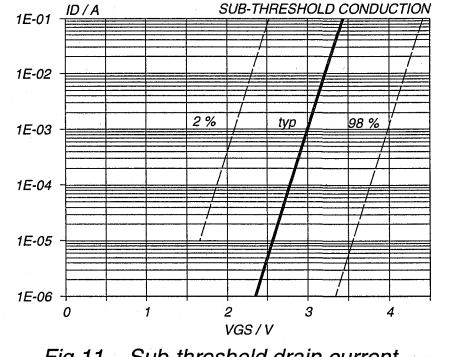


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

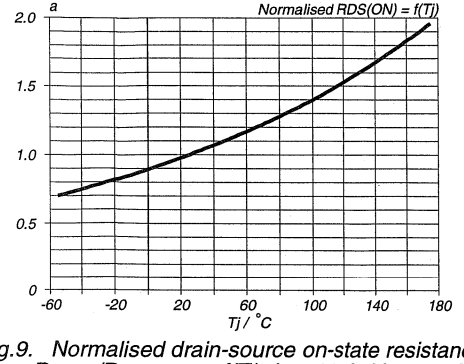


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 29 A; V_{GS} = 10 V

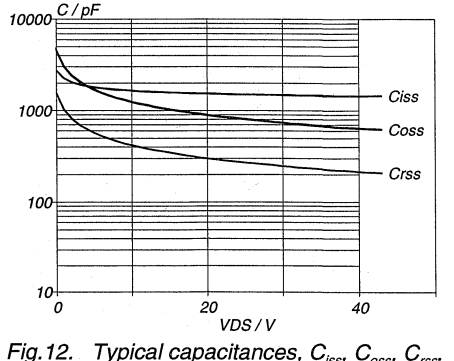


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

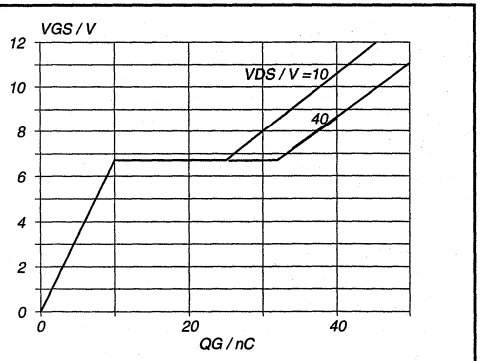


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 52$ A; parameter V_{DS}

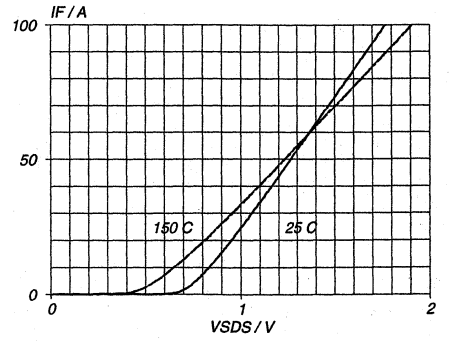


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

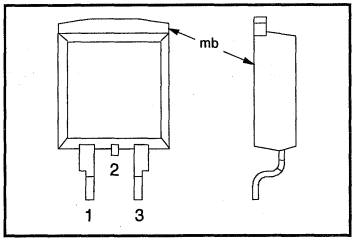
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.057	Ω

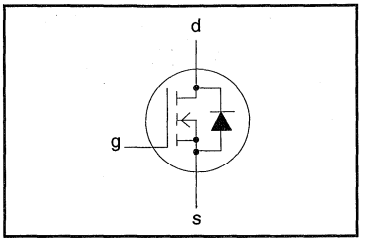
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A	-	0.052	0.057	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	450	600	pF
C_{rss}	Feedback capacitance		-	130	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	150	200	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	65	85	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	34	A
I_{DRM}	Pulsed reverse drain current	-	-	-	136	A
V_{SD}	Diode forward voltage	I_F = 34 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.0	-	µC

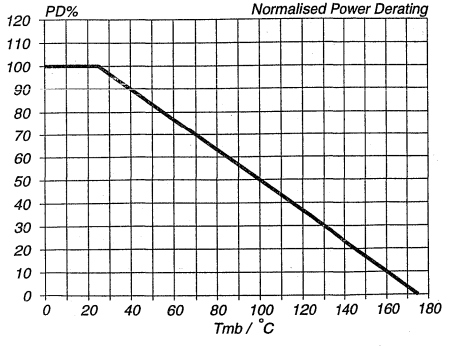


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

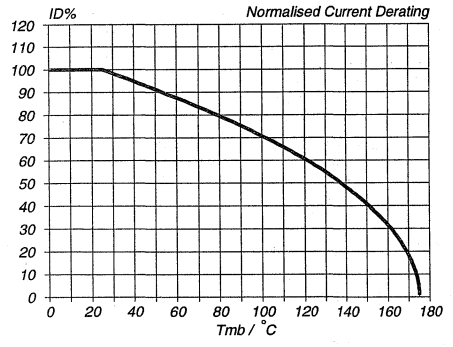


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

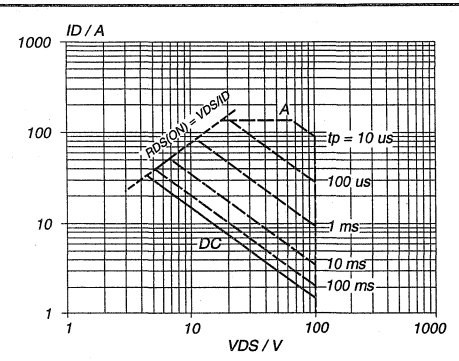


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

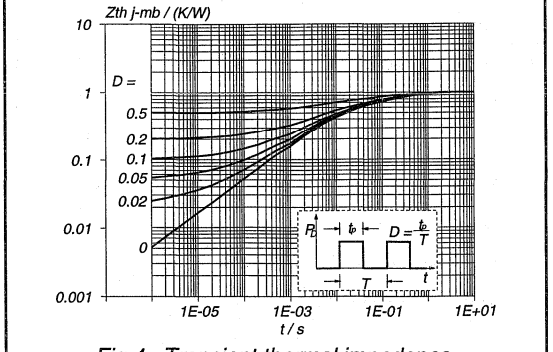


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

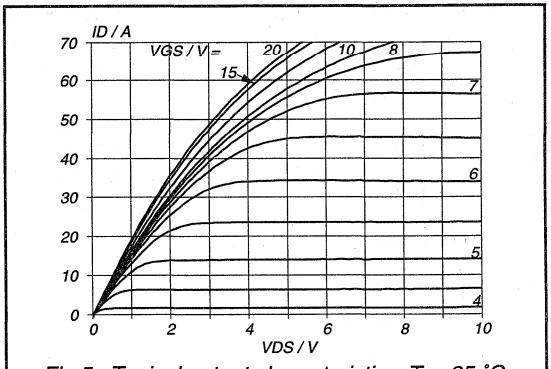


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

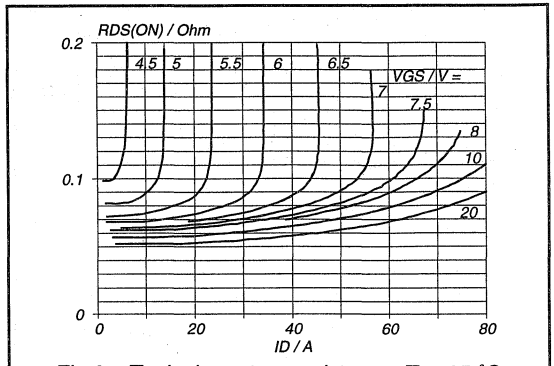


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

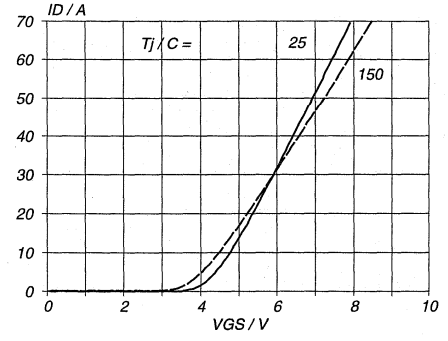


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

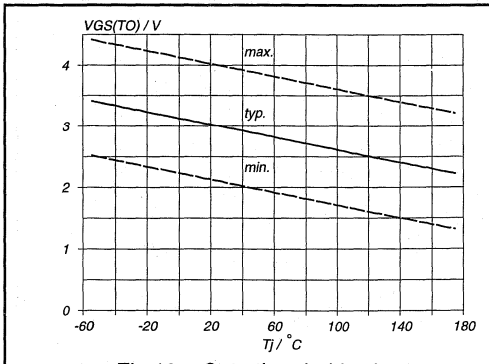


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

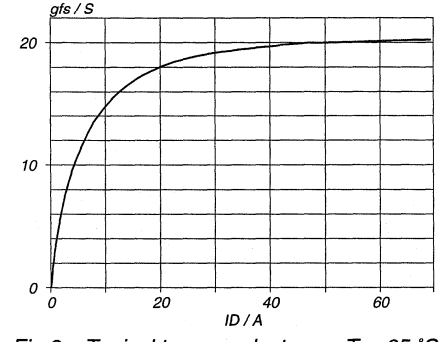


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

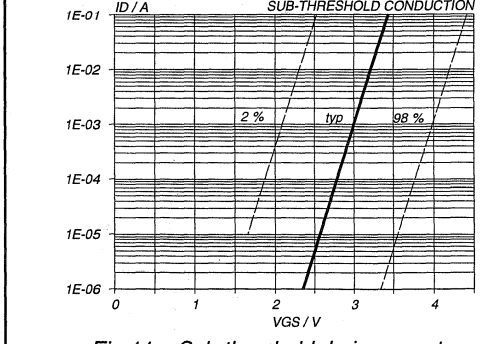


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

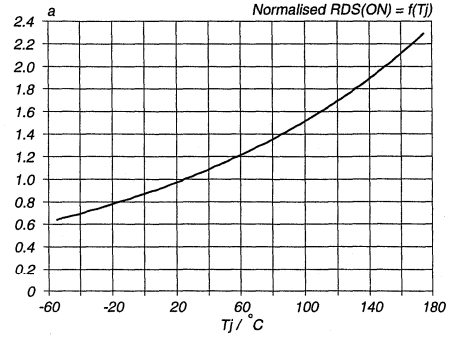


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 15 A; V_{GS} = 10 V

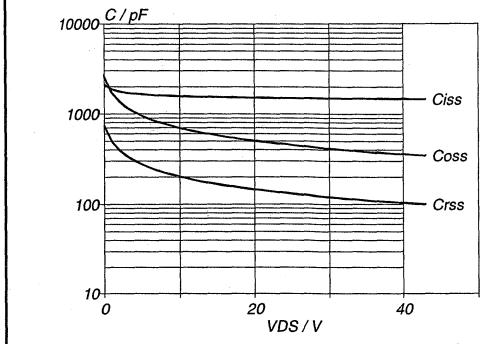


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

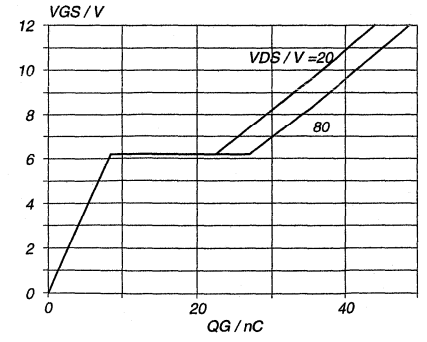


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 34$ A; parameter V_{DS}

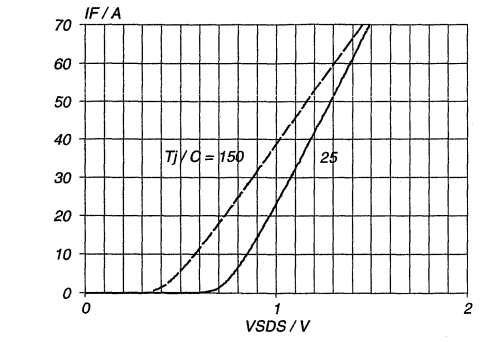


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for use in surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

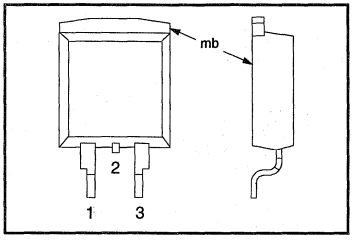
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	19	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	Ω

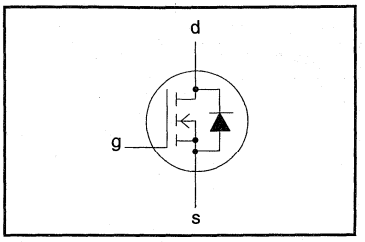
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	19	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	13	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	76	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	8.5	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	400	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	145	185	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	50	70	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	19	A
I_{DRM}	Pulsed reverse drain current	-	-	-	76	A
V_{SD}	Diode forward voltage	I_F = 19 A ; V_{GS} = 0 V	-	1.0	1.7	V
t_{rr}	Reverse recovery time	I_F = 19 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	2.5	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 19 A ; V_{DD} ≤ 30 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	150	mJ

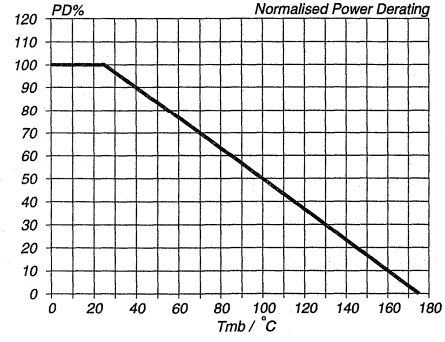


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

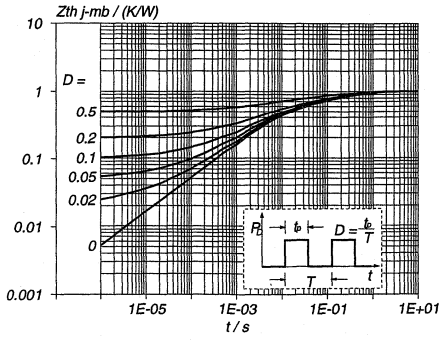


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

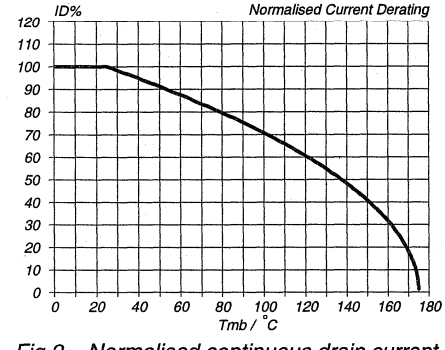


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

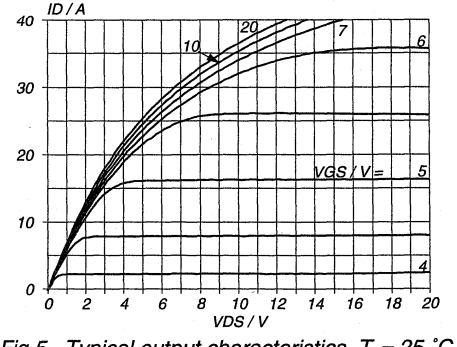


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

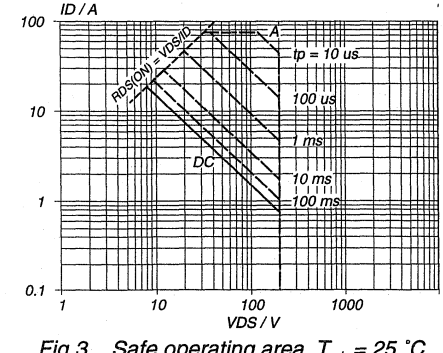


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

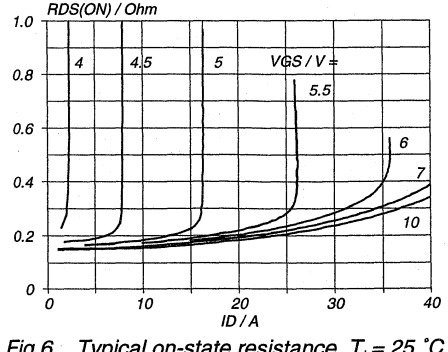


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

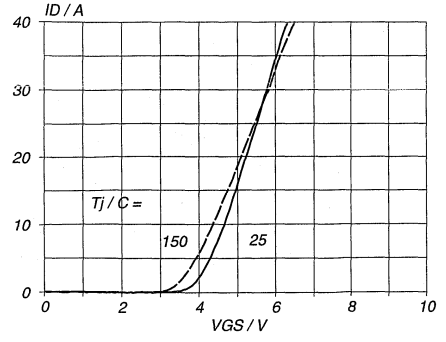


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

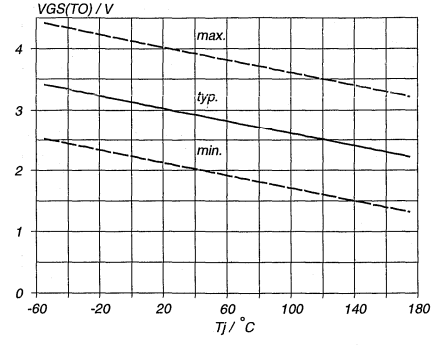


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

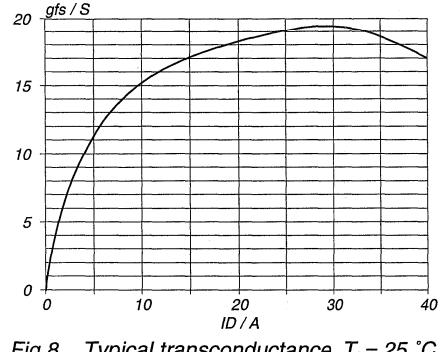


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

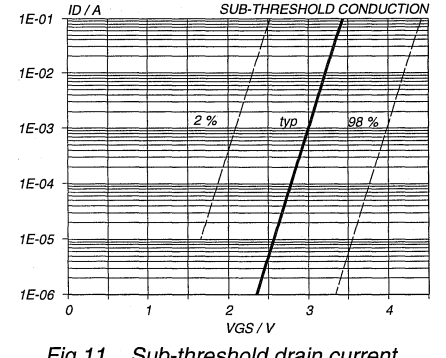


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

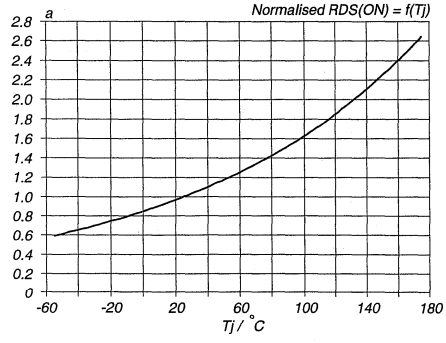


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 10 V

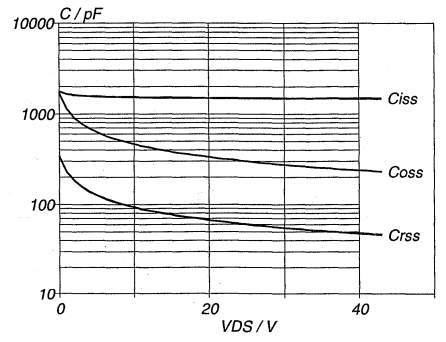


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

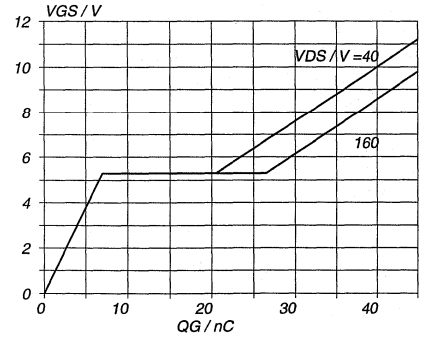


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 19$ A; parameter V_{DS}

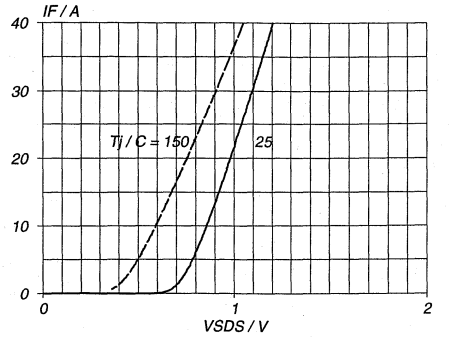


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

PowerMOS transistor
Isolated version of BUK452-60A/B

BUK472-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

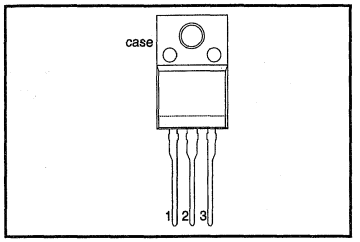
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK472	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	10	9.2	A
P_{tot}	Total power dissipation	22	22	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.13	0.15	Ω

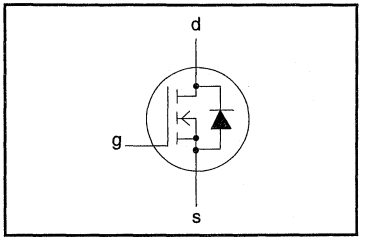
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	10	9.2	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	6.3	5.8	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	40	37	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	22		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.68	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK472-60A**	-	0.11	0.13	Ω
		I_D = 8.5 A **BUK472-60B**	-	0.13	0.15	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	3.5	4.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	70	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	8	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	45	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	10	A
I_{DRM}	Pulsed reverse drain current	-	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 10 A ; V_{GS} = 0 V	-	1.4	1.7	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 15 A ; $V_{DD} \leq$ 30 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	30	mJ

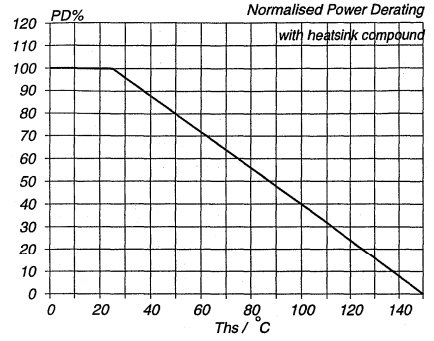


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

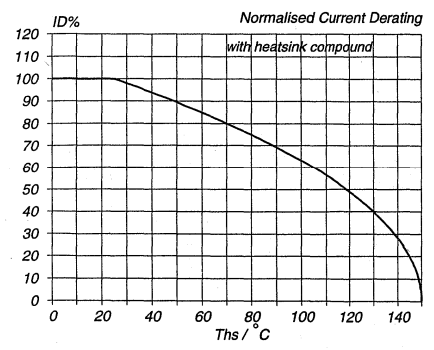


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

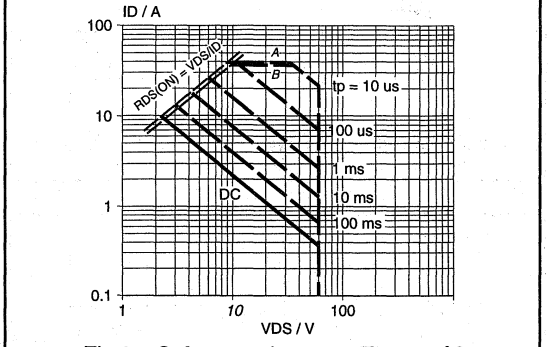


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

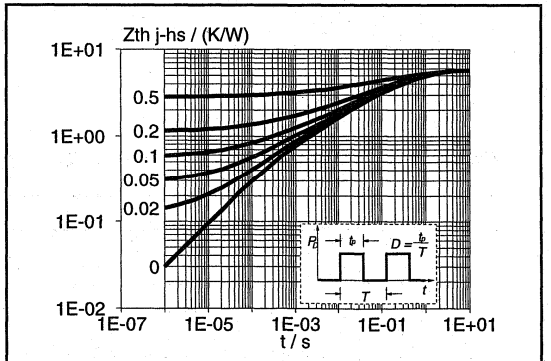


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

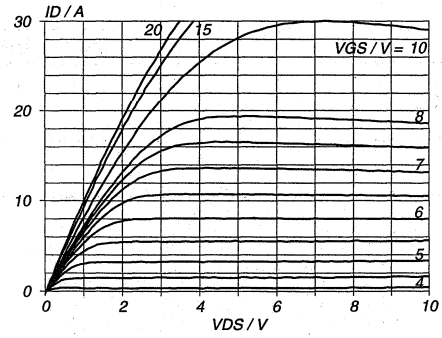


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

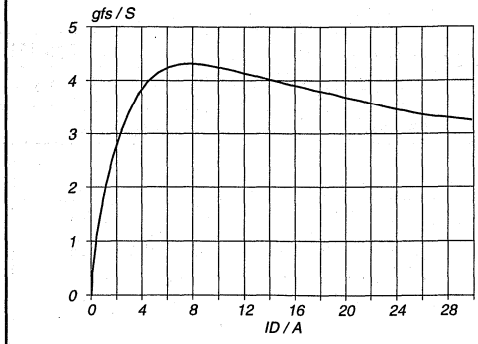


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

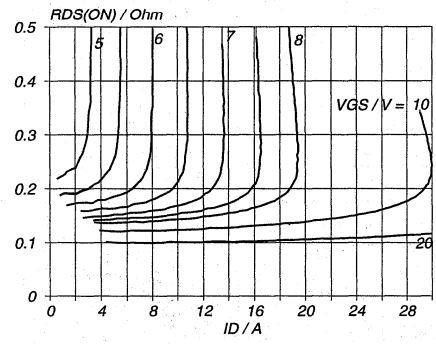


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

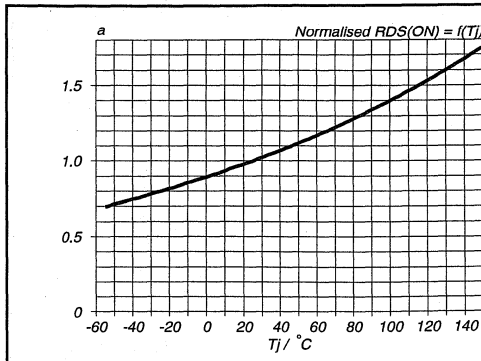


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 8.5 A; V_{GS} = 10 V

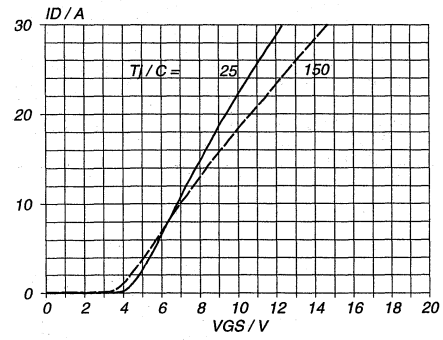


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

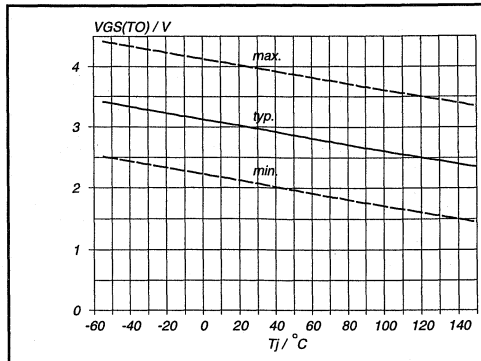


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

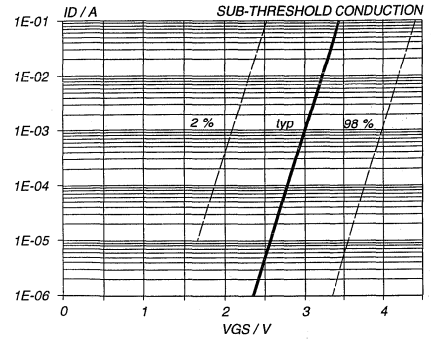


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

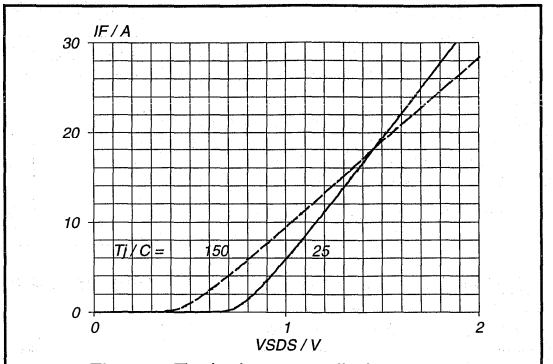


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

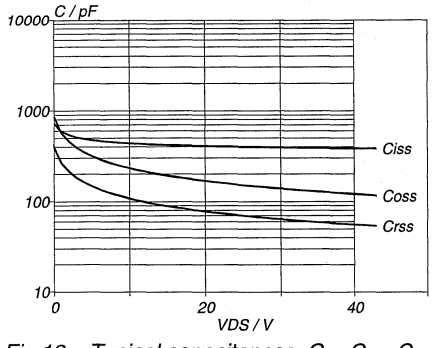


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

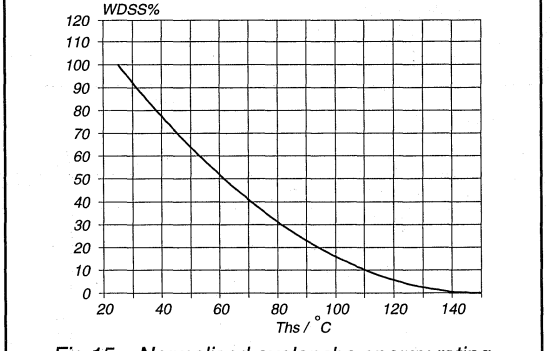


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 15$ A

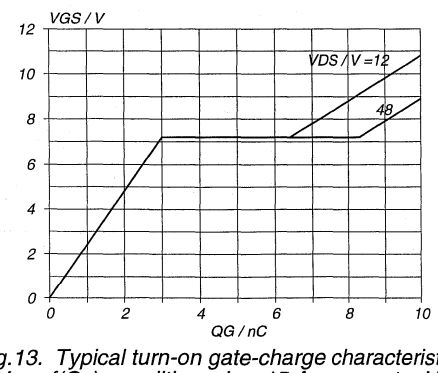


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; *conditions:* $I_D = 15$ A; *parameter* V_{DS}

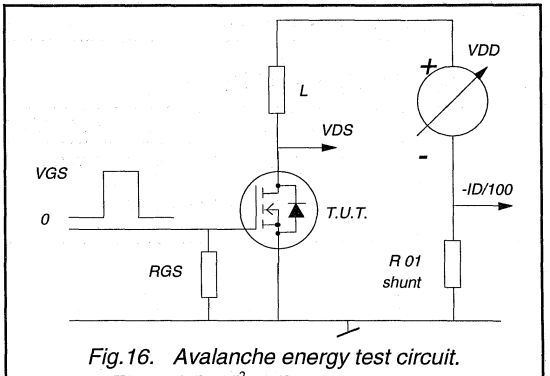


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Isolated version of BUK452-100A/B

BUK472-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

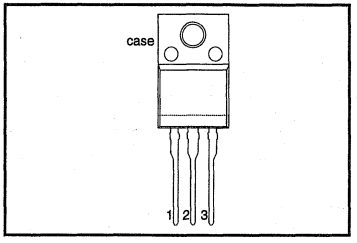
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK472	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	6.6	6.1	A
P_{tot}	Total power dissipation	22	22	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	0.3	Ω

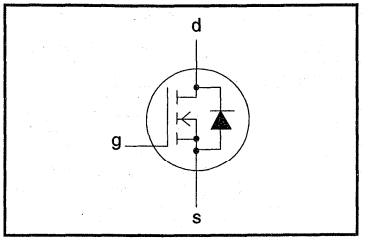
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	6.6	6.1	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.1	3.8	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	26	24	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	22		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.68	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK472-100A**	-	0.22	0.25	Ω
		I_D = 5.5 A **BUK472-100B**	-	0.25	0.3	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	6.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	26	A
V_{SD}	Diode forward voltage	I_F = 6.6 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 6.6 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

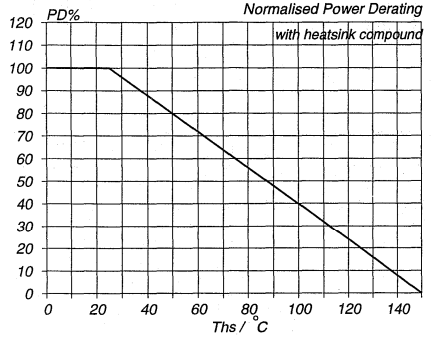


Fig.1. Normalised power dissipation. PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

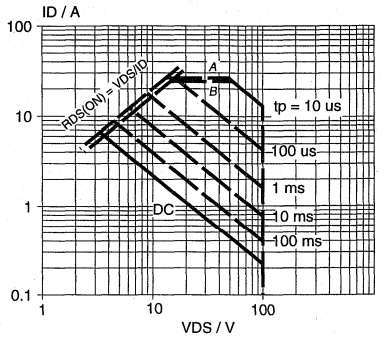


Fig.3. Safe operating area. T_{hs} = 25 °C I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

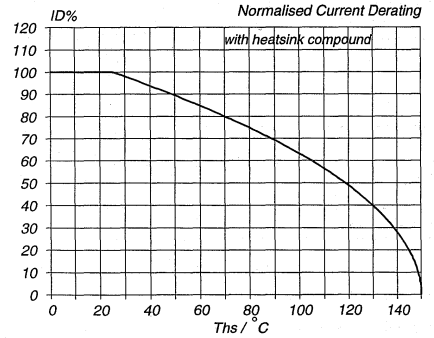


Fig.2. Normalised continuous drain current. ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

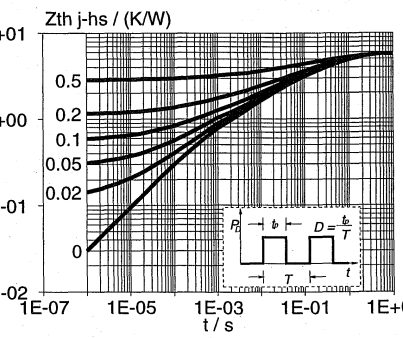


Fig.4. Transient thermal impedance. $Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

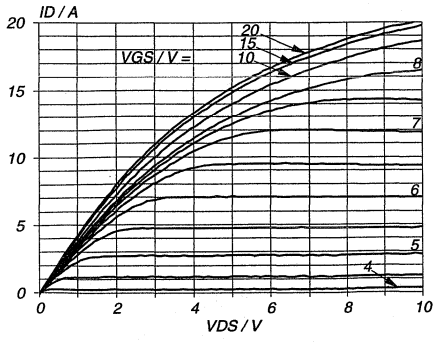


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

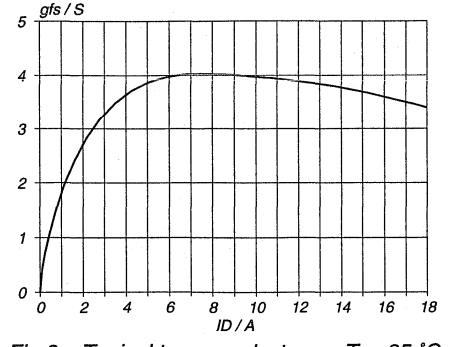


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

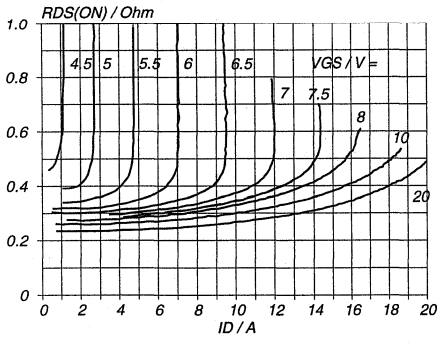


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

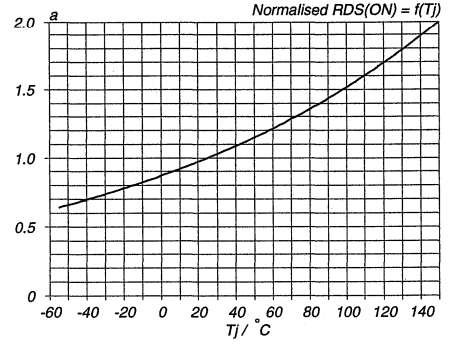


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

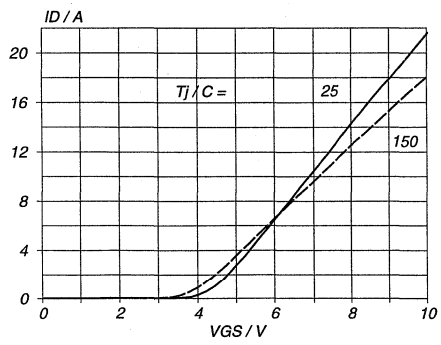


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

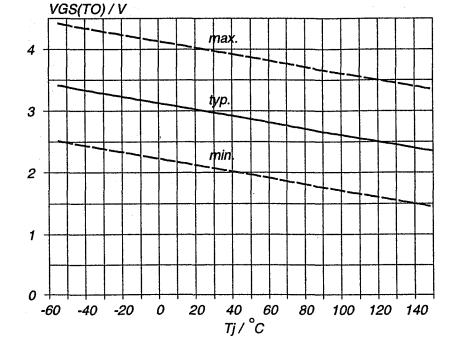


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

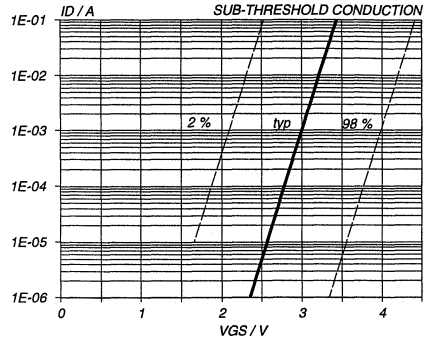


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

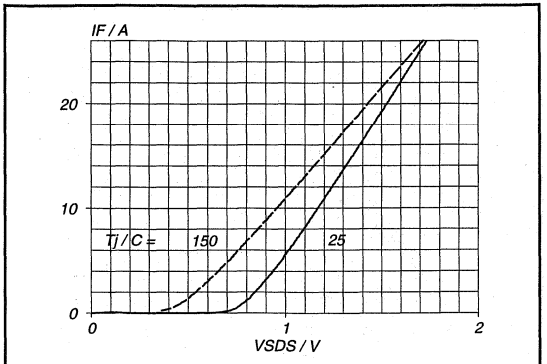


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

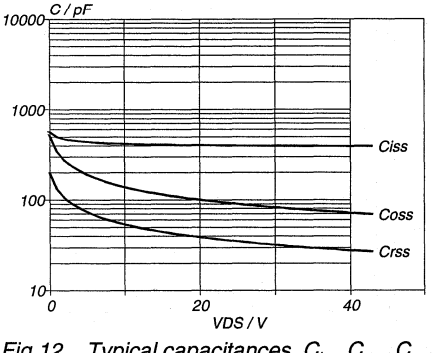


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

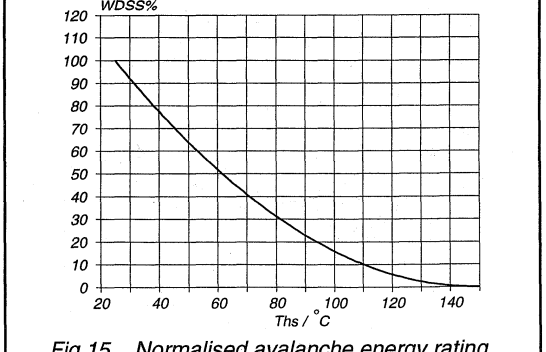


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 11$ A

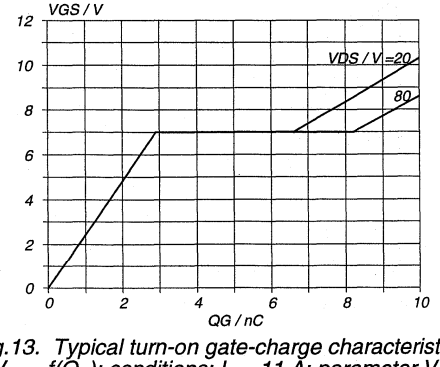


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 11$ A; *parameter* V_{DS}

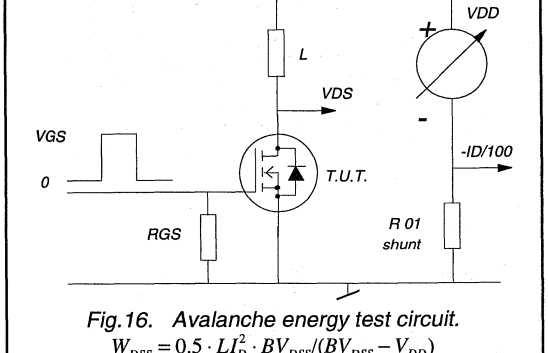


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Isolated version of BUK453-60A/B

BUK473-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

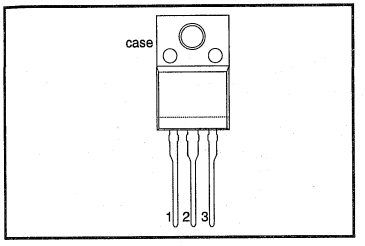
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK473	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	13	12	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	0.1	Ω

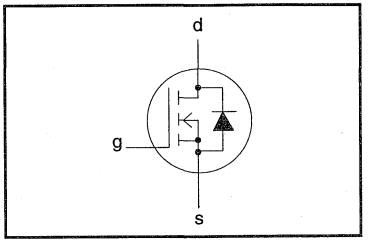
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	13	12	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	8.2	7.6	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	52	48	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK473-60A**	-	0.065	0.08	Ω
		I_D = 9 A **BUK473-60B**	-	0.08	0.10	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 9 A	4.5	6.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	120	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	55	80	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.20	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 22 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

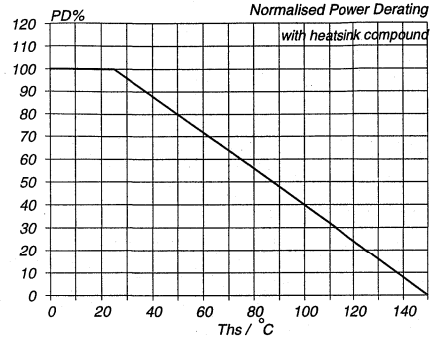


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

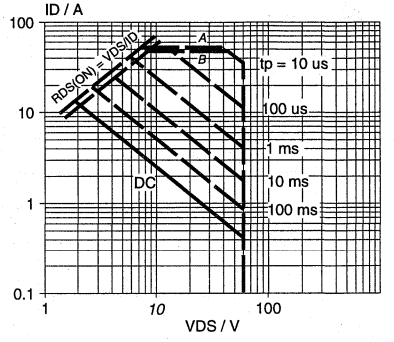


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

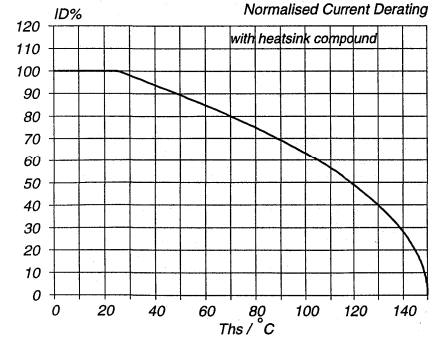


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

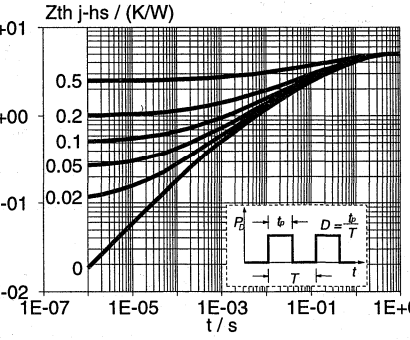


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

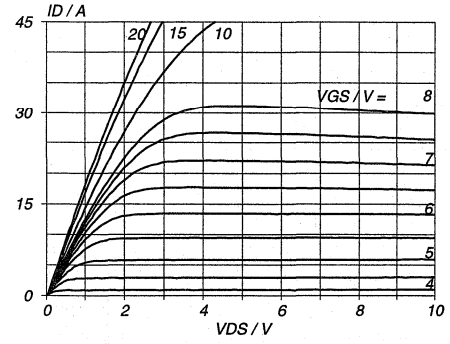


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

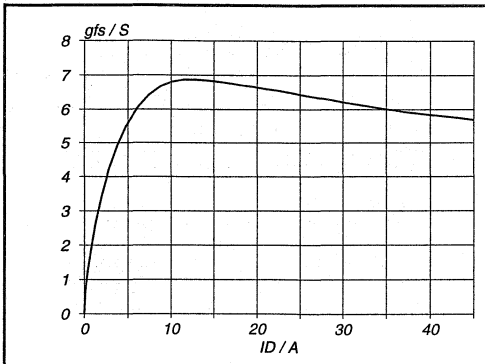


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

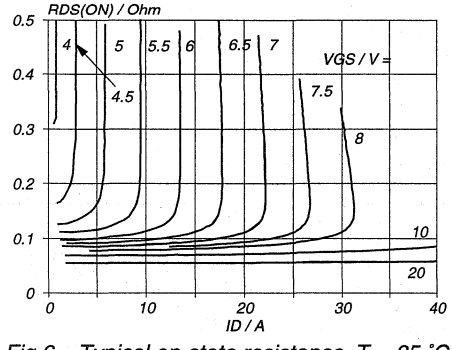


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

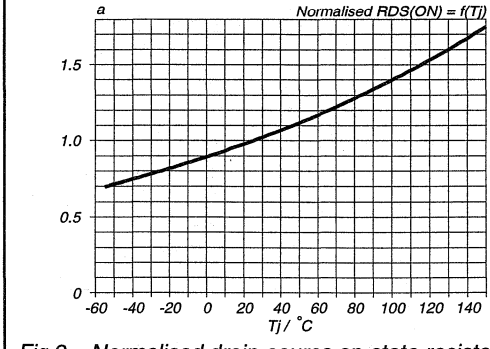


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 9 A; V_{GS} = 10 V

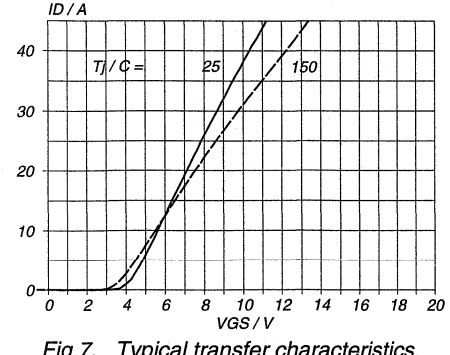


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

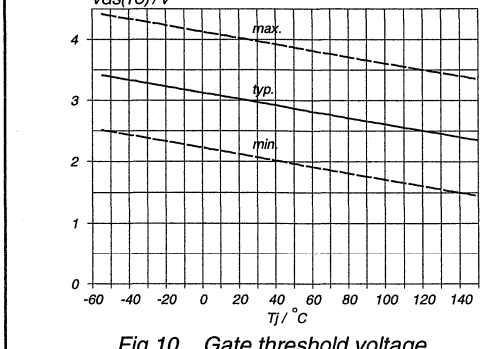


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

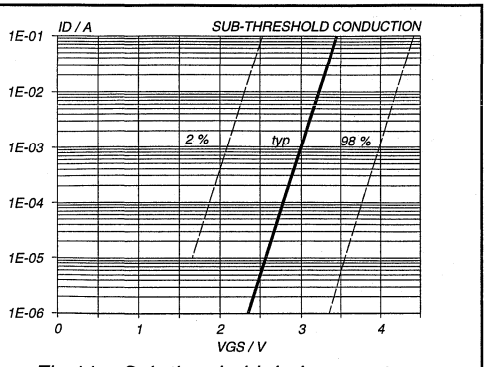


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

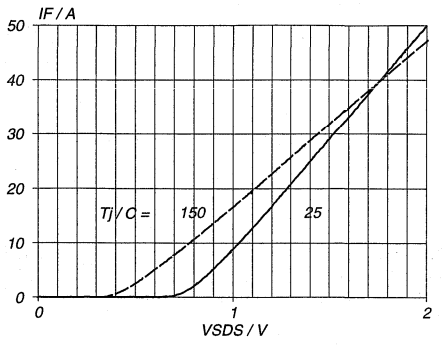


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

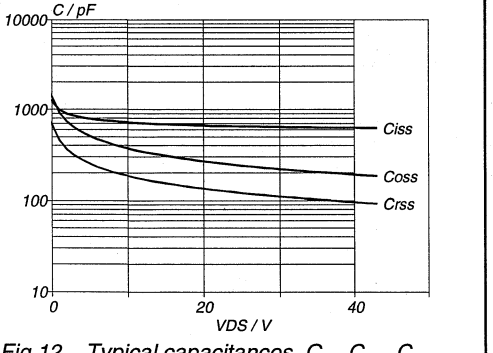


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

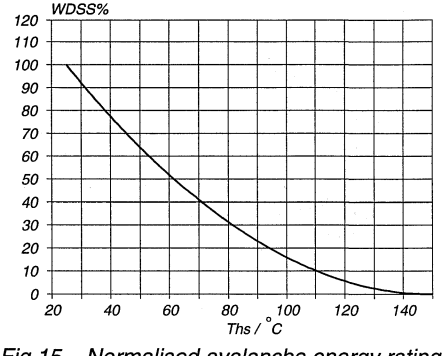


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 22$ A

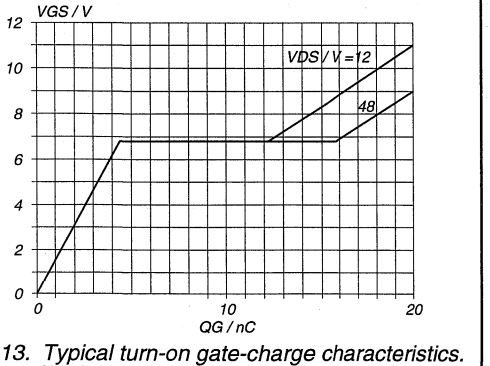


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 22$ A; parameter V_{DS}

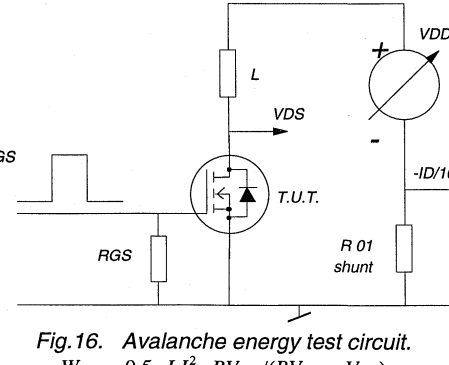


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Isolated version of BUK453-100A/B

BUK473-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

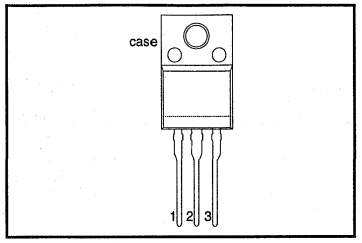
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK473	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	9	8	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	0.2	Ω

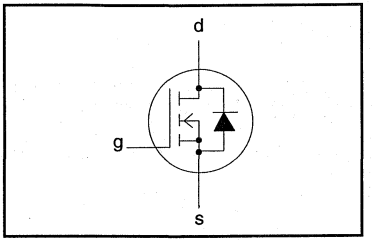
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	9	8	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	5.7	5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	36	32	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK473-100A**	-	0.15	0.16	Ω
		I_D = 5 A **BUK473-100B**	-	0.17	0.2	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.5	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	70	mJ

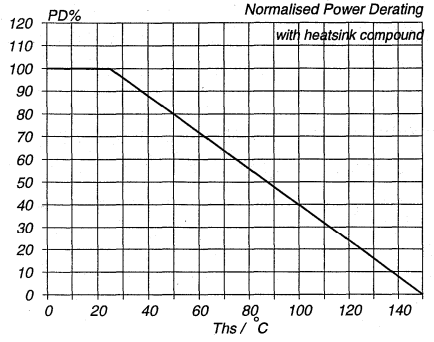


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

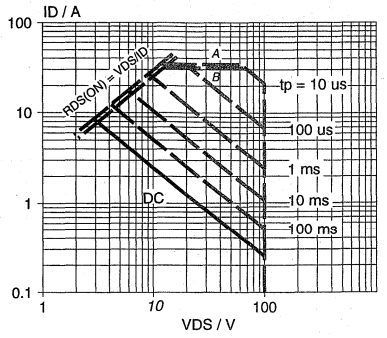


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

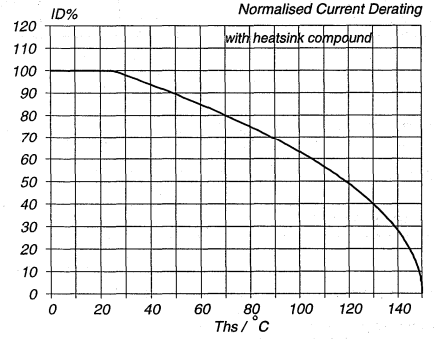


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

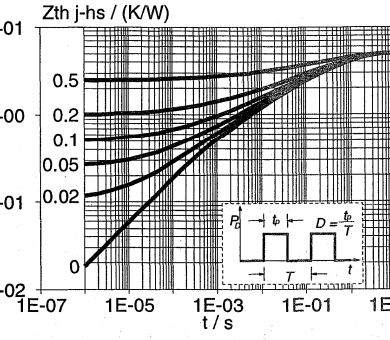


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

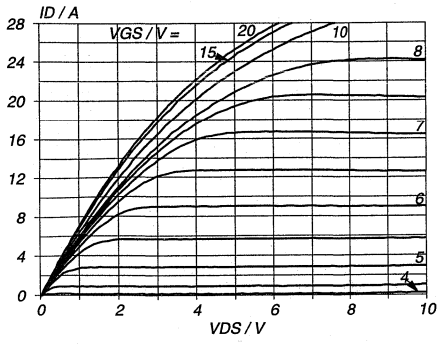


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

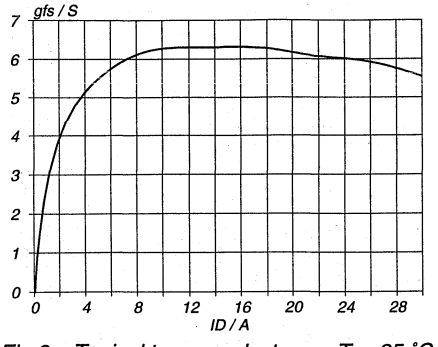


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

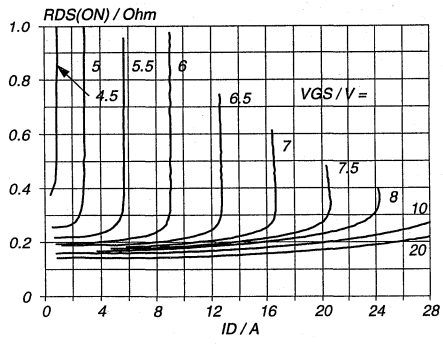


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

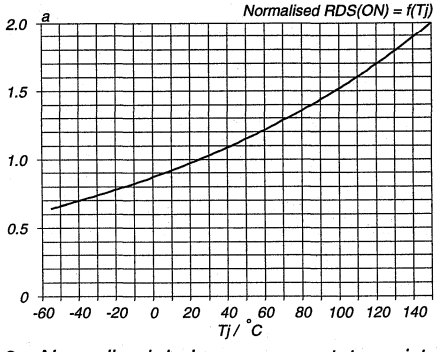


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 5 A; V_{GS} = 10 V

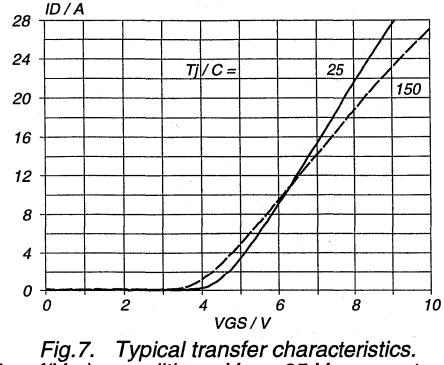


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

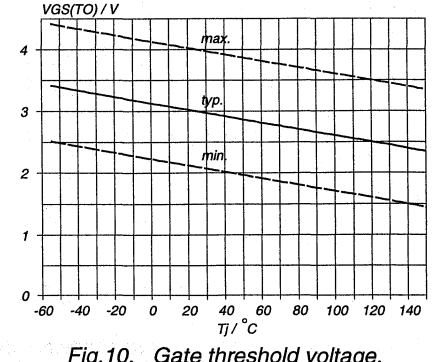


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

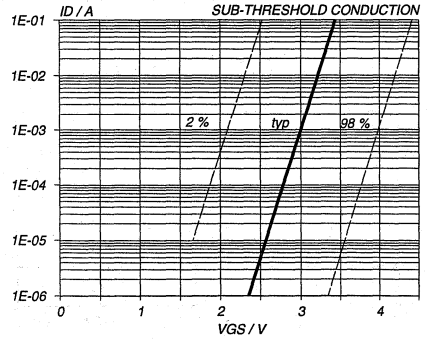


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

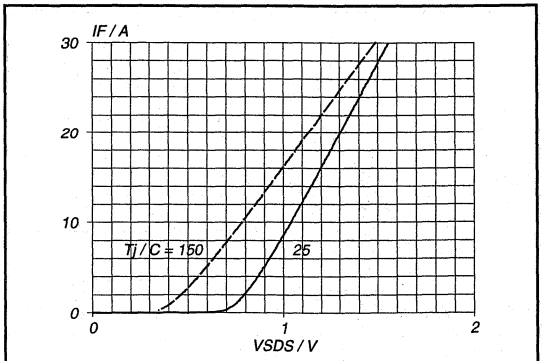


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

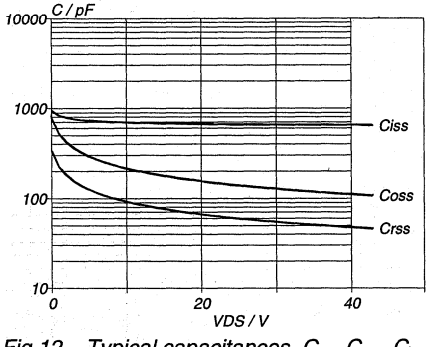


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

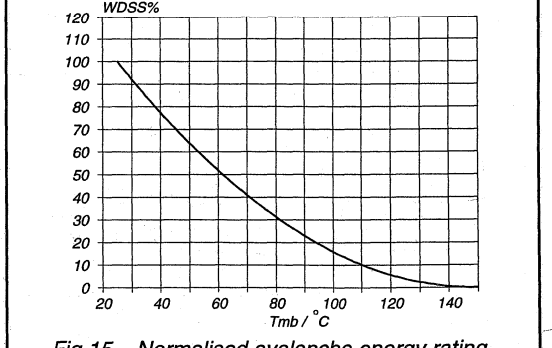


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 14$ A

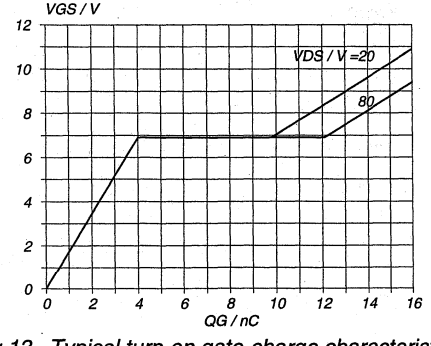


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 14$ A; *parameter* V_{DS}

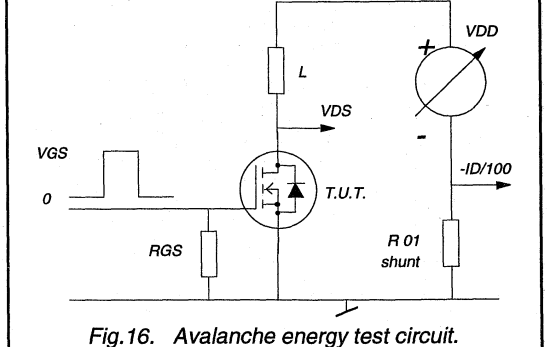


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

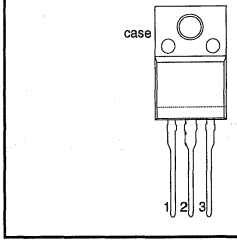
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	21	A
P_{tot}	Total power dissipation	30	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	38	mΩ

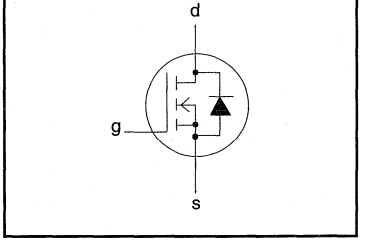
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	21	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	13	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	84	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	30	38	mΩ

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	7	14	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	900	1600	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	55	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	75	125	ns
t_f	Turn-off fall time		-	60	100	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	21	A
I_{DRM}	Pulsed reverse drain current	-	-	-	84	A
V_{SD}	Diode forward voltage	I_F = 21 A ; V_{GS} = 0 V	-	0.9	1.8	V
t_{rr}	Reverse recovery time	I_F = 21 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

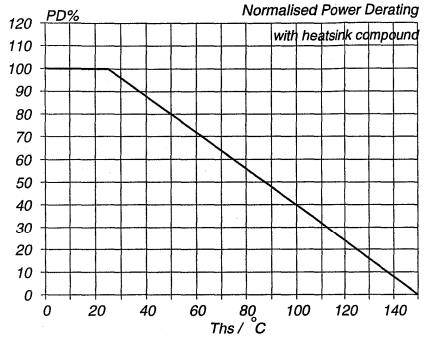


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

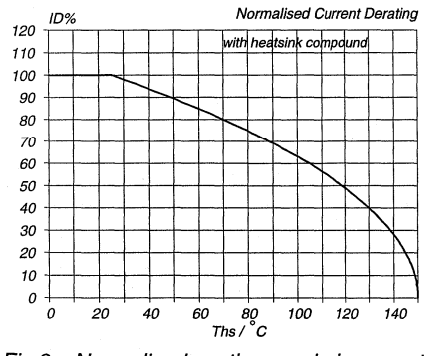


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

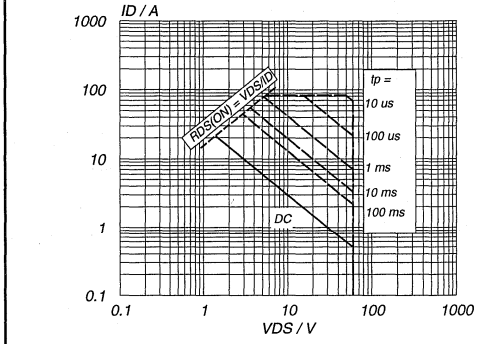


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

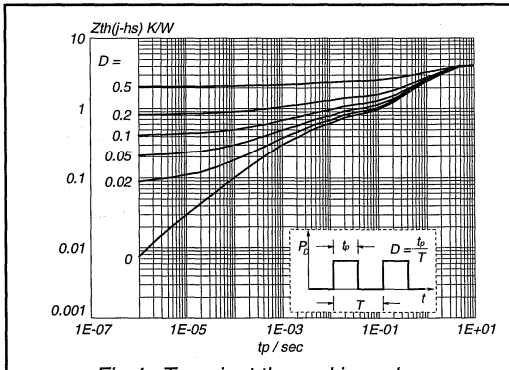


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

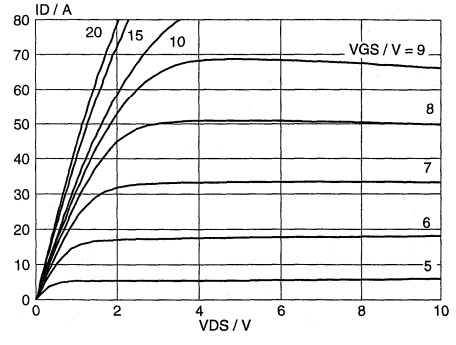


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

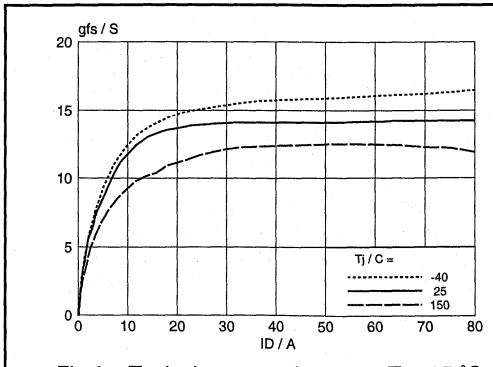


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

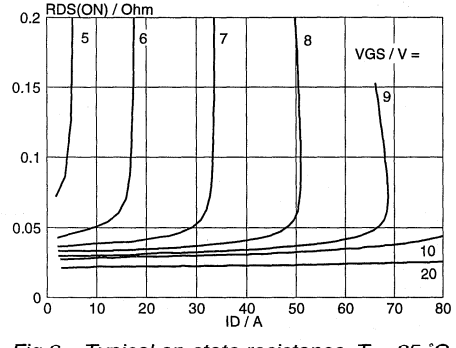


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

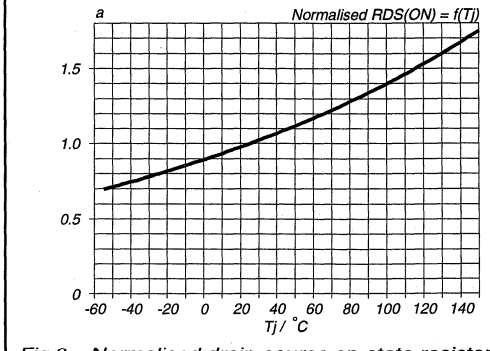


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

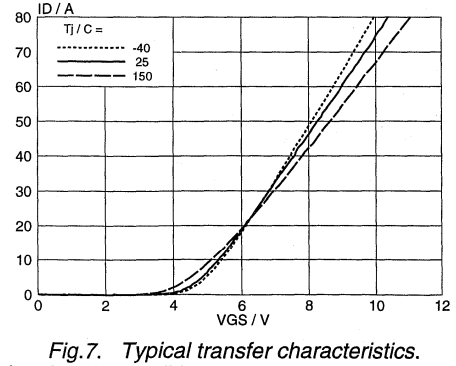


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 15 V; parameter T_j

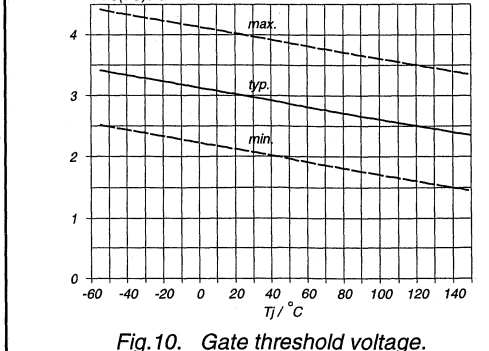


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

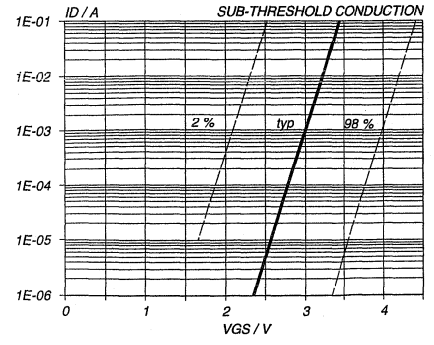


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

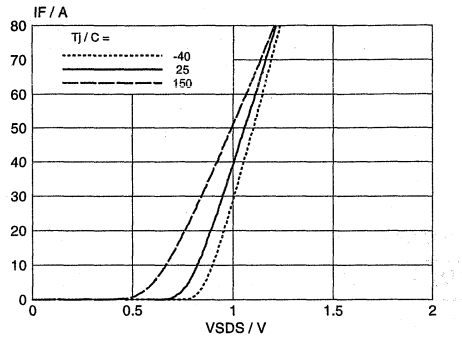


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

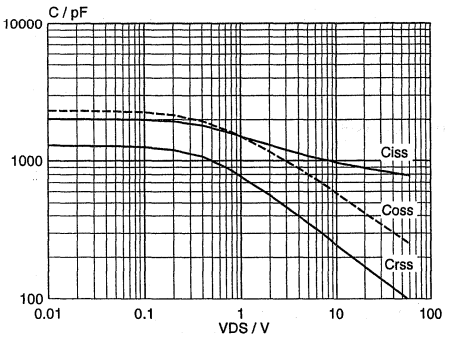


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

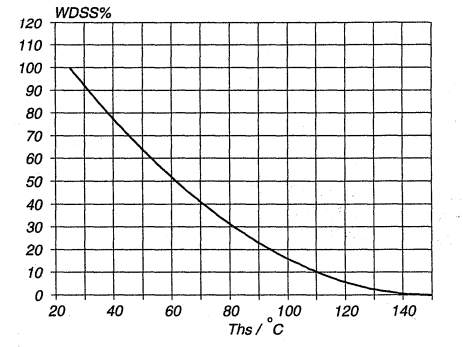


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: I_D = 41 A

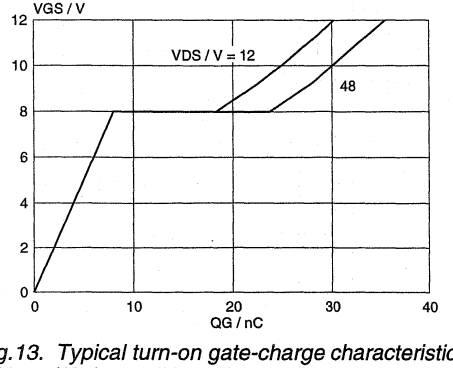


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 41 A; parameter V_{DS}

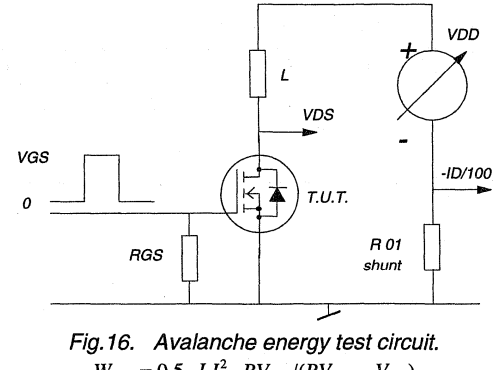


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Isolated version of BUK454-200A/B

BUK474-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

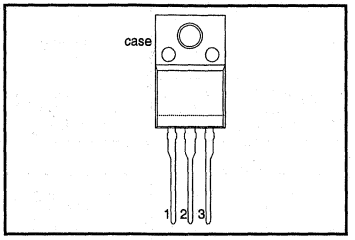
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK474	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	5.3	4.7	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	0.5	Ω

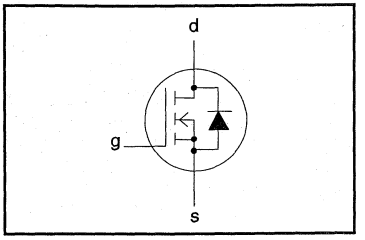
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	5.3	4.7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	3.3	3.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	21	19	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK474-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK474-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	5.3	A
I_{DRM}	Pulsed reverse drain current	-	-	-	21	A
V_{SD}	Diode forward voltage	I_F = 5.3 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 5.3 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.9	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

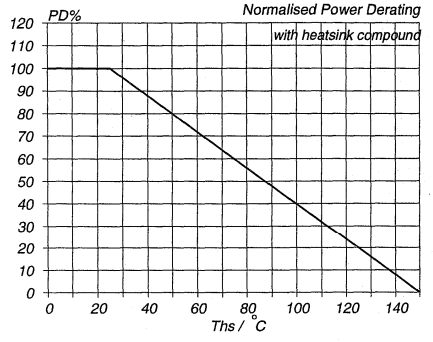


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

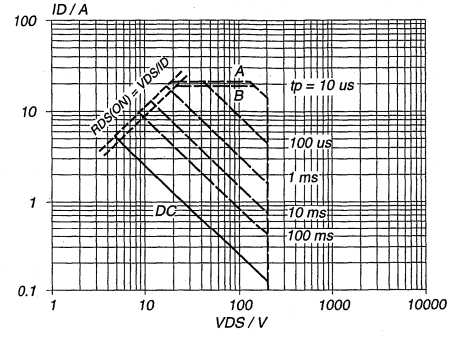


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

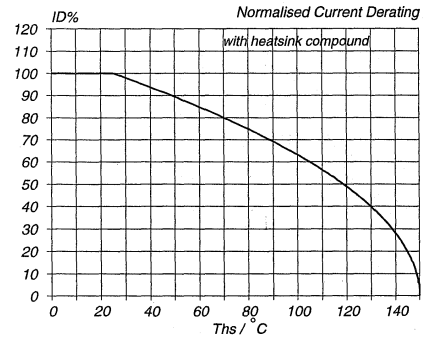


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

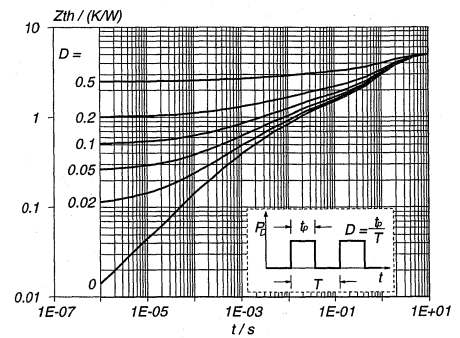


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

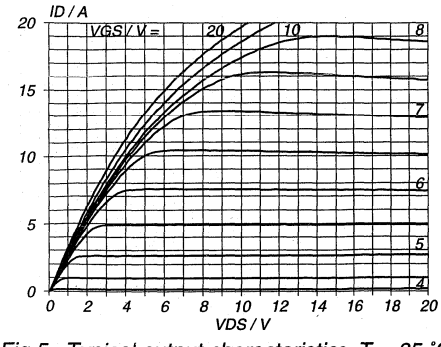


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

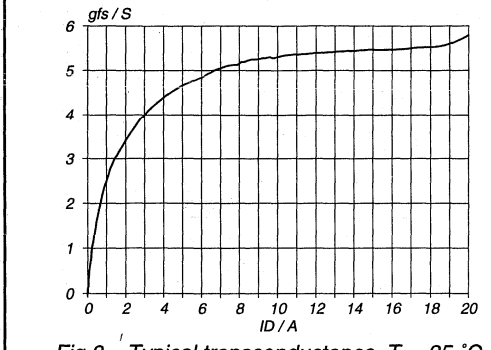


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

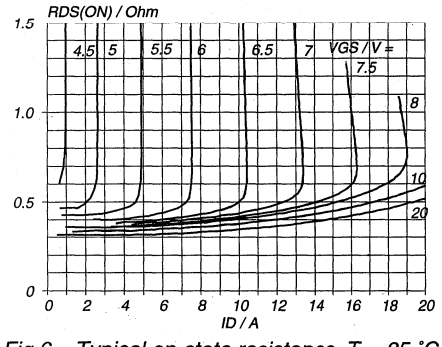


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

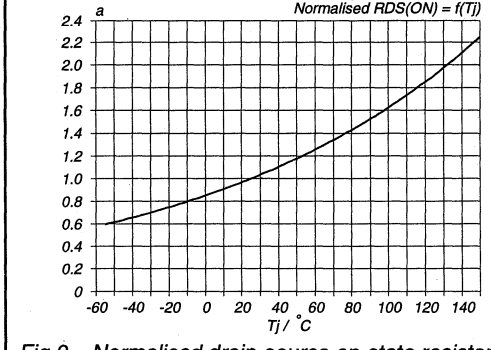


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

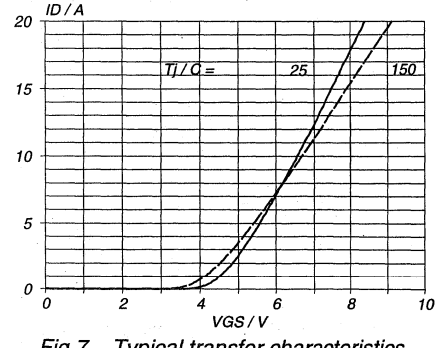


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

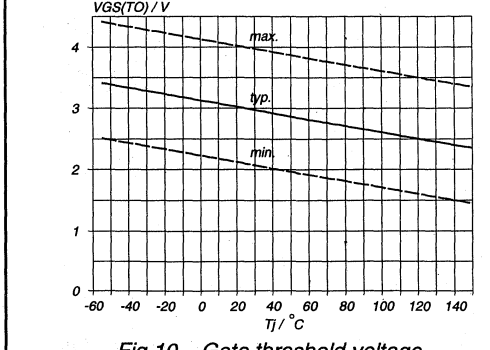


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

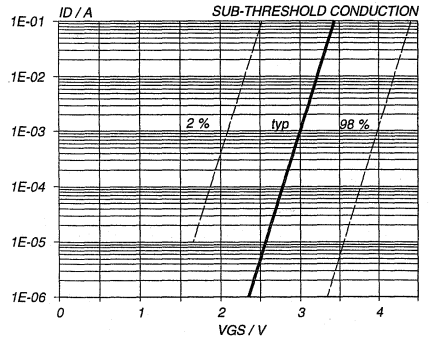


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

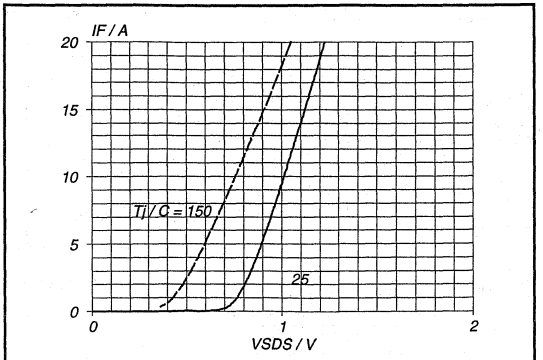


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

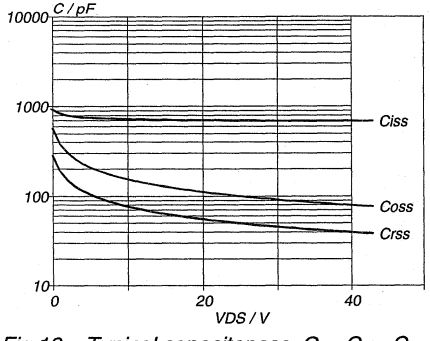


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

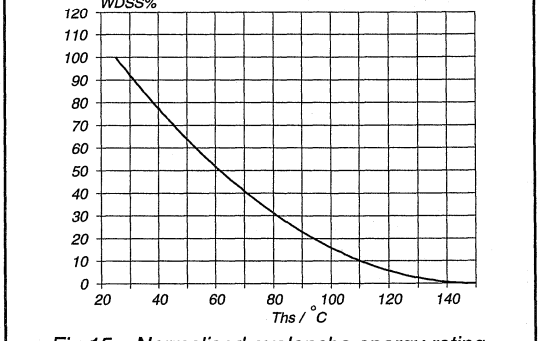


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 9$ A

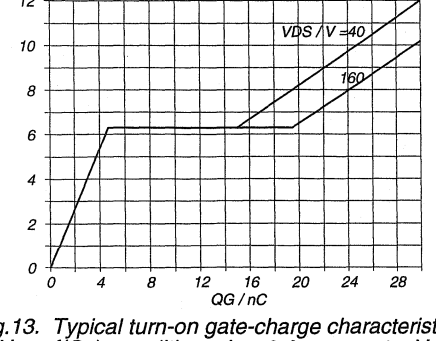


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 9$ A; *parameter* V_{DS}

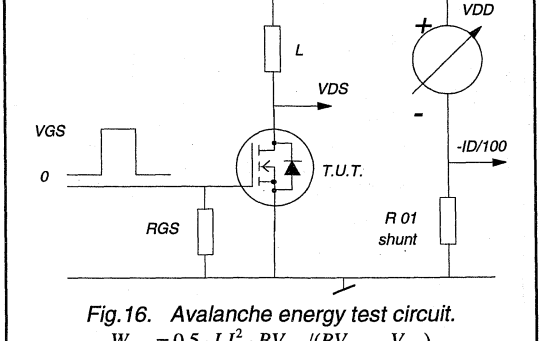


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Isolated version of BUK455-60A/B

BUK475-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

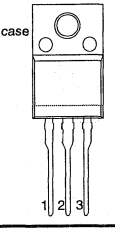
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK475	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	21	20	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.038	0.045	Ω

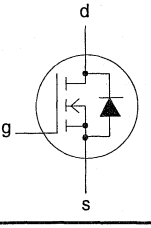
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-60A	-60B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	21	20	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	13	12.6	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	84	80	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK475-60A**	-	0.03	0.038	Ω
		I_D = 20 A **BUK475-60B**	-	0.04	0.045	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	8	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	560	750	pF
C_{rss}	Feedback capacitance		-	300	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	125	160	ns
t_f	Turn-off fall time		-	100	130	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	21	A
I_{DRM}	Pulsed reverse drain current	-	-	-	84	A
V_{SD}	Diode forward voltage	I_F = 21 A ; V_{GS} = 0 V	-	1.4	1.8	V
t_{rr}	Reverse recovery time	I_F = 21 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

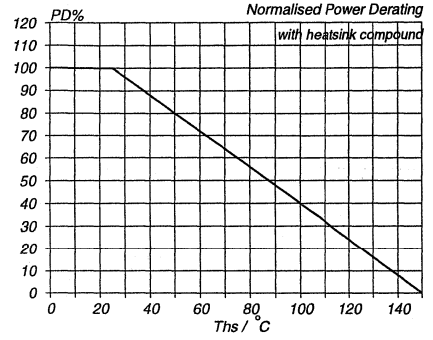


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

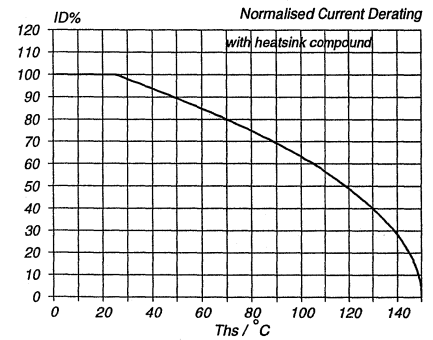


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

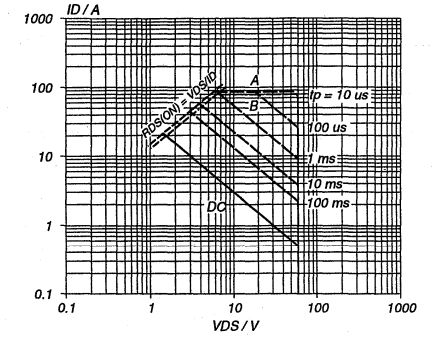


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

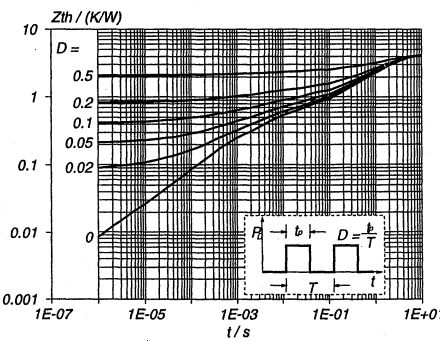


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

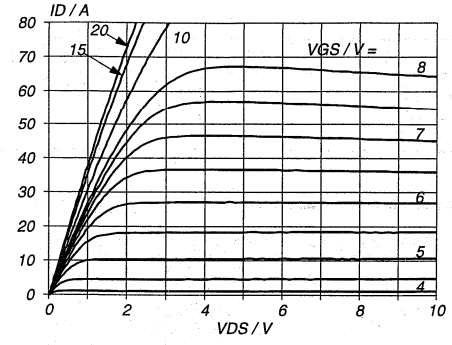


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

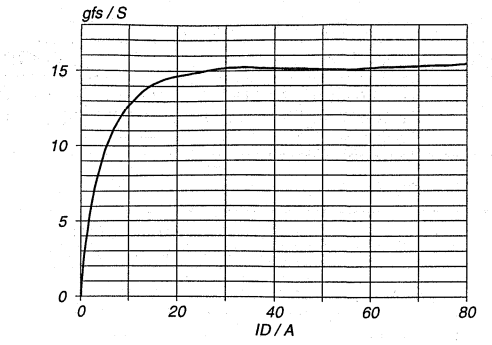


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

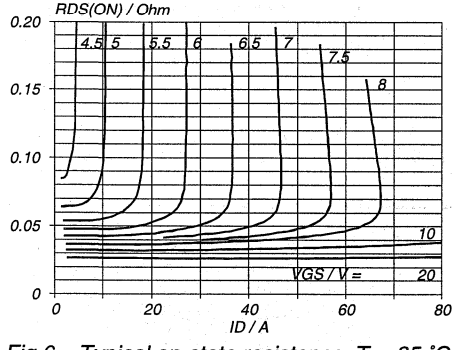


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

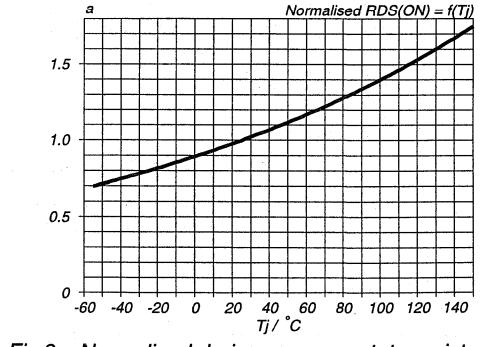


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

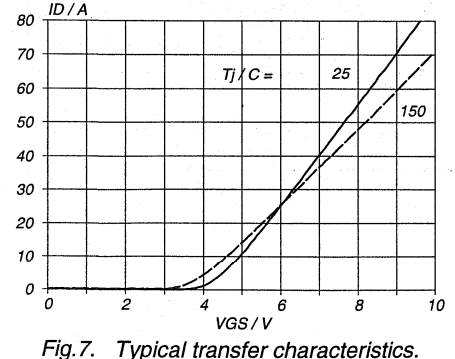


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

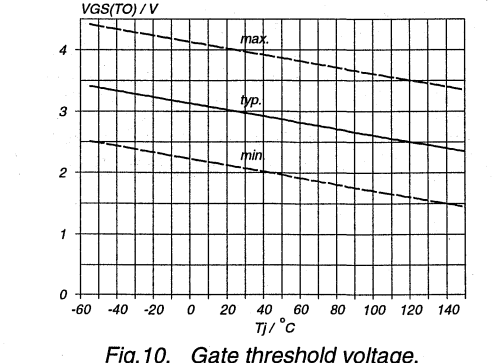


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

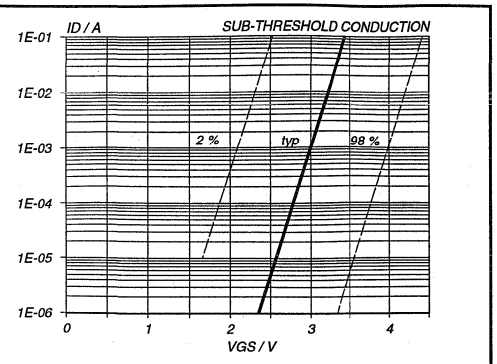


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

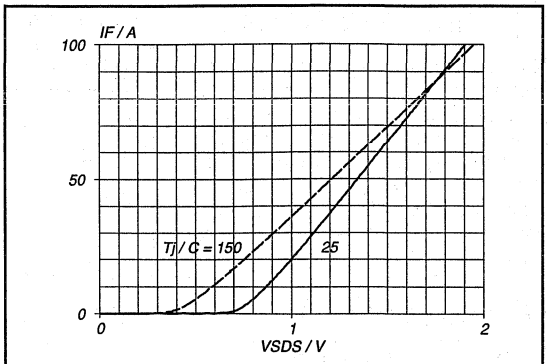


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

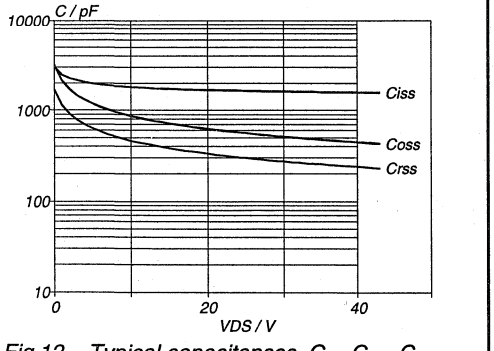


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

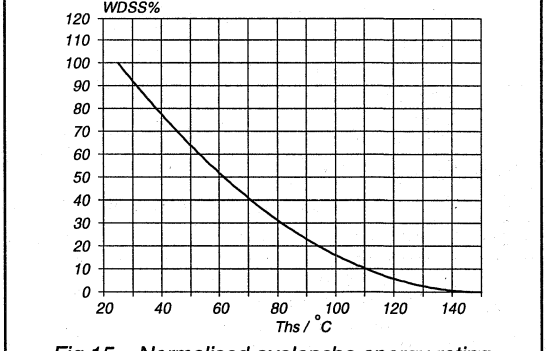


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 41$ A

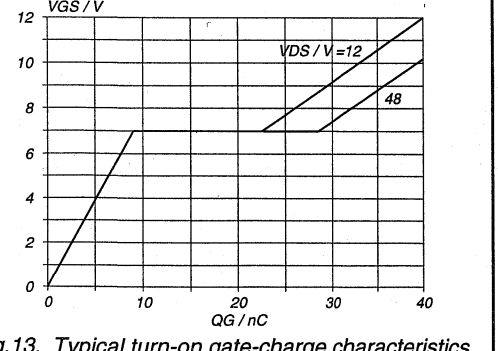


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

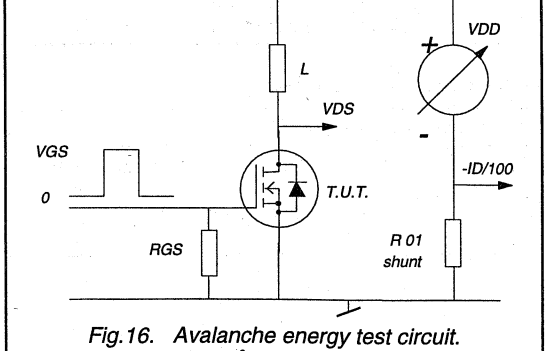


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor | BUK475-60H

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

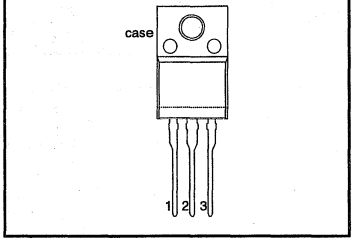
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	24	A
P_{tot}	Total power dissipation	30	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	30	mΩ

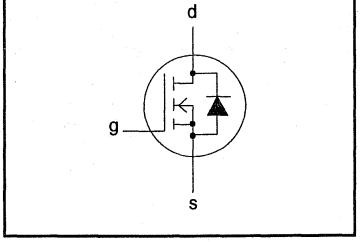
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	24	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	15	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	90	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	24	30	mΩ

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	8	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1000	1600	pF
C_{oss}	Output capacitance		-	470	600	pF
C_{rss}	Feedback capacitance		-	180	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	125	160	ns
t_f	Turn-off fall time		-	100	130	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	24	A
I_{DRM}	Pulsed reverse drain current	-	-	-	90	A
V_{SD}	Diode forward voltage	I_F = 22.5 A ; V_{GS} = 0 V	-	0.9	1.8	V
t_{rr}	Reverse recovery time	I_F = 22.5 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 43 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

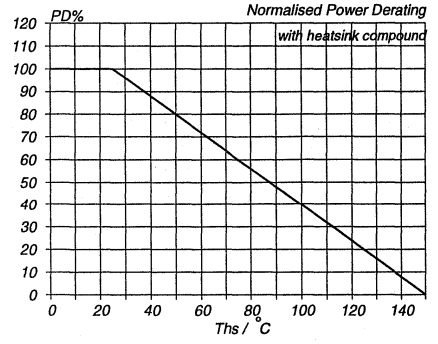


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

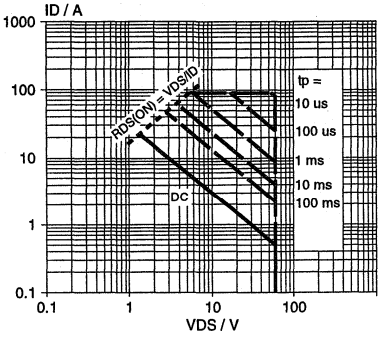


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

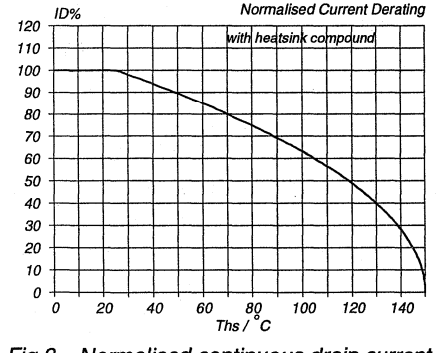


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

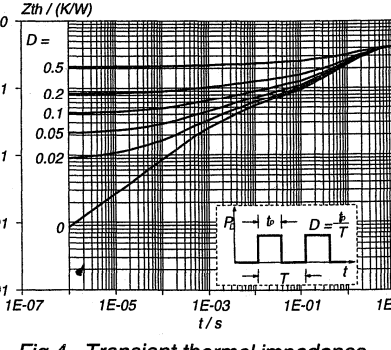


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

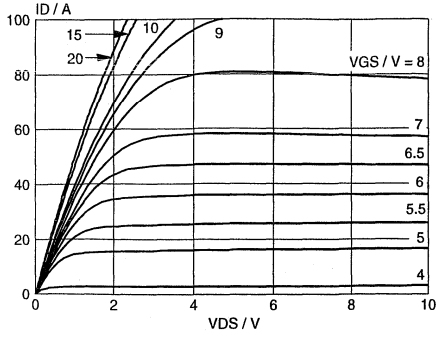


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

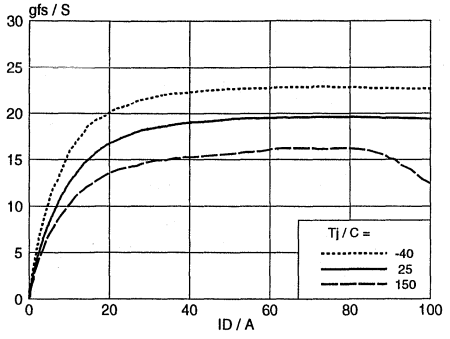


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V

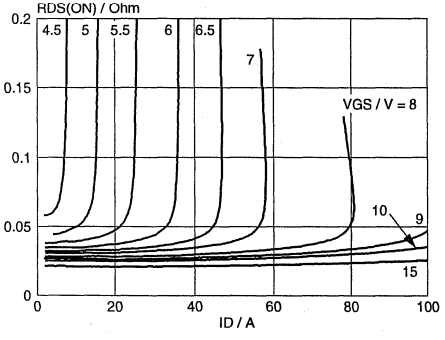


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

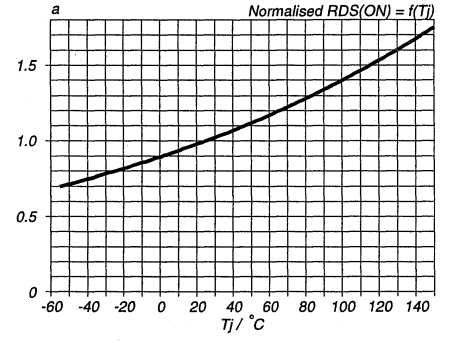


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

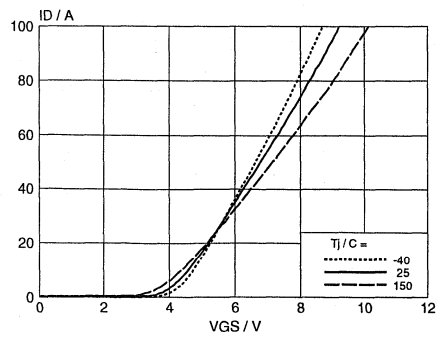


Fig.7. Typical transfer characteristics. $i_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

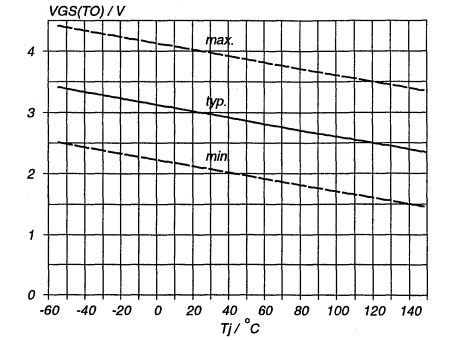


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

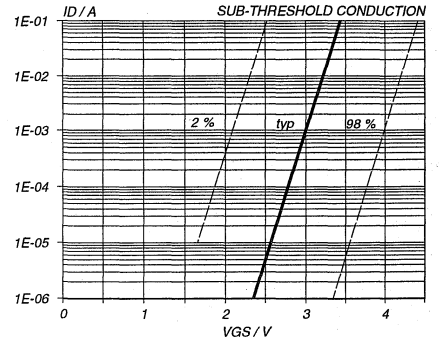


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

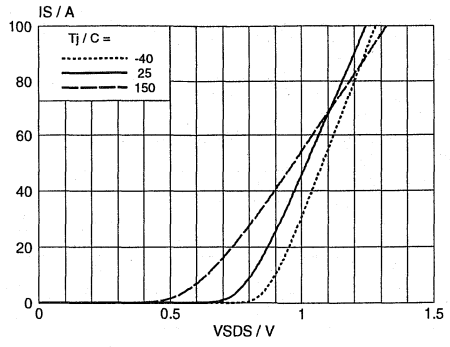


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

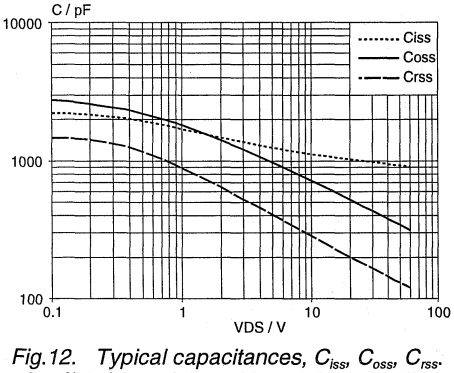


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

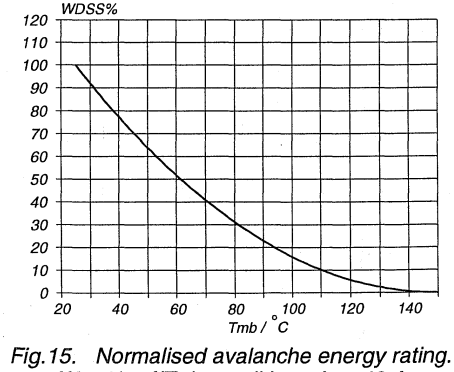


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 43$ A

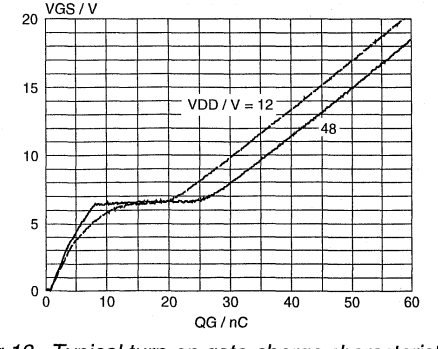


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 43$ A; parameter V_{DS}

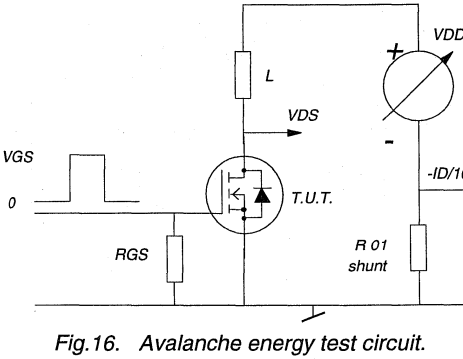


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Isolated version of BUK455-100A/B

BUK475-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

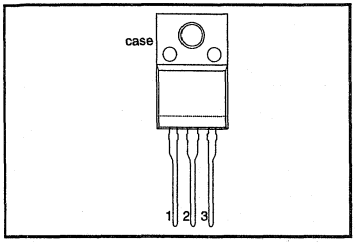
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK475	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	14	12	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	0.1	Ω

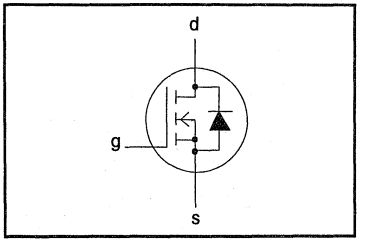
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	14	12	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	8.7	7.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	56	48	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK475-100A** I_D = 13 A **BUK475-100B**	- -	0.07 0.08	0.08 0.1	Ω Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	7.0	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	350	500	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	100	160	ns
t_f	Turn-off fall time		-	50	80	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.70	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 26 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

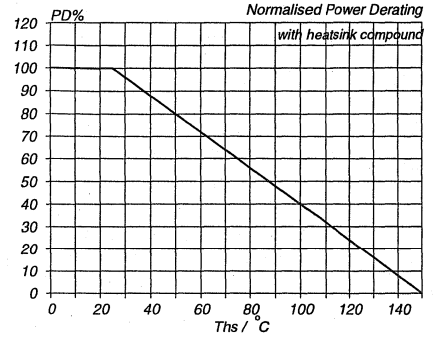


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

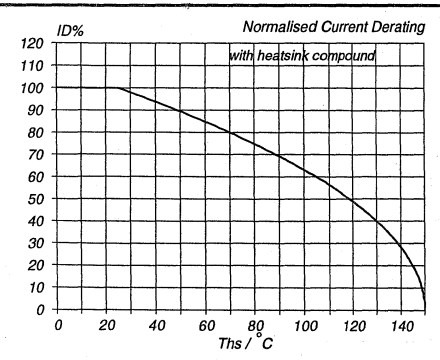


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

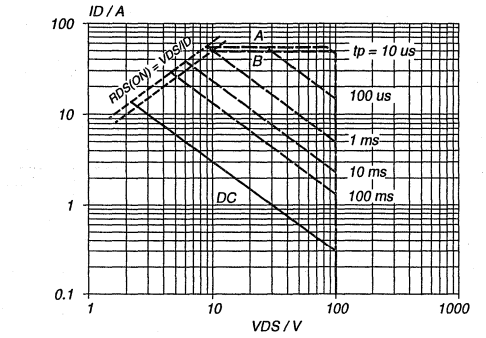


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

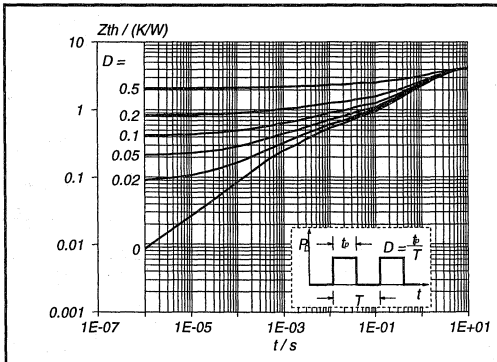


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

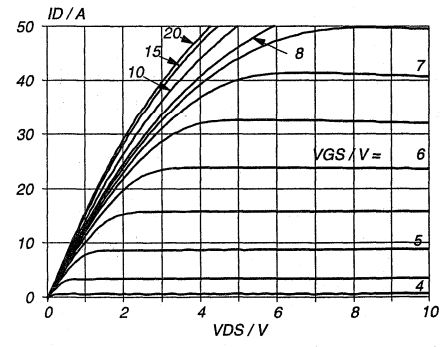


Fig.5. Typical output characteristics, $T_j = 25$ ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

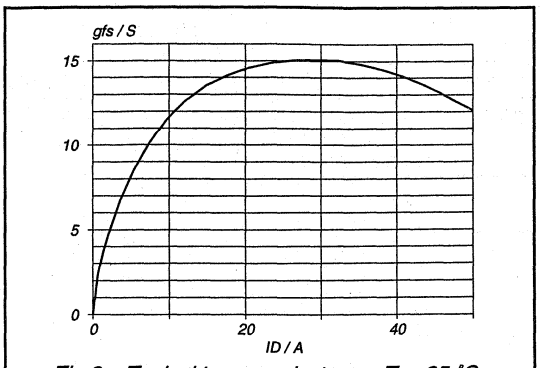


Fig.8. Typical transconductance, $T_j = 25$ ˚C. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

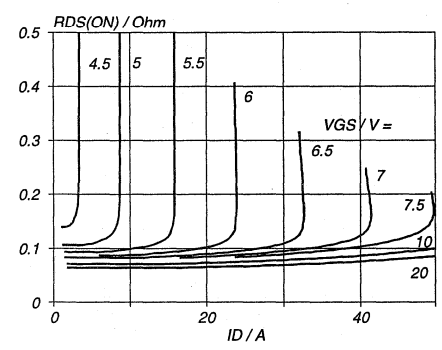


Fig.6. Typical on-state resistance, $T_j = 25$ ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

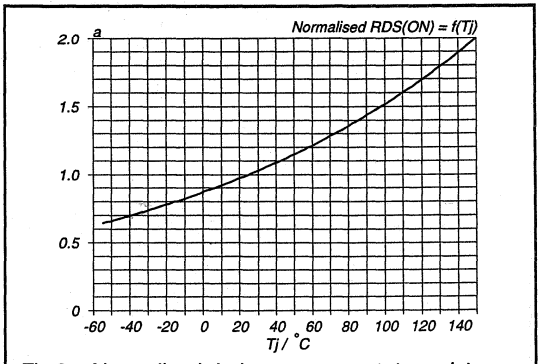


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; $I_D = 13$ A; $V_{GS} = 10$ V

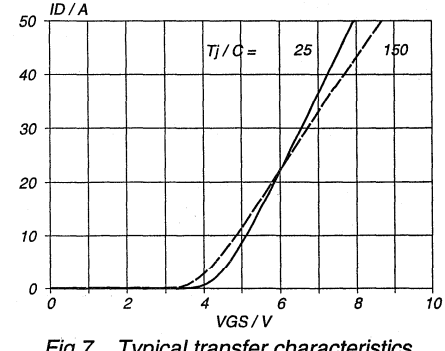


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

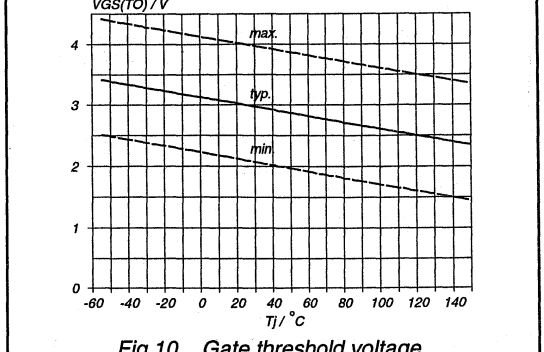


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

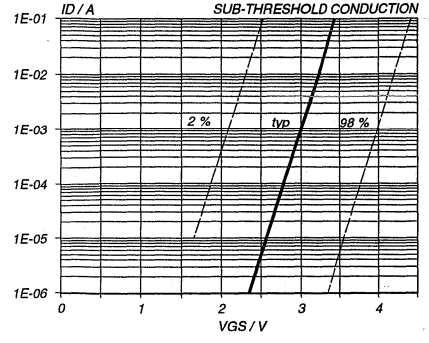


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

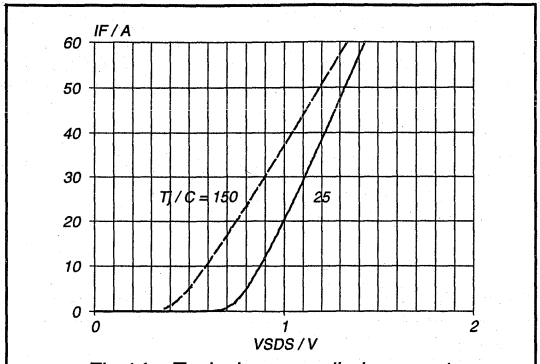


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

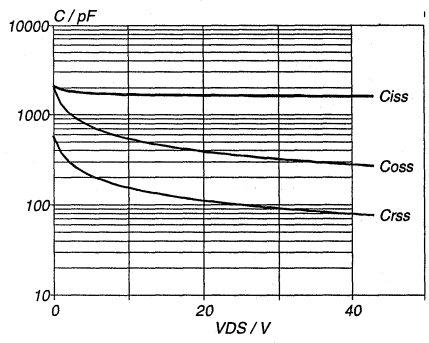


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

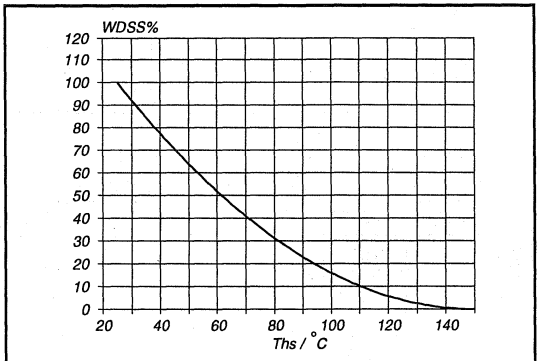


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 26$ A

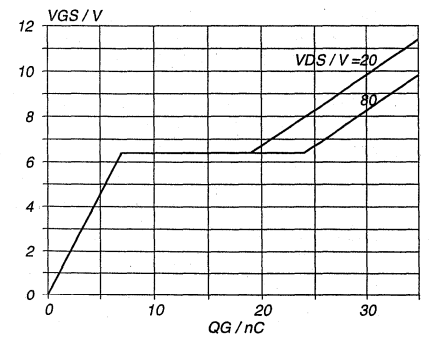


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 26$ A; parameter V_{DS}

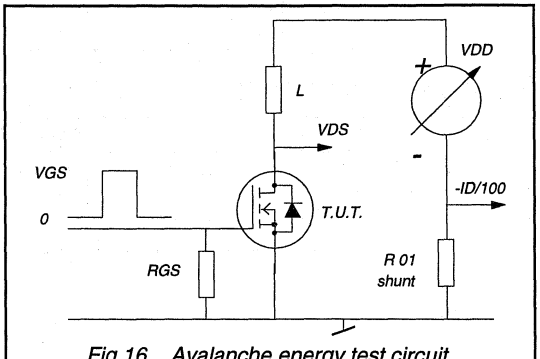


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Isolated version of BUK455-200A/B

BUK475-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

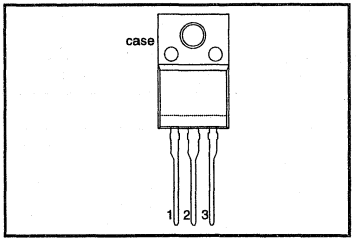
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK475	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	7.6	7	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.23	0.28	Ω

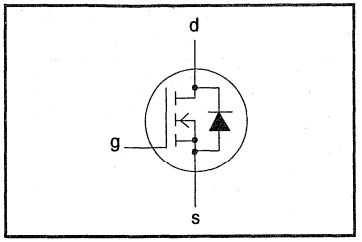
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	30		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	7.6	7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.8	4.4	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	30	28	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; **BUK475-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK475-200B**	-	0.22	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	6	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1400	1750	pF
C_{oss}	Output capacitance		-	190	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	7.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 7.6 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 7.6 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.3	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

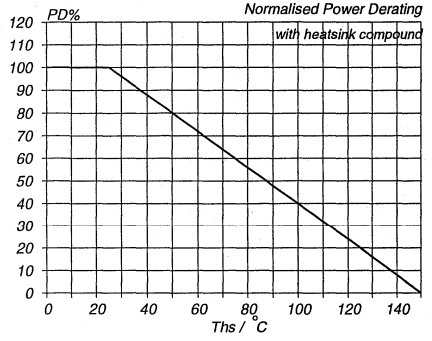


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

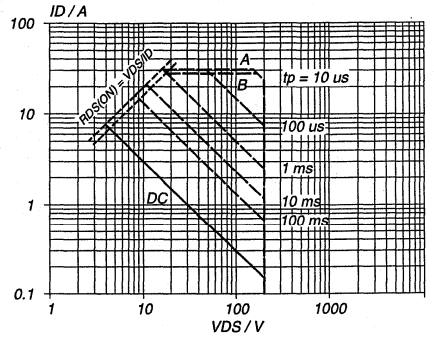


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

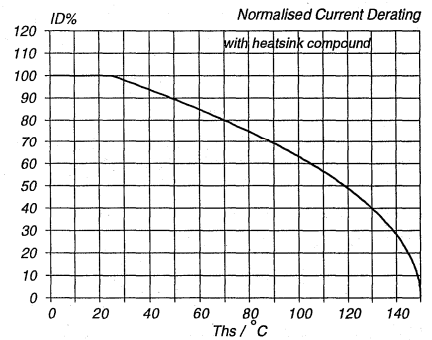


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

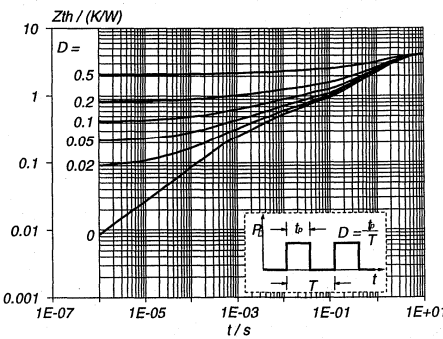


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

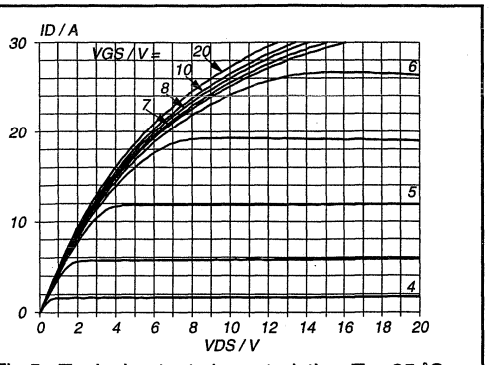


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

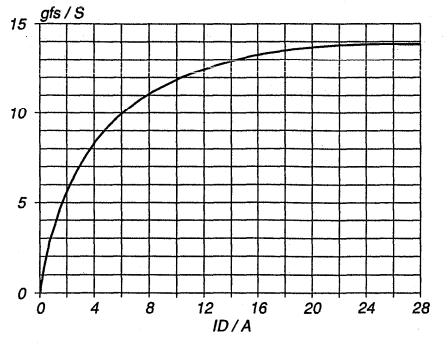


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

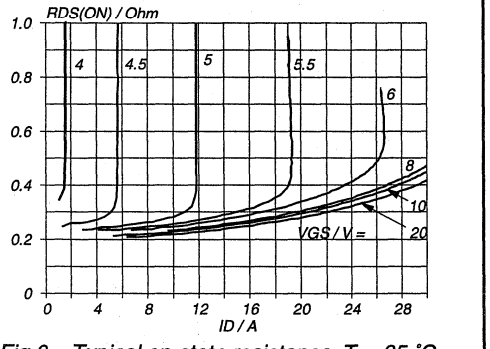


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

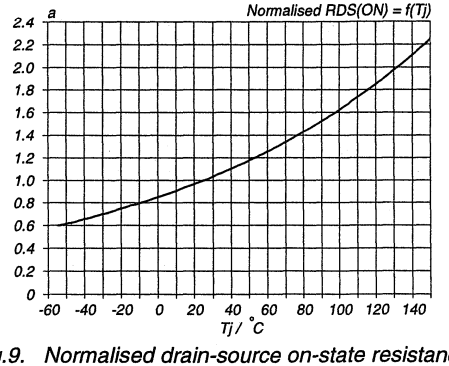


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; $I_D = 7$ A; $V_{GS} = 10$ V

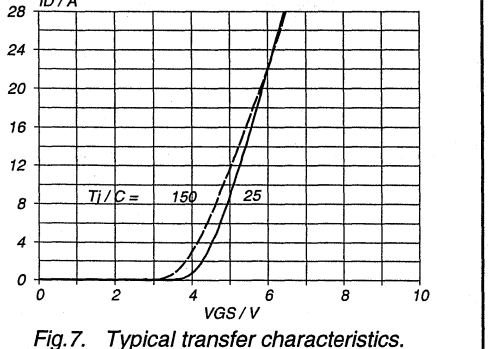


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

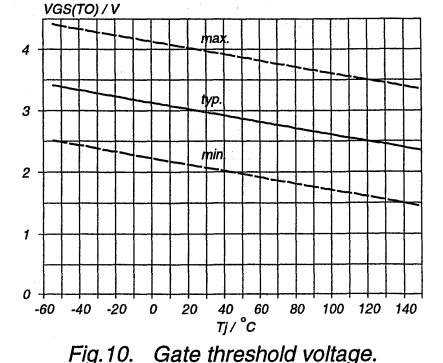


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

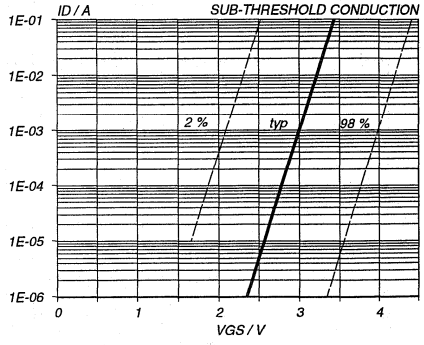


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

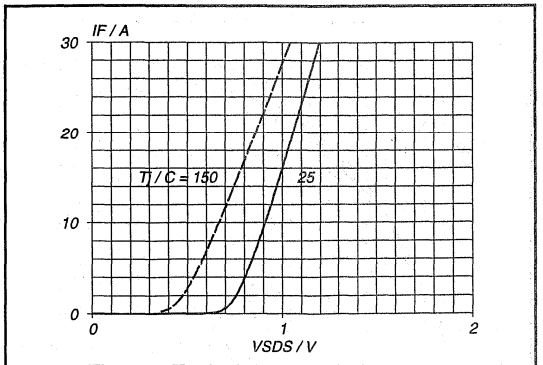


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

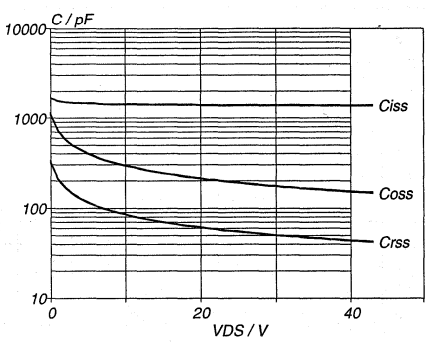


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

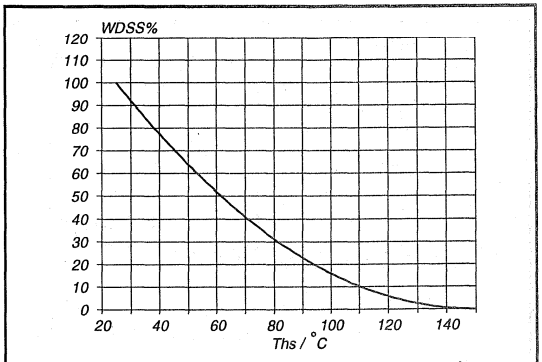


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 14$ A

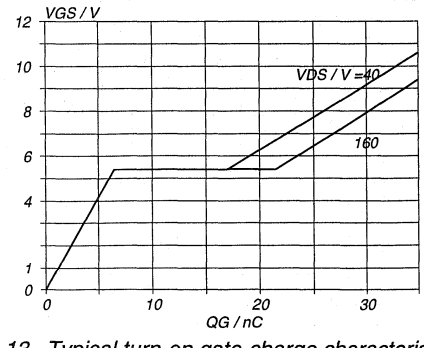


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

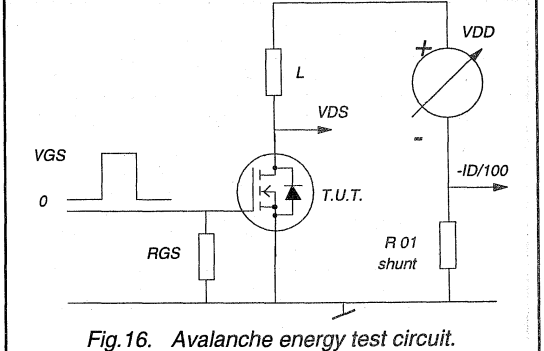


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

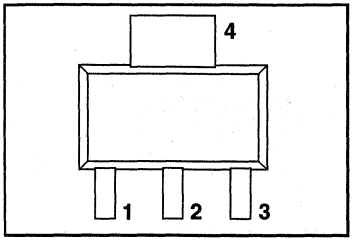
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	1.6	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.35	Ω

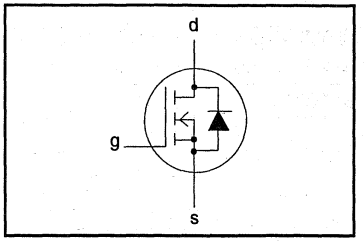
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1.6	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	6.4	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.5	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point[1]	Mounted on any PCB .	-	14	17	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	85	K/W

1 Temperature measured at solder joint on drain tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.6 A	-	0.22	0.35	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.6 A	1.0	1.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	140	240	pF
C_{oss}	Output capacitance		-	60	100	pF
C_{rss}	Feedback capacitance		-	28	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	5	10	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	35	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	10	20	ns
t_f	Turn-off fall time		-	15	25	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	6.4	A
V_{SD}	Diode forward voltage	I_F = 1.6 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1.6 A; -dI_F/dt = 100 A/µs;	-	30	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	60	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non repetitive unclamped inductive turn-off energy	I_D = 1.6 A ; $V_{DD} \leq$ 25 V V_{GS} = 10 V ; R_{GS} = 50 Ω T_{amb} = 25 °C	-	-	10	mJ

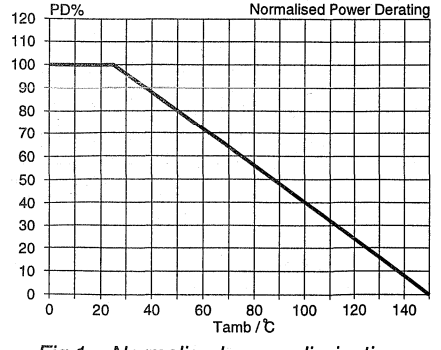


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

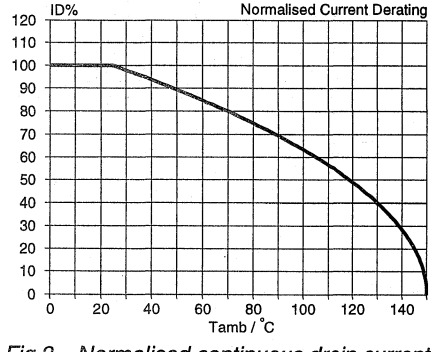


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 10 V

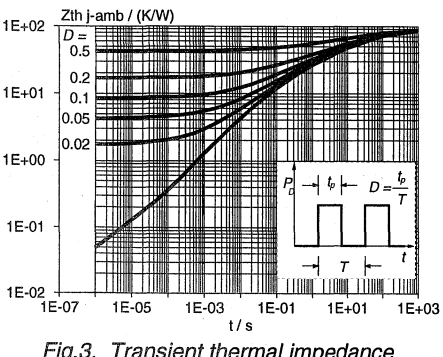


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

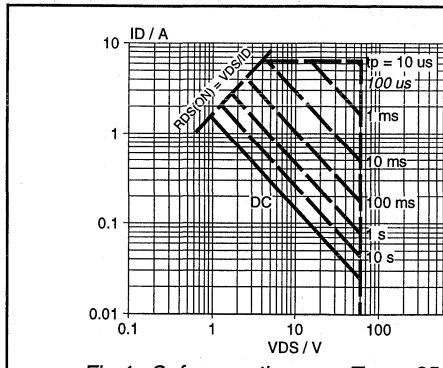


Fig.4. Safe operating area T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

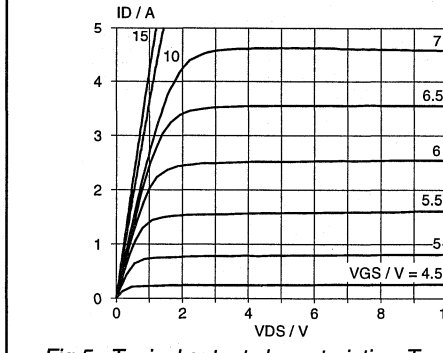


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

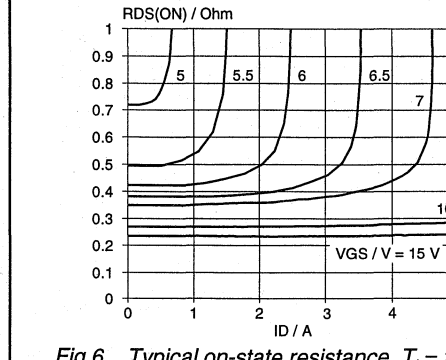


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

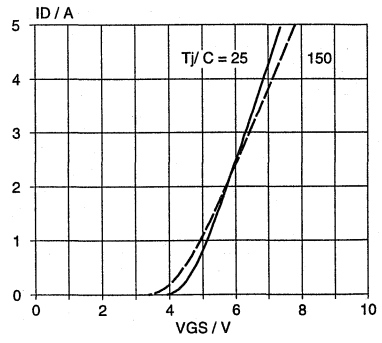


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

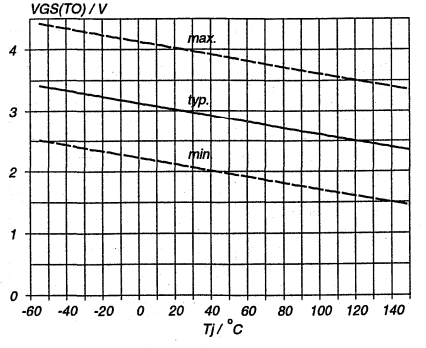


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.1 mA; $V_{DS} = V_{GS}$

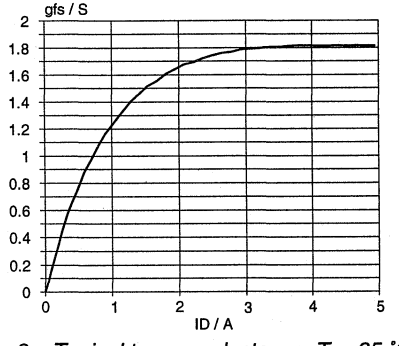


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

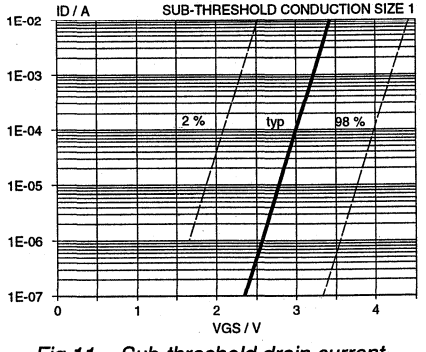


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

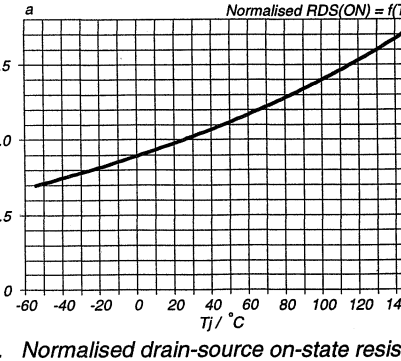


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.6 A; V_{GS} = 10 V

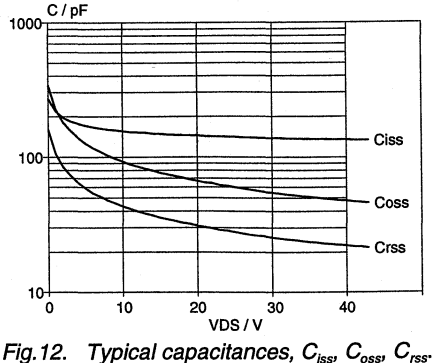


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

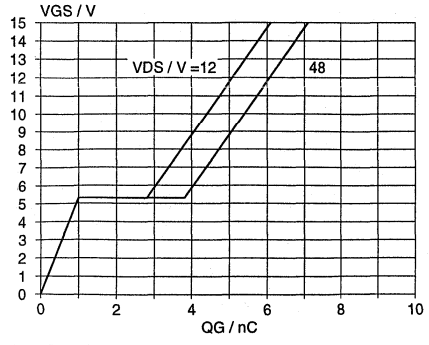


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 1.6$ A; parameter V_{DS}

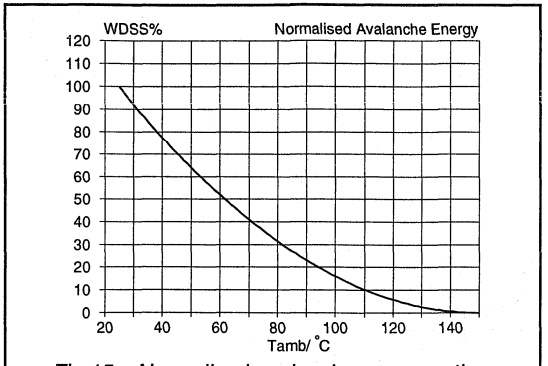


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1.6$ A

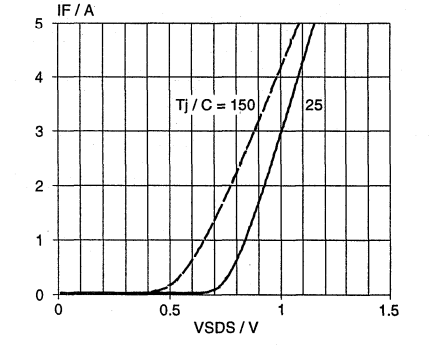


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

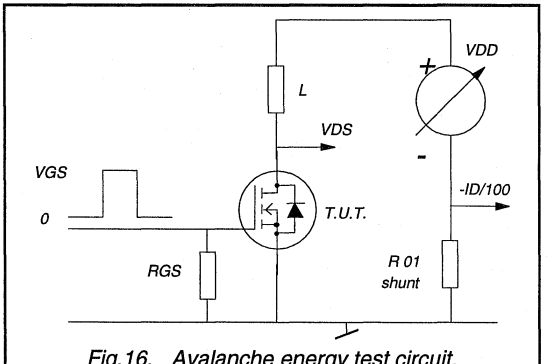


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — BUK481-100A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

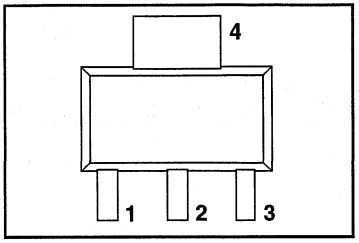
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	1.0	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.80	Ω

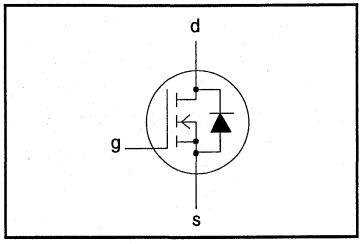
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	0.6	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	4	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.5	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB e.g. Fig.18	-	50	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	85	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1 A	-	0.48	0.80	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1 A	0.8	1.1	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	140	240	pF
C_{oss}	Output capacitance		-	40	60	pF
C_{rss}	Feedback capacitance		-	16	25	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	5	10	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	35	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	10	20	ns
t_f	Turn-off fall time		-	10	20	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1	A
I_{DRM}	Pulsed reverse drain current	-	-	-	4	A
V_{SD}	Diode forward voltage	I_F = 1 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	100	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	10	mJ

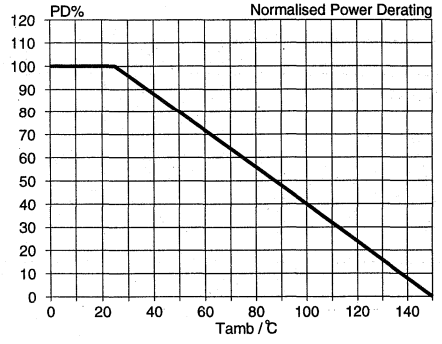


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{amb})

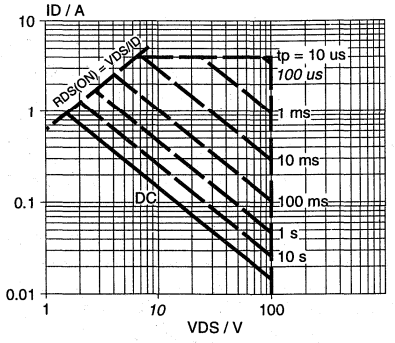


Fig.4. Safe operating area T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

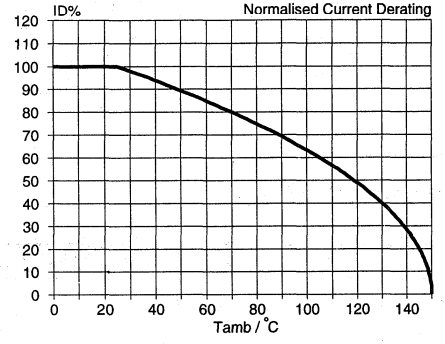


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{amb}); conditions: V_{GS} ≥ 10 V

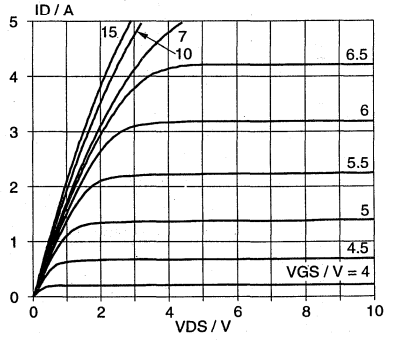


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

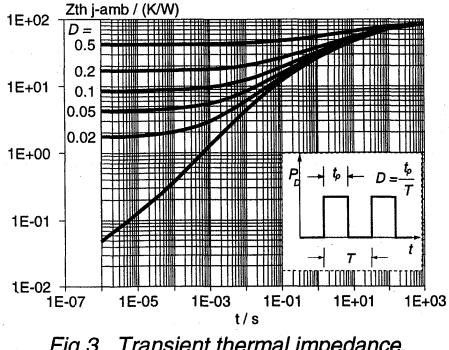


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

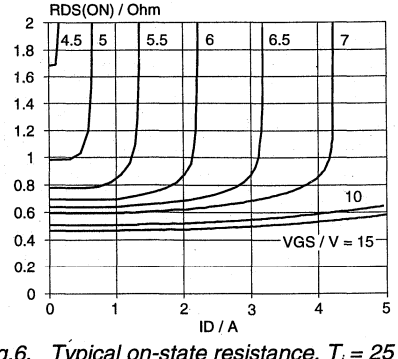


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

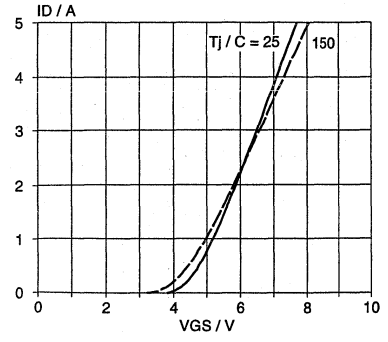


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

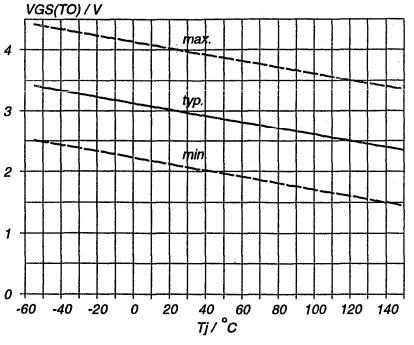


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.1$ mA; $V_{DS} = V_{GS}$

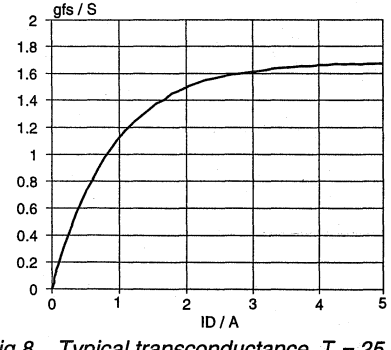


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

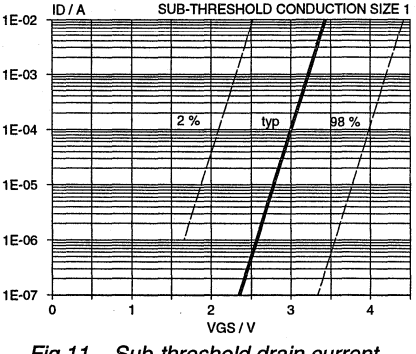


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

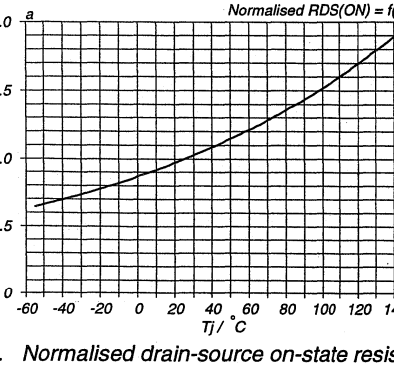


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 1$ A; $V_{GS} = 10$ V

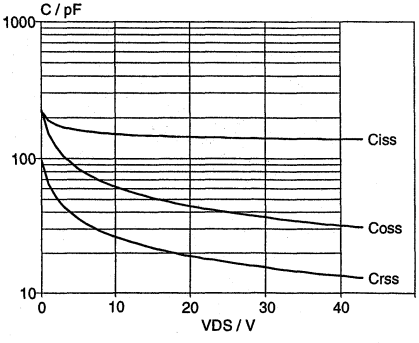


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

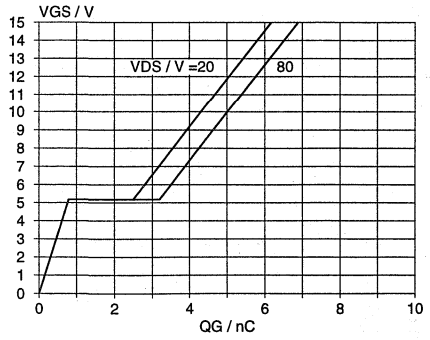


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 1$ A; parameter V_{DS}

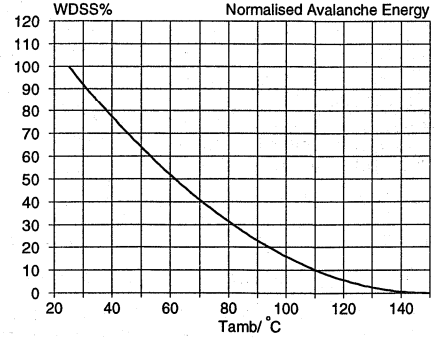


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1$ A

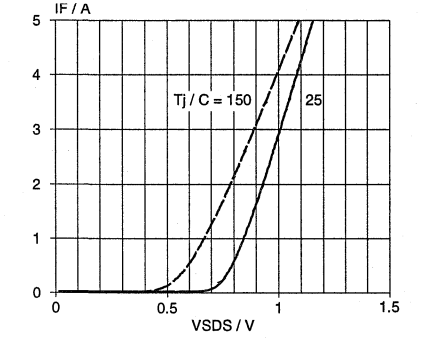


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

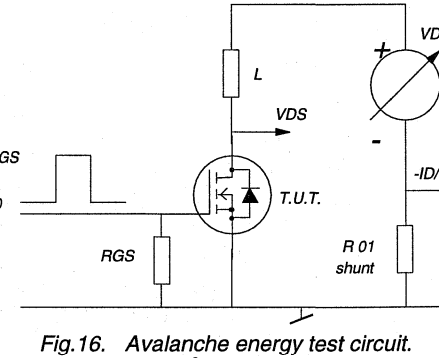


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — BUK482-60A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

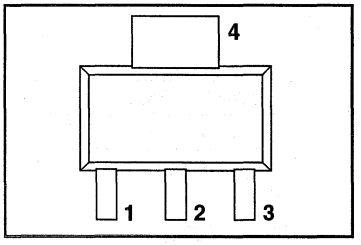
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	2.7	A
P_{tot}	Total power dissipation	1.7	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.13	Ω

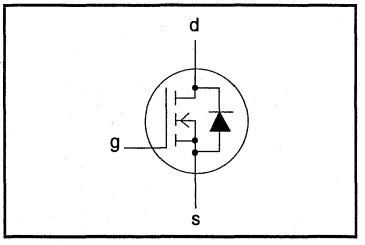
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	2.7	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1.7	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	11	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.7	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB e.g. Fig.18	-	40	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	75	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.7 A	-	0.11	0.13	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2.7 A	2	3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	500	pF
C_{oss}	Output capacitance		-	130	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	8	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	45	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	30	45	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	2.7	A
I_{DRM}	Pulsed reverse drain current	-	-	-	11	A
V_{SD}	Diode forward voltage	I_F = 2.7 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 2.7 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	70	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.7 A; V_{DD} ≤ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	30	mJ

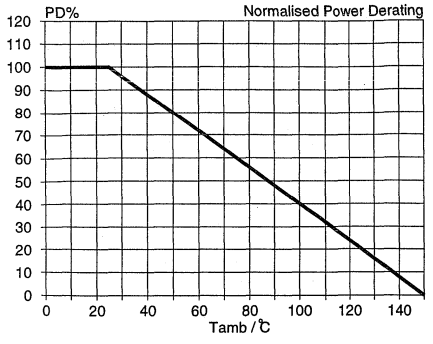


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

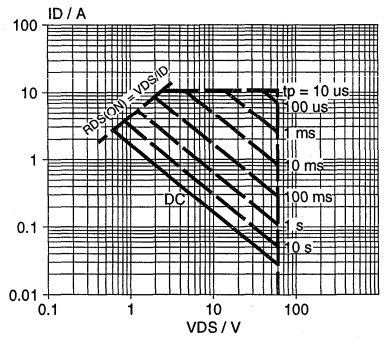


Fig.4. Safe operating area T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

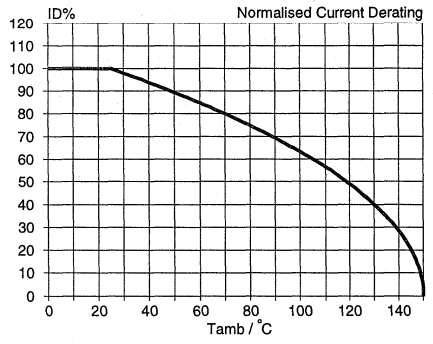


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 10 V

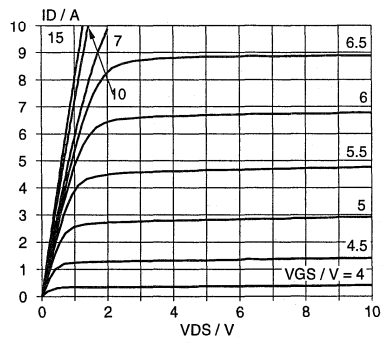


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

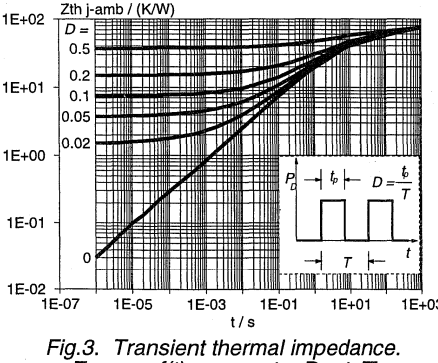


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

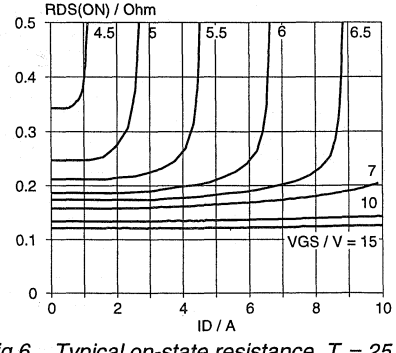


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

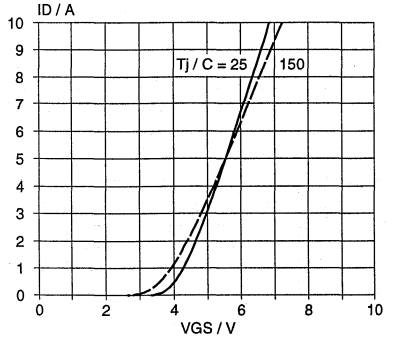


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

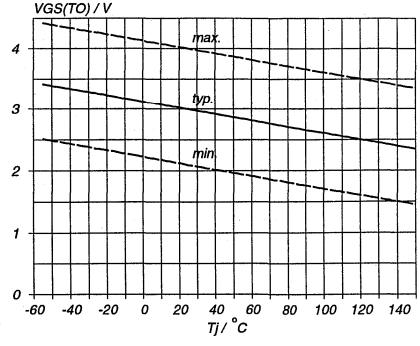


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

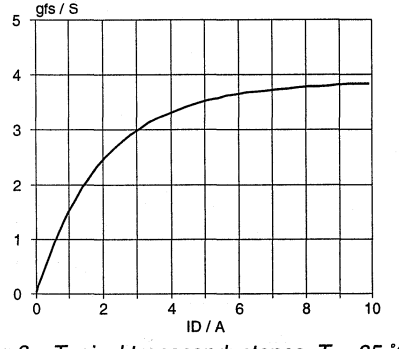


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

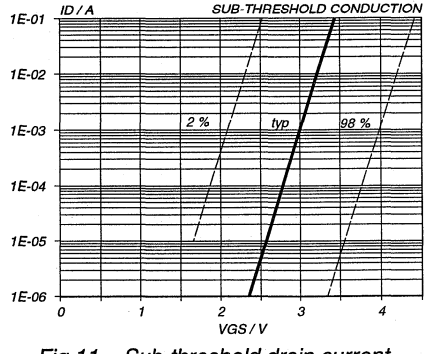


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

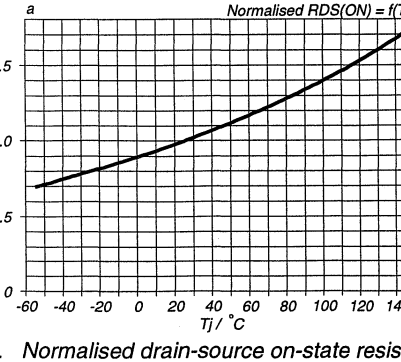


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.7 A; V_{GS} = 10 V

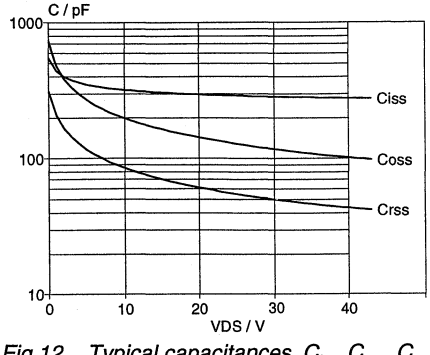


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

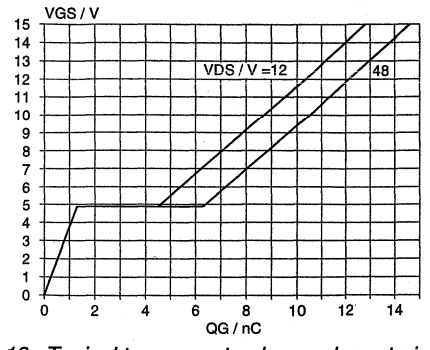


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2.7$ A; parameter V_{DS}

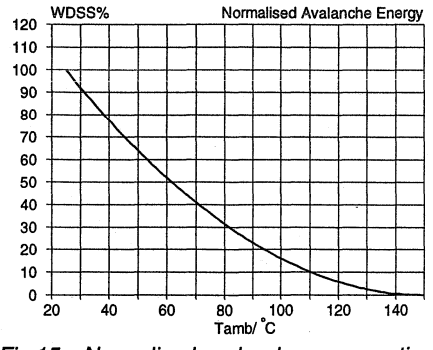


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 2.7$ A

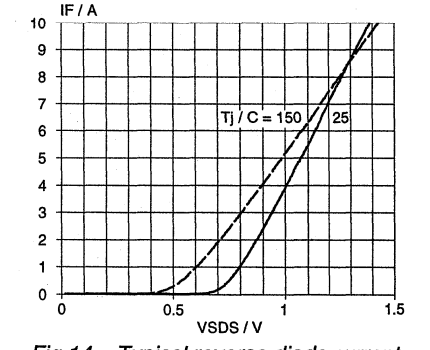


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

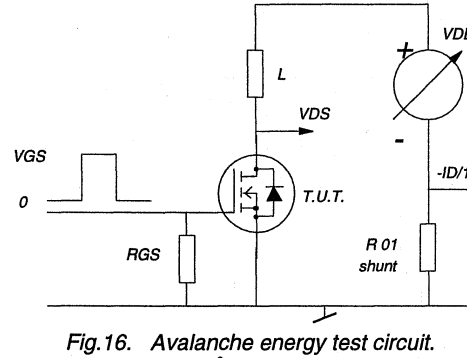


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

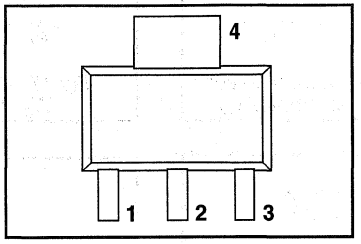
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	1.8	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.28	Ω

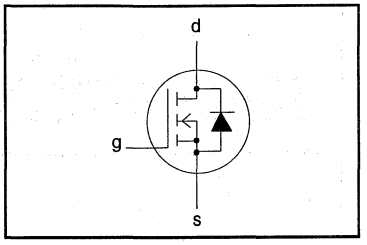
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1.8	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	7.2	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.8	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB e.g. Fig.18	-	40	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	70	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.8 A	-	0.21	0.28	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.8 A	1.5	2.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.8	A
I_{DRM}	Pulsed reverse drain current	-	-	-	7.2	A
V_{SD}	Diode forward voltage	I_F = 1.8 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1.8 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.8 A; V_{DD} ≤ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	40	mJ

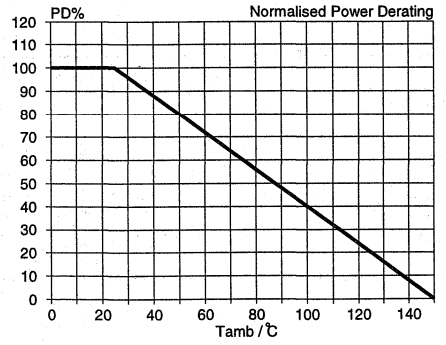


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

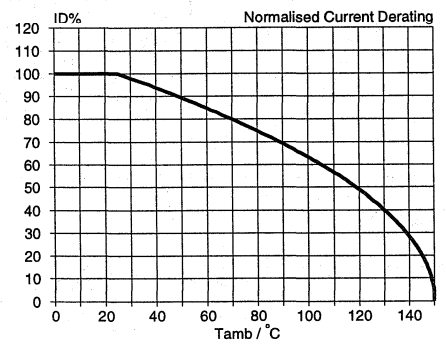


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 10 V

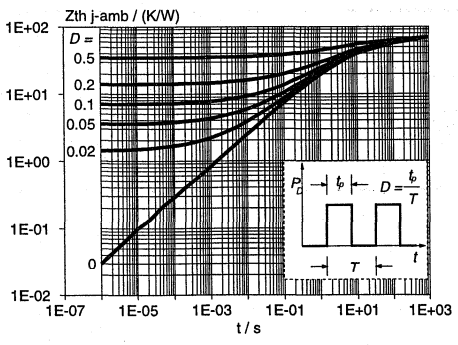


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

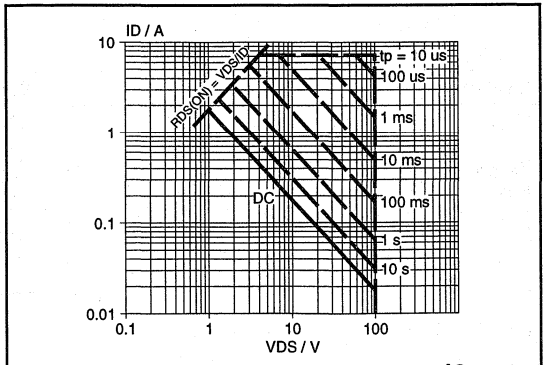


Fig.4. Safe operating area. T_{amb} = 25 ˚C.
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

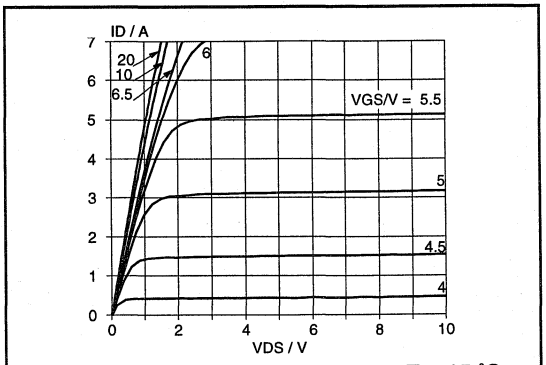


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

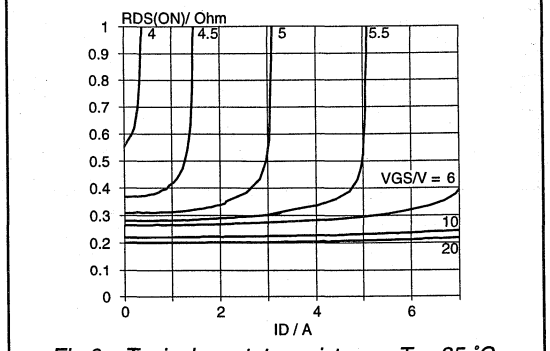


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

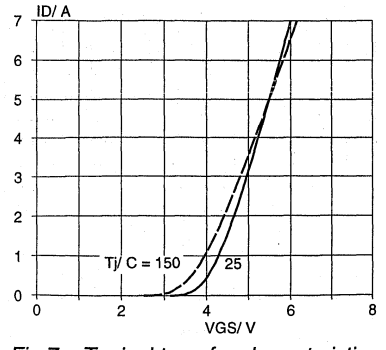


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

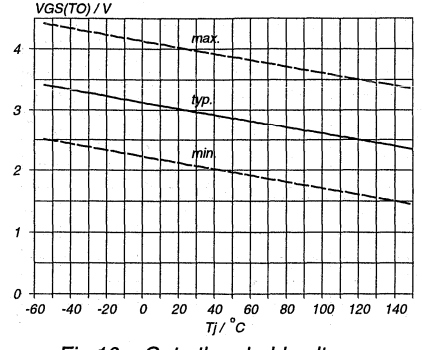


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

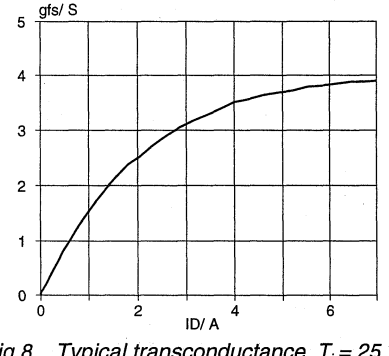


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

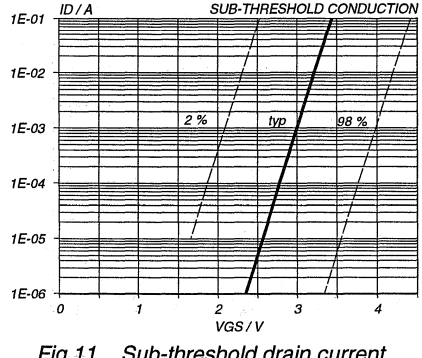


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

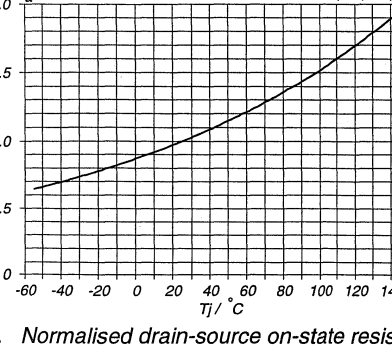


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.8 A; V_{GS} = 10 V

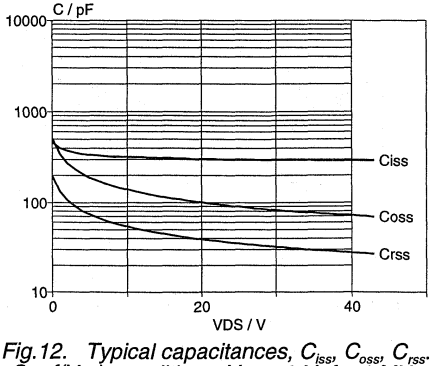


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

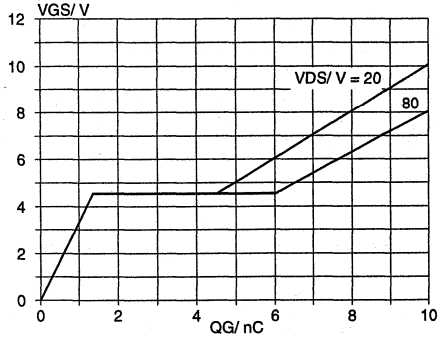


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 1.8$ A; parameter V_{DS}

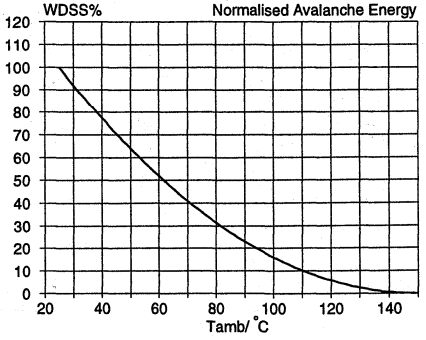


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1.8$ A

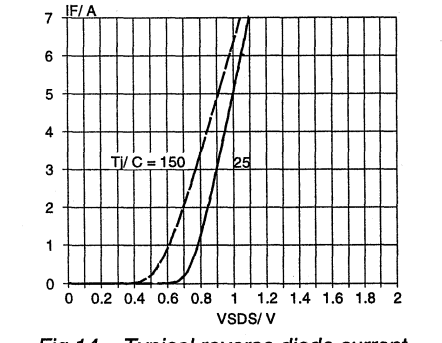


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

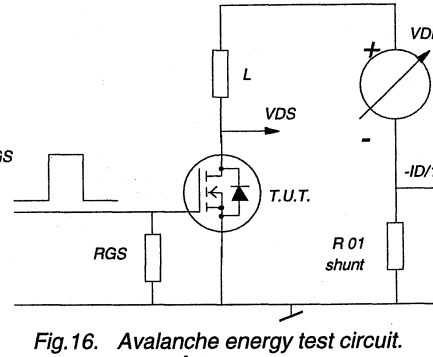


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance. Intended for use in Switched Mode Power Supplies (SMPS) and general purpose switching applications.

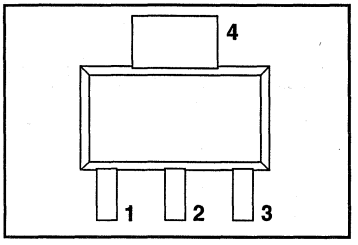
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	2.0	A
P_{tot}	Total power dissipation	8.3	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.9	Ω

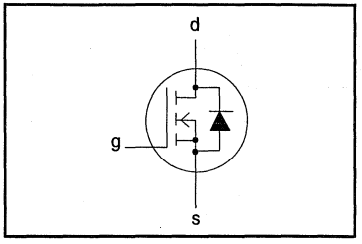
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{sp} = 25 °C	-	2.0	A
		T_{sp} = 100 °C	-	1.3	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 °C	-	8.0	A
I_{DR}	Source-drain diode current (DC)	T_{sp} = 25 °C	-	2.0	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{sp} = 25 °C	-	8.0	A
P_{tot}	Total power dissipation	T_{sp} = 25 °C	-	8.3	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction Temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	50	mJ
		T_j = 100°C prior to surge	-	8	mJ

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:17	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	0.1	10	µA
		V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2 A	-	0.53	0.9	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2 A ;V_{GS} = 0 V	-	0.87	1.0	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2 A	0.5	2.6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	305	400	pF
C_{oss}	Output capacitance		-	60	100	pF
C_{rss}	Feedback capacitance		-	24	50	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 2 A; V_{DS} = 160 V	-	13	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	5	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.75 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	45	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	40	ns
t_f	Turn-off fall time		-	20	30	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	88	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	370	-	nC

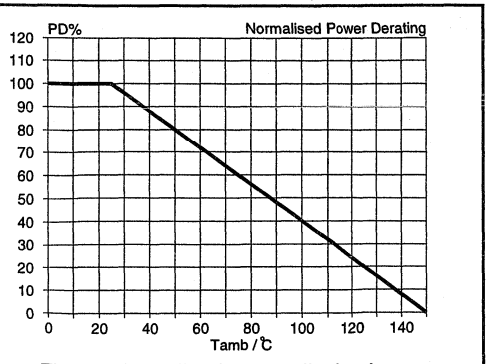


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

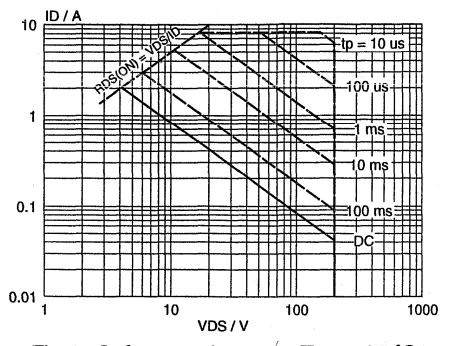


Fig.4. Safe operating area. T_{amb} = 25 °C.
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

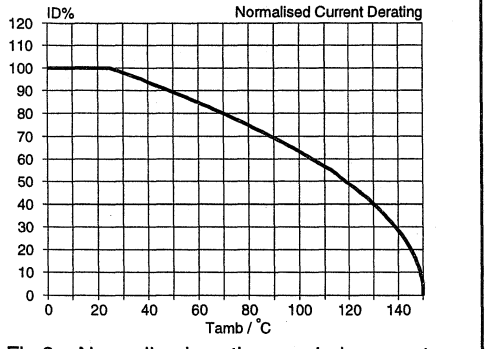


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 10 V

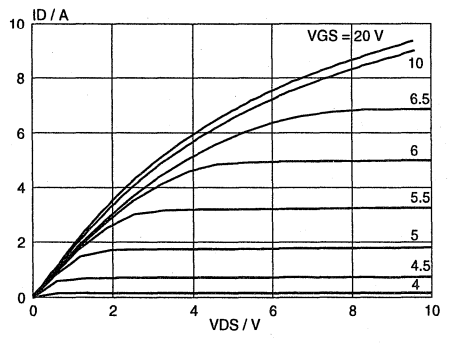


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

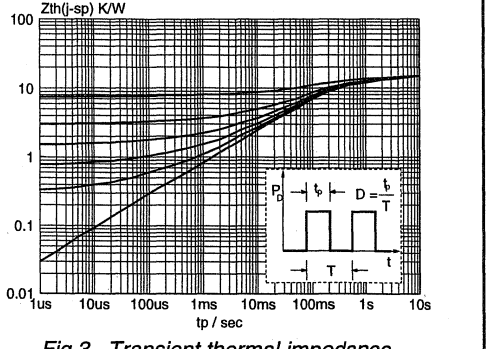


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

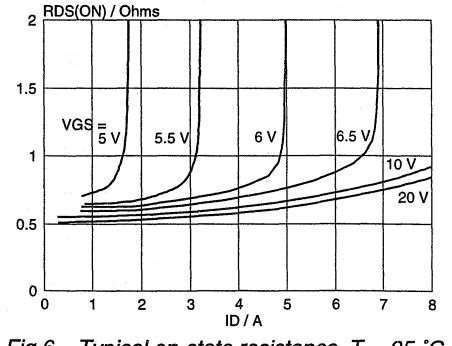


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

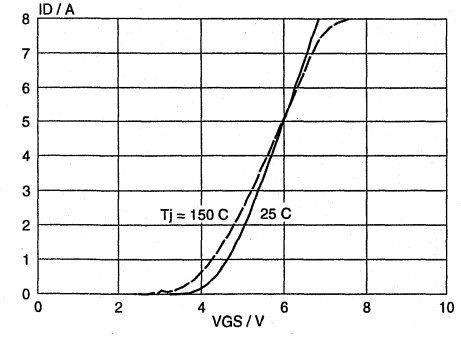


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

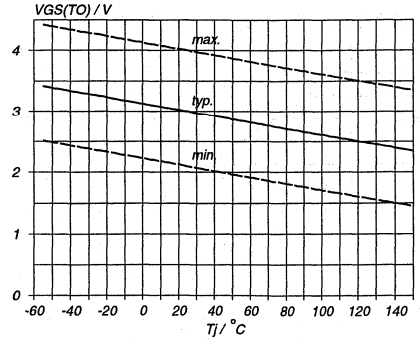


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

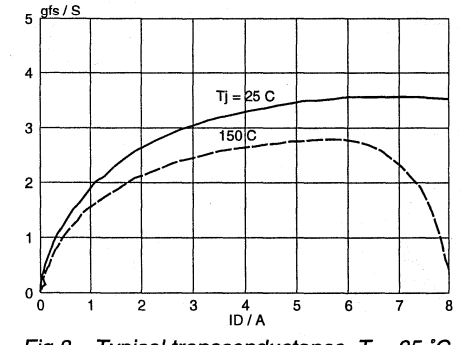


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

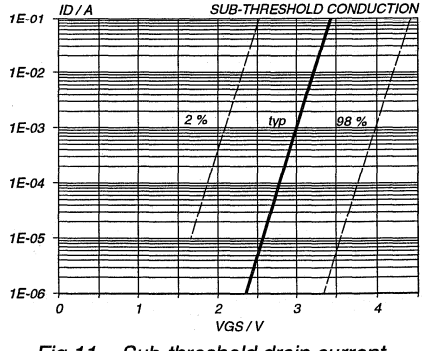


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

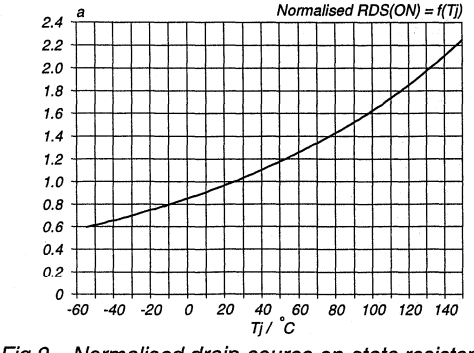


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2 A; V_{GS} = 10 V

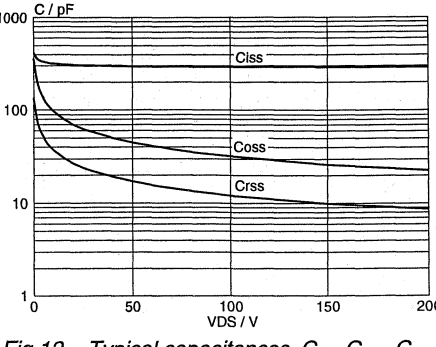


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

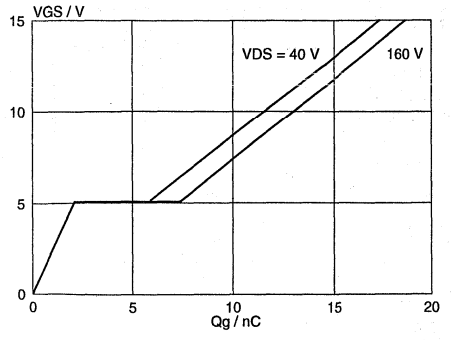


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2$ A; parameter V_{DS}

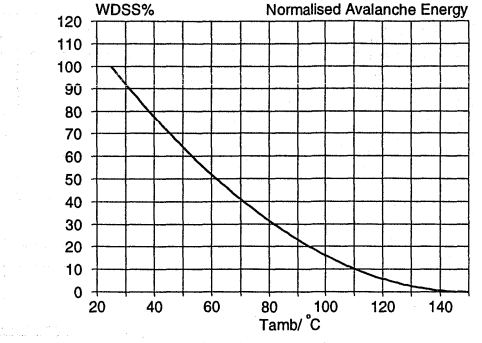


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 2$ A

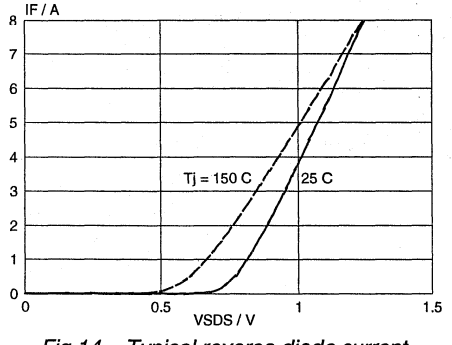


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

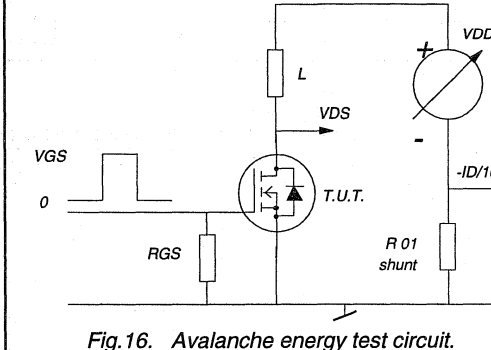


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

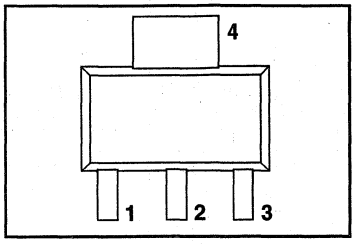
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	3.2	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.10	Ω

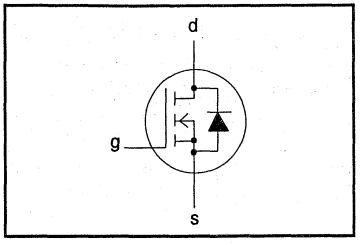
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	3.2	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	2.0	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	13	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.8	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point[1]	Mounted on any PCB	-	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of fig.18	-	-	70	K/W

1 Temperature measured at solder joint on drain tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	70	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.2 A	-	0.07	0.10	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.2 A	-	6.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	120	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	55	80	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	3.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	13	A
V_{SD}	Diode forward voltage	I_F = 3.2 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 3.2 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.2 A; V_{DD} ≤ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	45	mJ

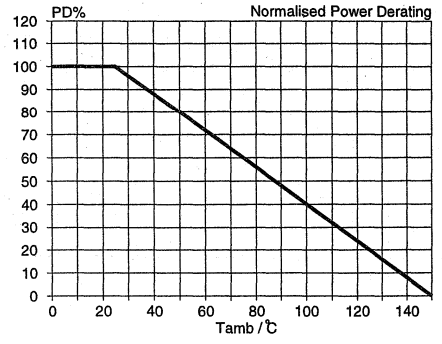


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{amb})

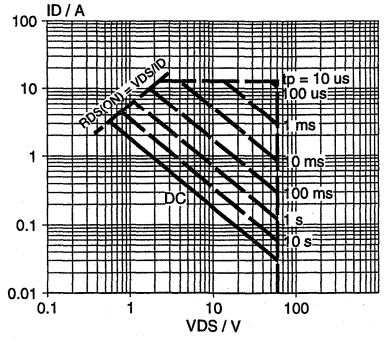


Fig.4. Safe operating area T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

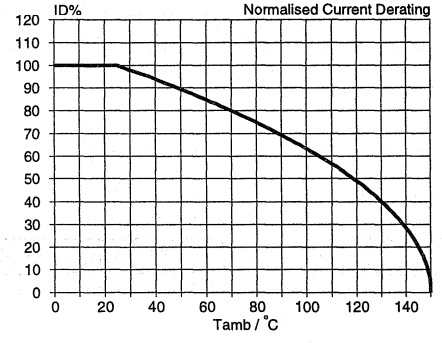


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{amb}); conditions: V_{GS} ≥ 10 V

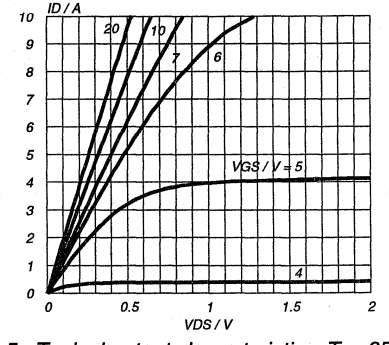


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

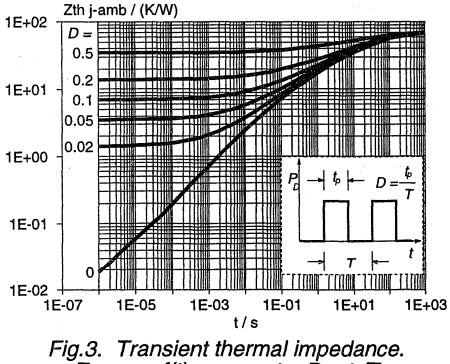


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

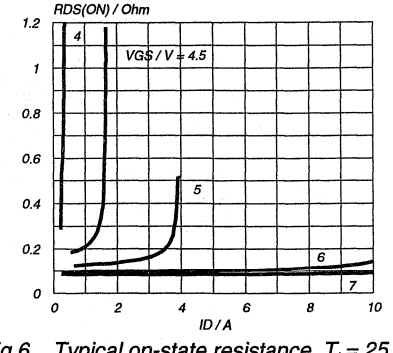


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

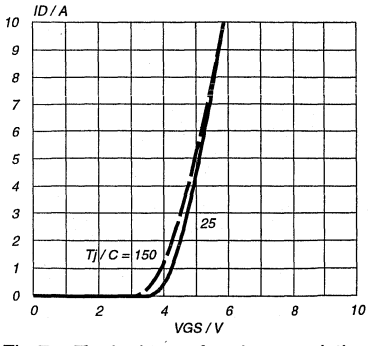


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

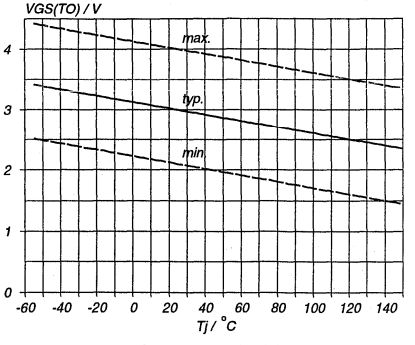


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

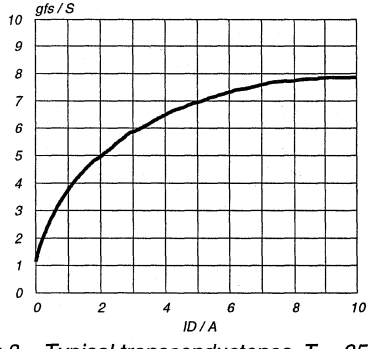


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

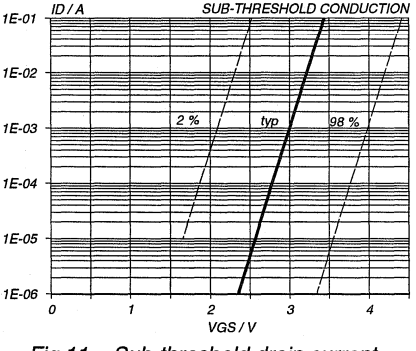


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

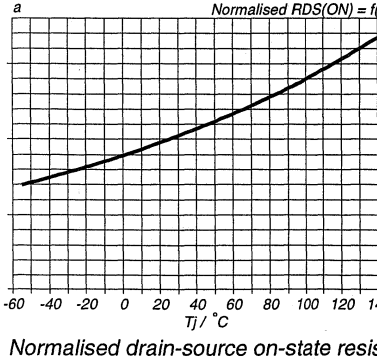


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.2 A; V_{GS} = 10 V

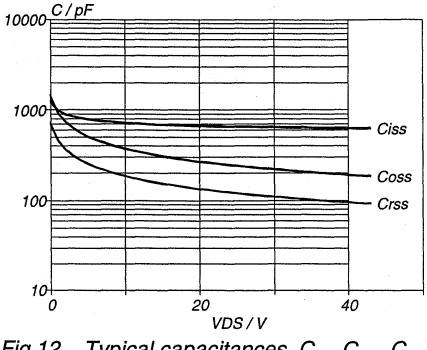


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

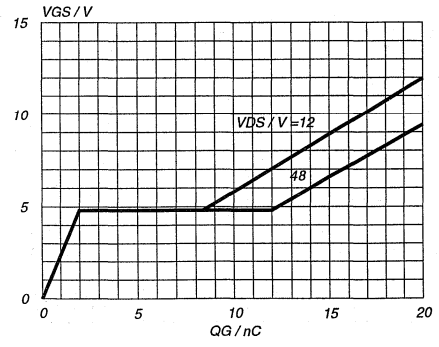


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3.2$ A; parameter V_{DS}

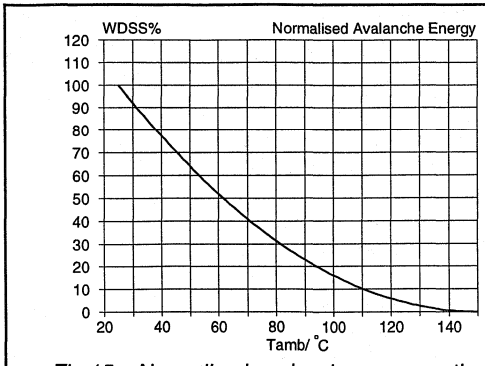


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 3.2$ A

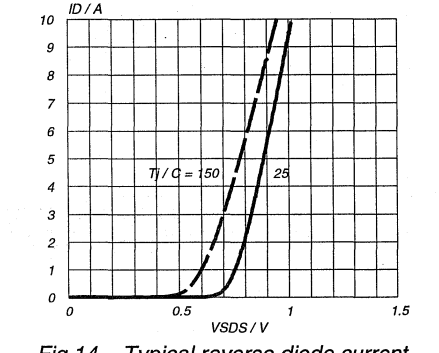


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

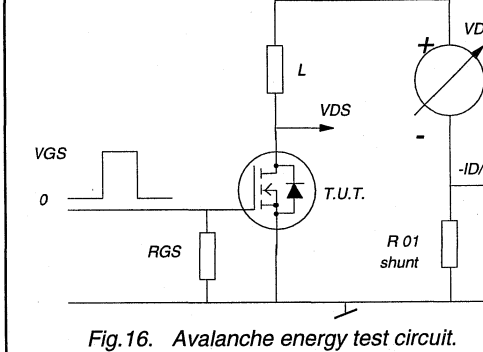


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK542-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

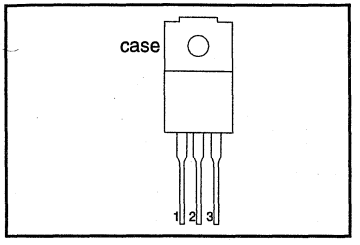
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
		BUK542	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	9.2	8.4	A
P_{tot}	Total power dissipation	22	22	W
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.15	0.18	Ω

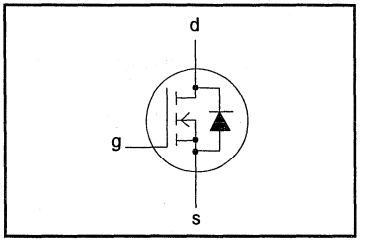
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-60A	-60B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	9.2	8.4	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	5.8	5.3	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	37	33	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	22		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.68	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK542-60A**	-	0.12	0.15	Ω
		I_D = 8.5 A **BUK542-60B**	-	0.15	0.18	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	5	6.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	65	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	60	80	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	45	70	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	37	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

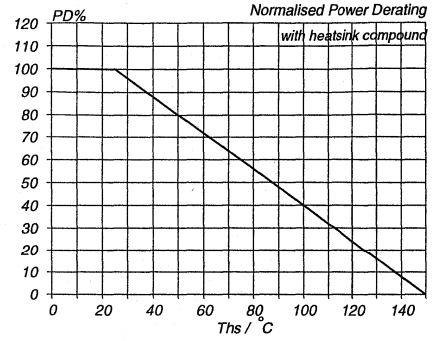


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

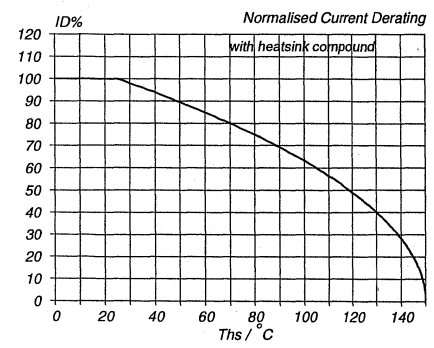


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

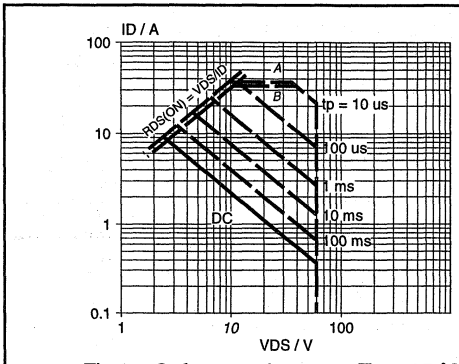


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

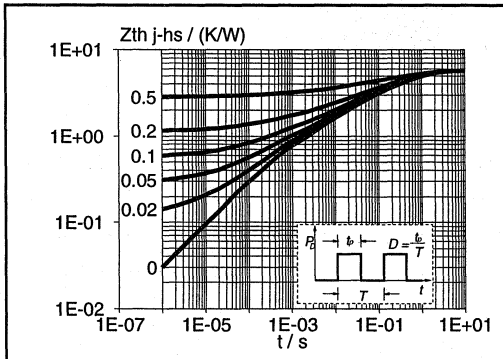


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

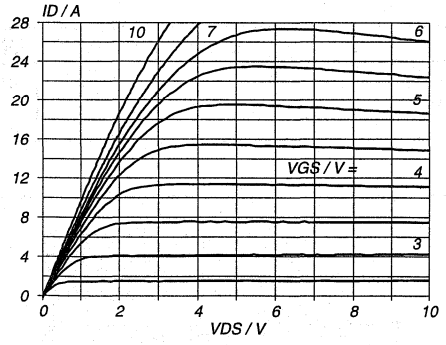


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

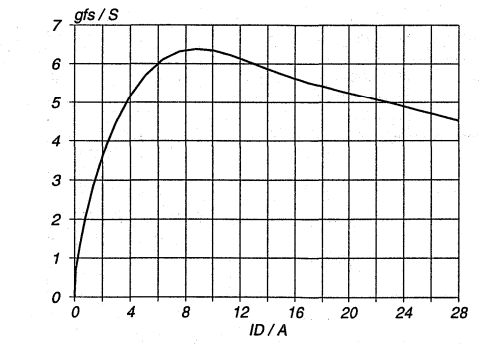


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

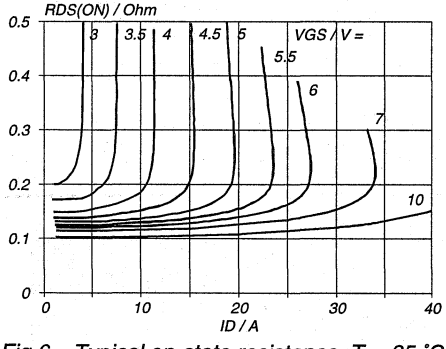


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

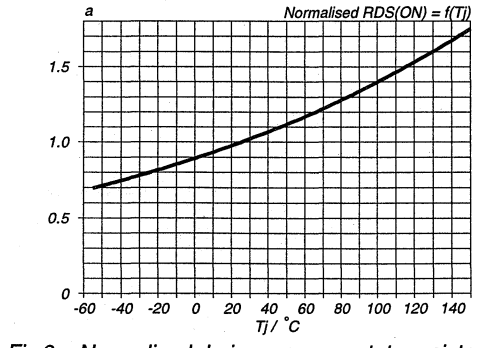


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 8.5 A; V_{GS} = 5 V

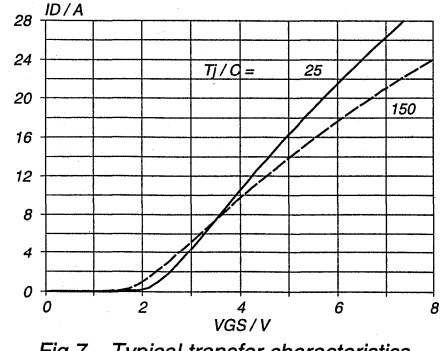


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

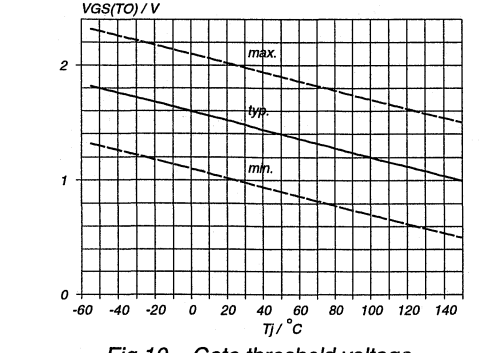


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

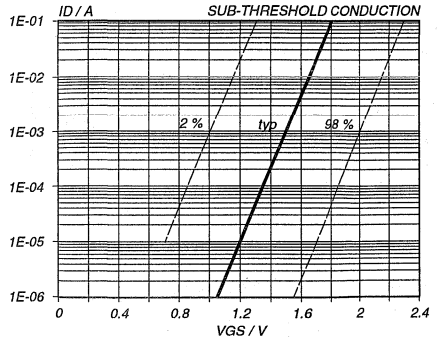


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

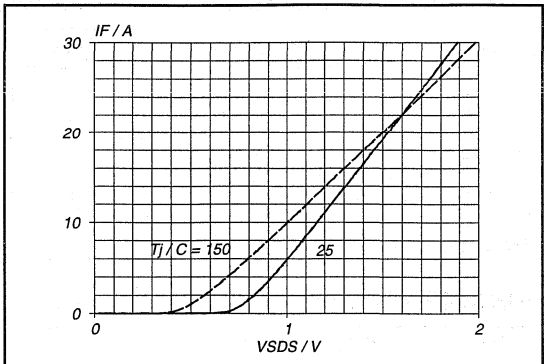


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

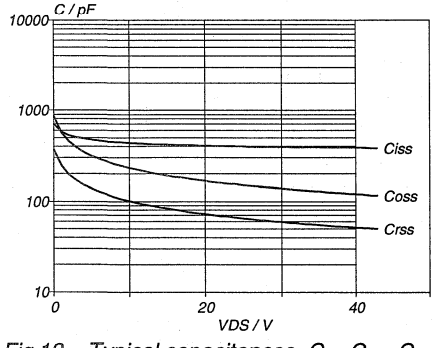


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

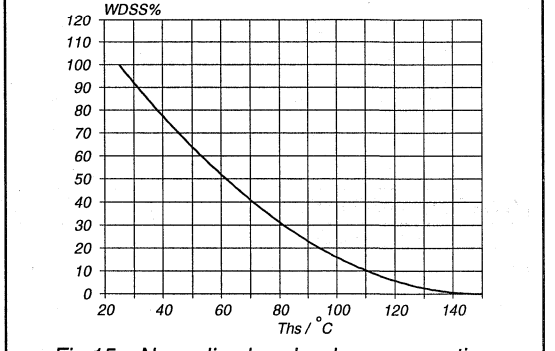


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 14$ A

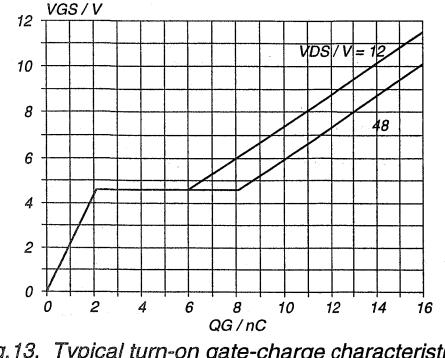


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

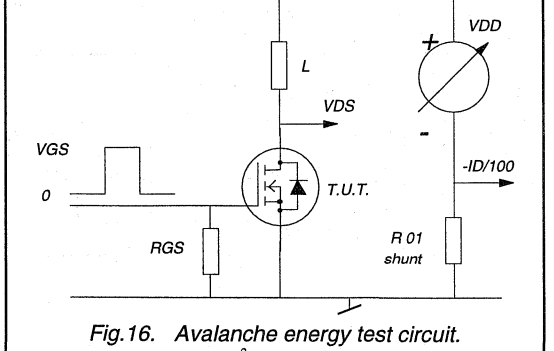


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK542-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

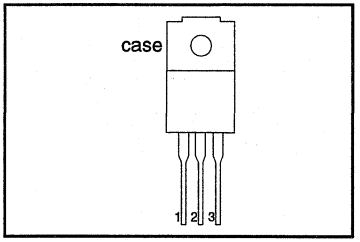
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
		BUK542	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	6.3	5.6	A
P_{tot}	Total power dissipation	22	22	W
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.28	0.35	Ω

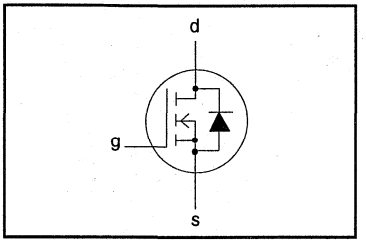
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	6.3	5.6	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4	3.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	25	22	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	22		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.68	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK542-100A** I_D = 5.5 A **BUK542-100B**	- -	0.25 0.3	0.28 0.35	Ω Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	4.5	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	6.3	A
I_{DRM}	Pulsed reverse drain current	-	-	-	25	A
V_{SD}	Diode forward voltage	I_F = 6.3 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 6.3 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

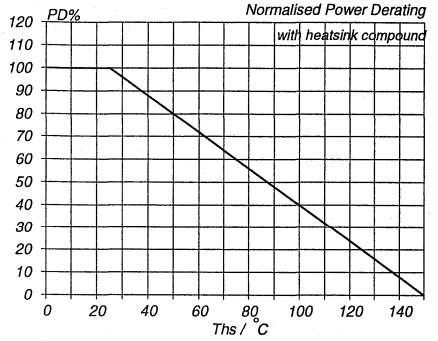


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

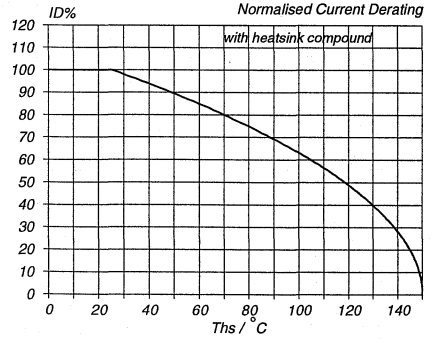


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

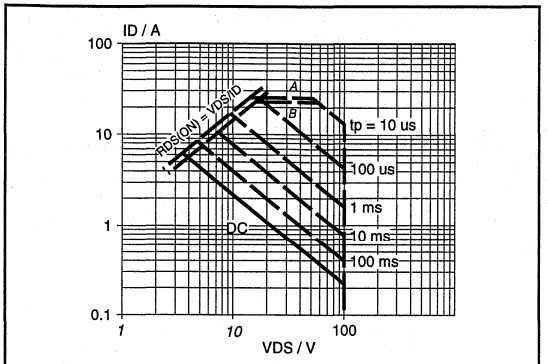


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

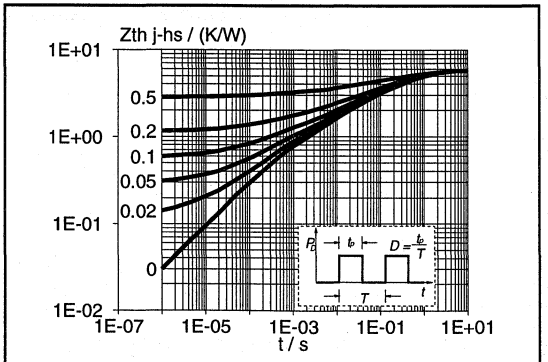


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

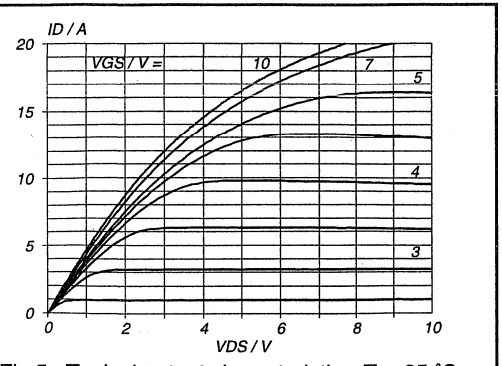


Fig.5. Typical output characteristics, T_j = 25 °C.
$I_D = f(V_{DS})$; parameter V_{GS}

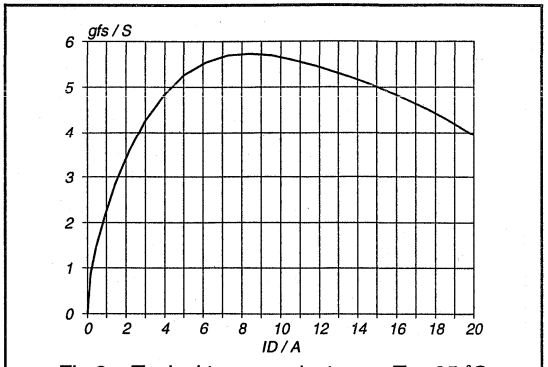


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

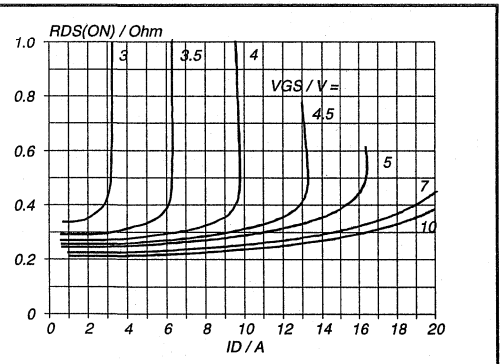


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

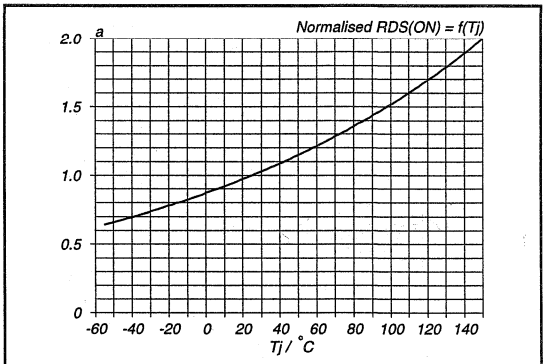


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 5 V

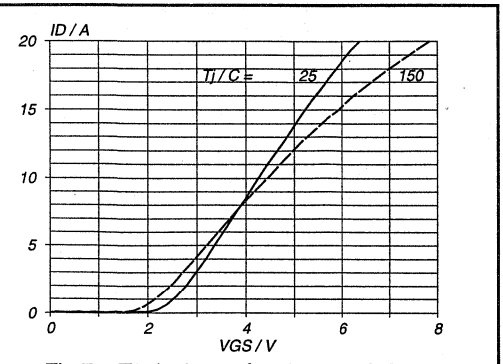


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

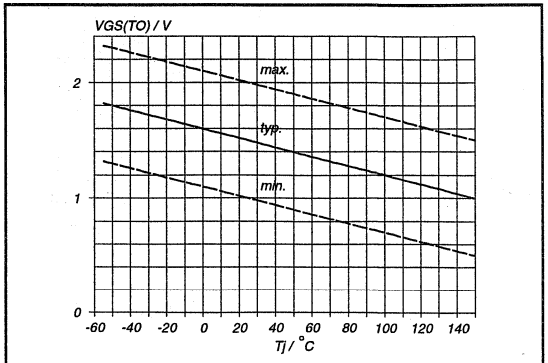


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

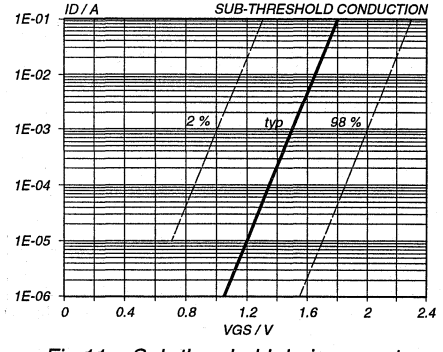


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

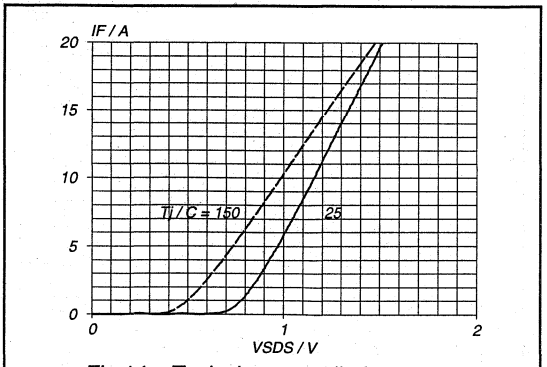


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

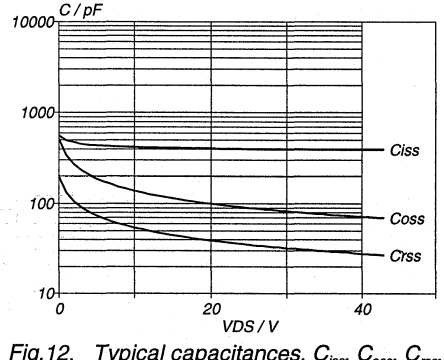


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

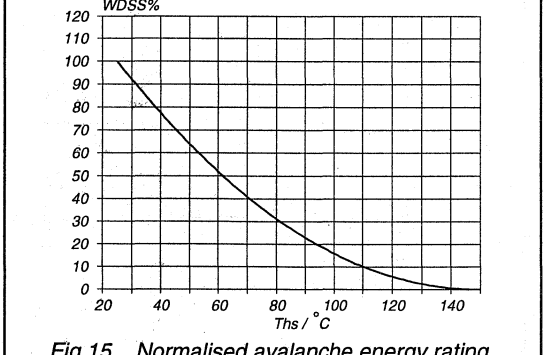


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 10$ A

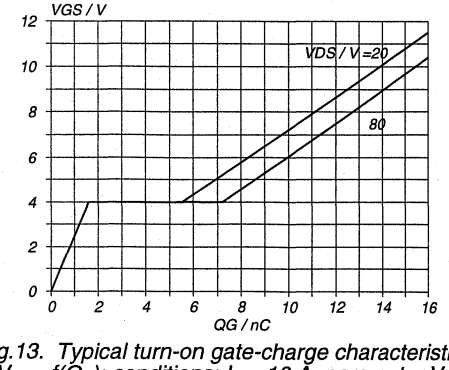


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 10$ A; parameter V_{DS}

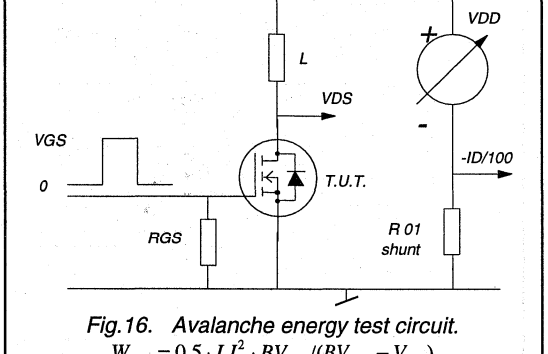


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK543-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

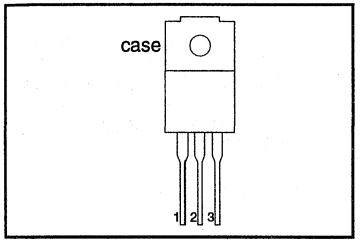
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK543	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	13	12	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} 5 V	0.085	0.1	Ω

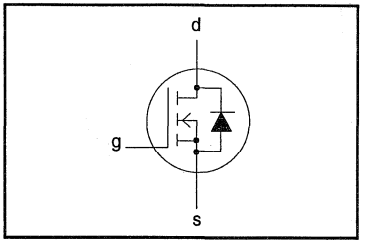
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-60A	-60B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	13	12	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	8.2	7.6	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	52	48	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK543-60A**	-	0.075	0.085	Ω
		I_D = 10 A **BUK543-60B**	-	0.08	0.10	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	7	10	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	130	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	95	120	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	110	ns
t_f	Turn-off fall time		-	65	85	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.20	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	45	mJ

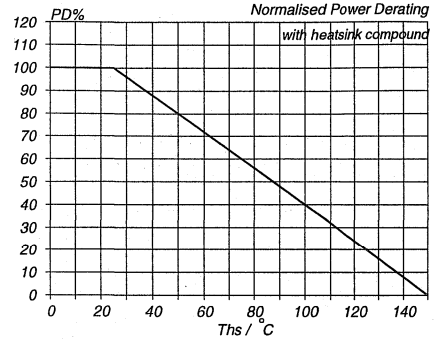


Fig.1. Normalised power dissipation.
PD% = 100·$P_D/P_{D\,25\,°C}$ = f(T_{hs})

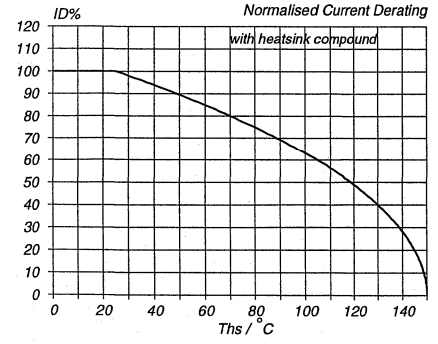


Fig.2. Normalised continuous drain current.
ID% = 100·$I_D/I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

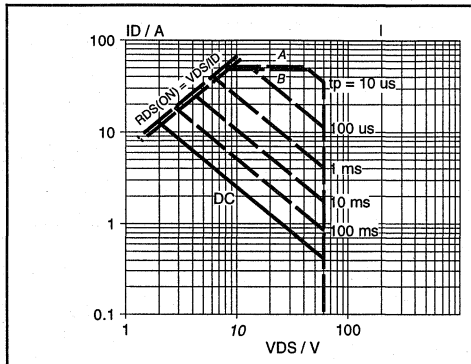


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

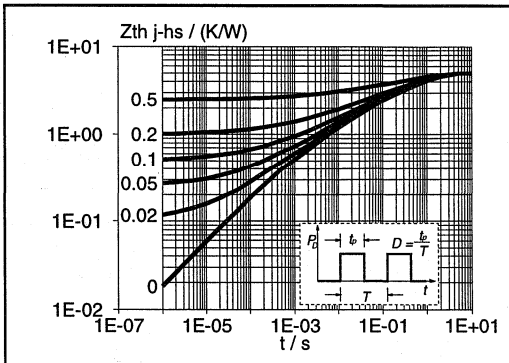


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

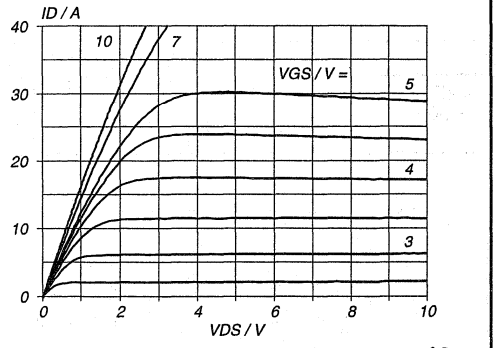


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

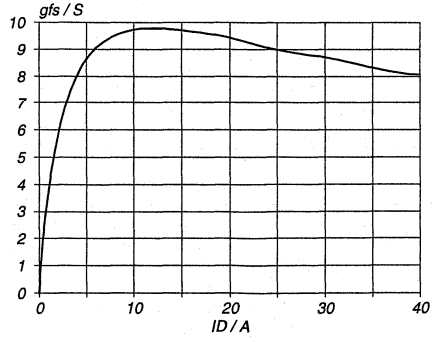


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

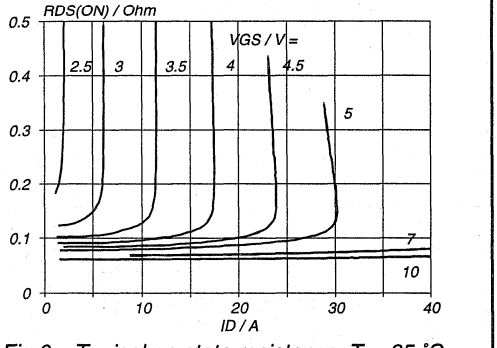


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

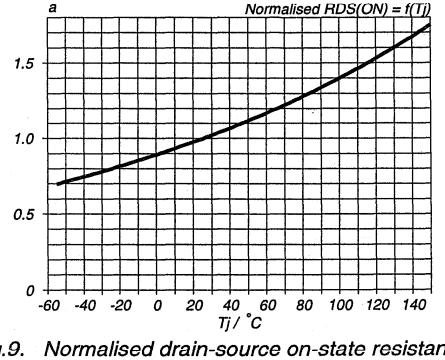


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 5 V

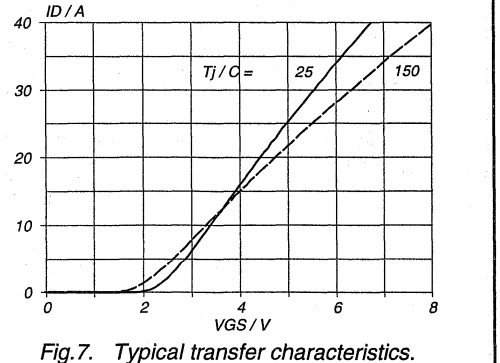


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

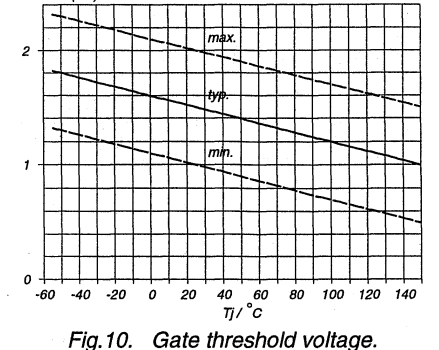


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

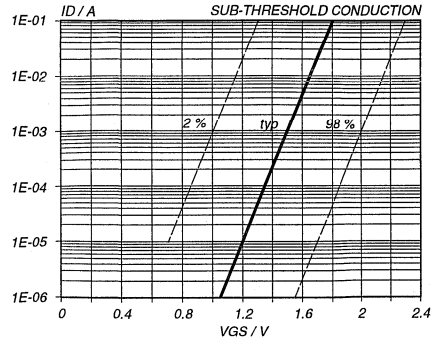


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

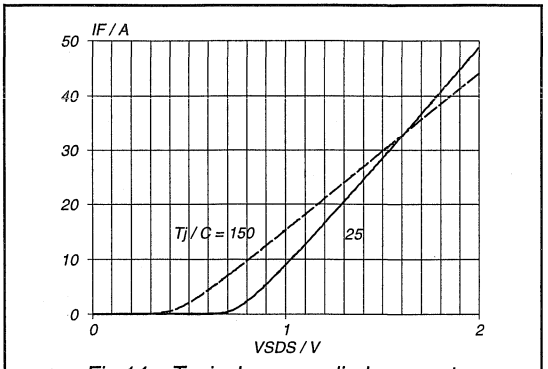


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

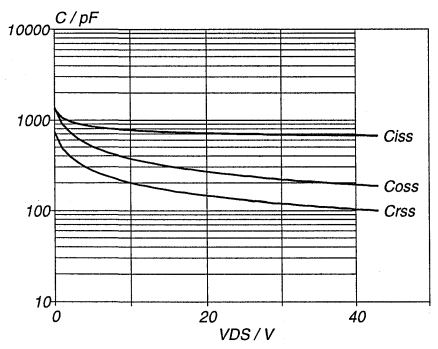


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

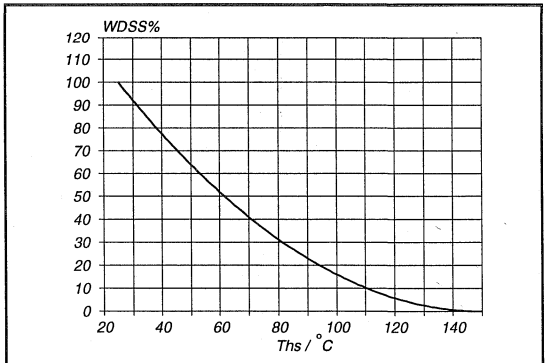


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 20$ A

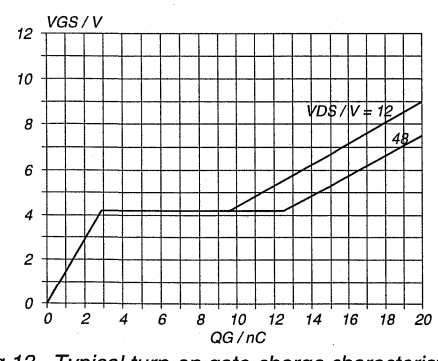


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 20$ A; *parameter* V_{DS}

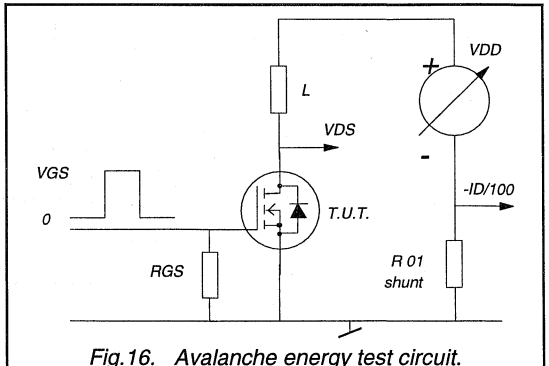


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK543-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

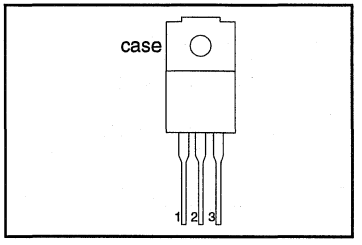
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK543	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	8.3	7.5	A
P_{tot}	Total power dissipation	25	25	W
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.18	0.22	Ω

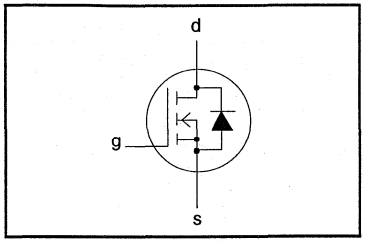
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	8.3	7.5	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	5.2	4.7	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	33	30	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK543-100A**	-	0.17	0.18	Ω
		I_D = 5 A **BUK543-100B**	-	0.20	0.22	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	6.0	8.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	825	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	90	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	90	115	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	8.3	A
I_{DRM}	Pulsed reverse drain current	-	-	-	33	A
V_{SD}	Diode forward voltage	I_F = 8.3 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 8.3 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.5	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 13 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	70	mJ

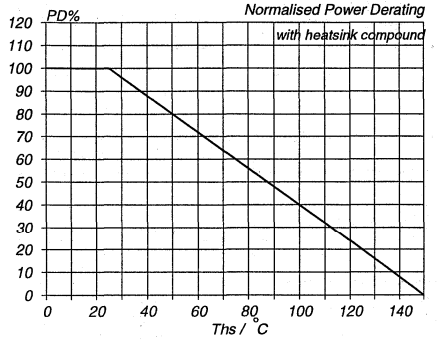


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

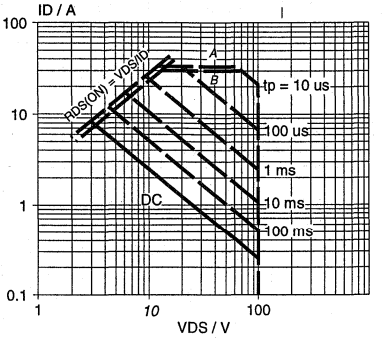


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

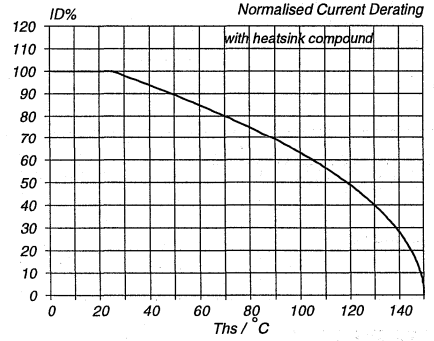


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

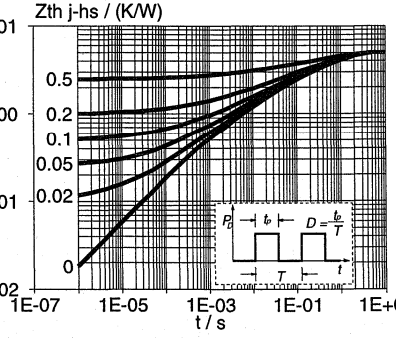


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

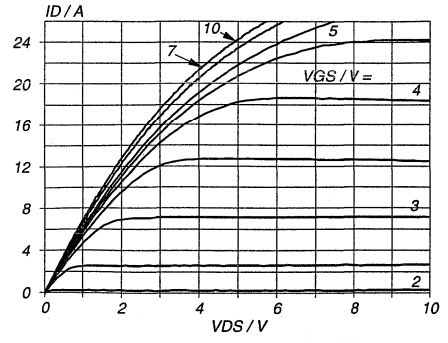


Fig.5. Typical output characteristics, $T_j = 25$ °C. $I_D = f(V_{DS})$; parameter V_{GS}

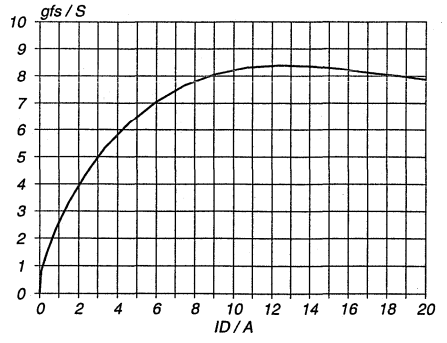


Fig.8. Typical transconductance, $T_j = 25$ °C. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

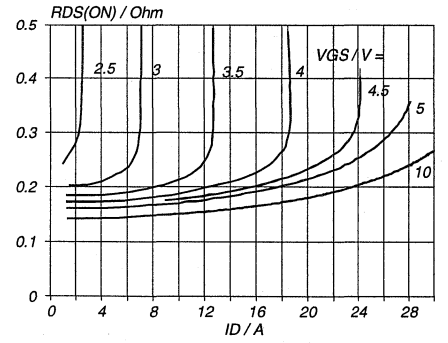


Fig.6. Typical on-state resistance, $T_j = 25$ °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

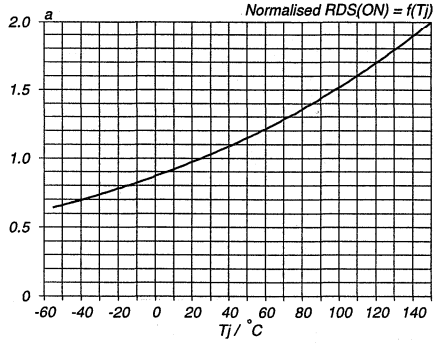


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 5$ A; $V_{GS} = 5$ V

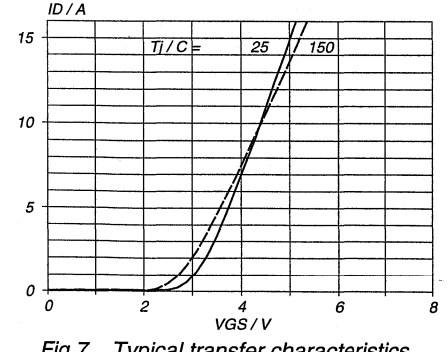


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

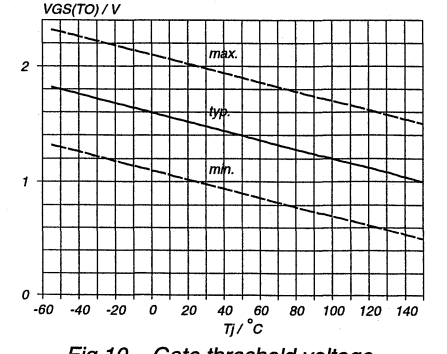


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

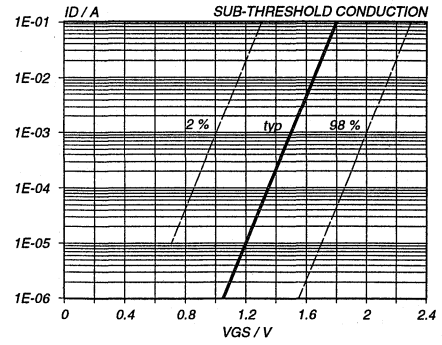


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

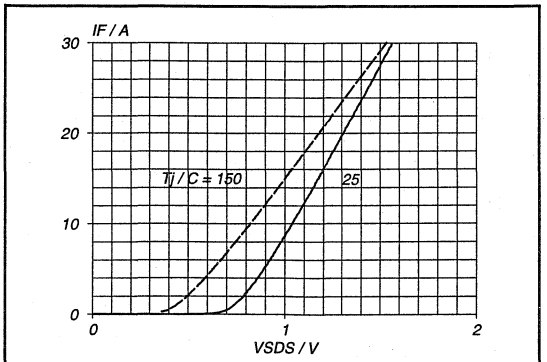


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

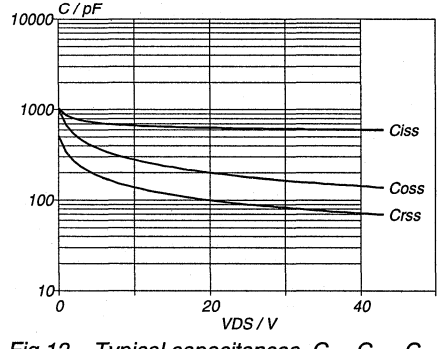


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

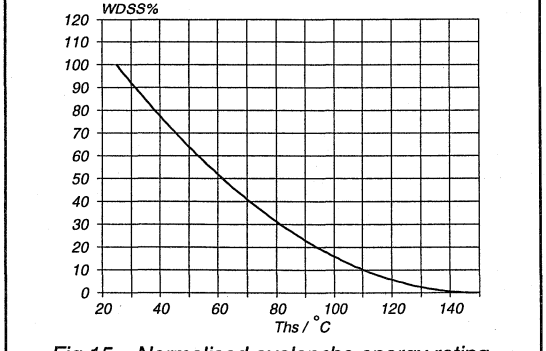


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 13$ A

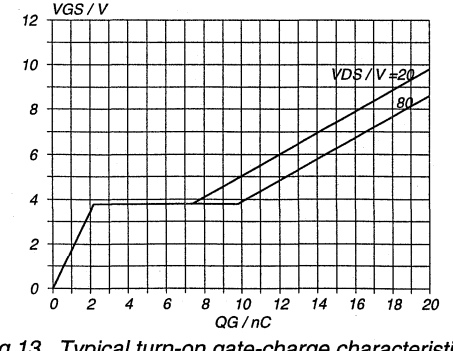


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 13$ A; parameter V_{DS}

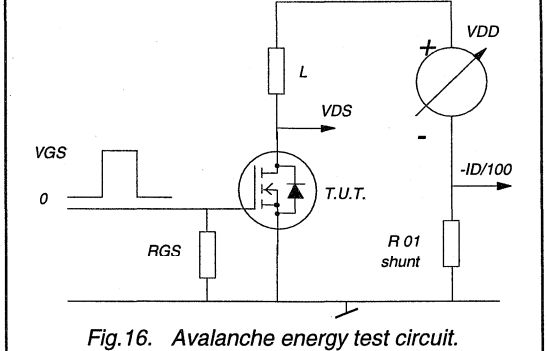


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK545-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

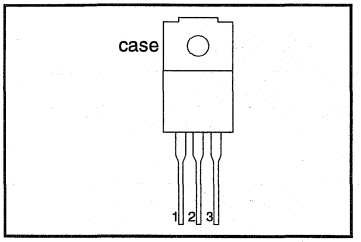
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK545	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	20	18	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.042	0.055	Ω

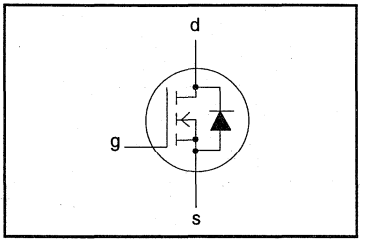
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-60A	-60B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	20	18	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	13	11	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	80	72	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK545-60A** I_D = 20 A **BUK545-60B**	- -	0.035 0.045	0.042 0.055	Ω Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	11	20	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	220	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	120	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	160	220	ns
t_f	Turn-off fall time		-	110	145	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	20	A
I_{DRM}	Pulsed reverse drain current	-	-	-	80	A
V_{SD}	Diode forward voltage	I_F = 20 A ; V_{GS} = 0 V	-	1.4	2.0	V
t_{rr}	Reverse recovery time	I_F = 20 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 39 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

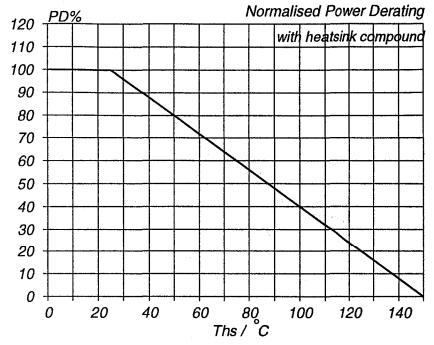


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

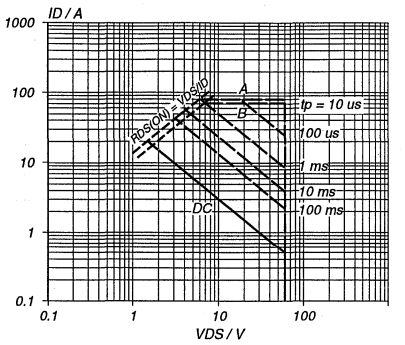


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

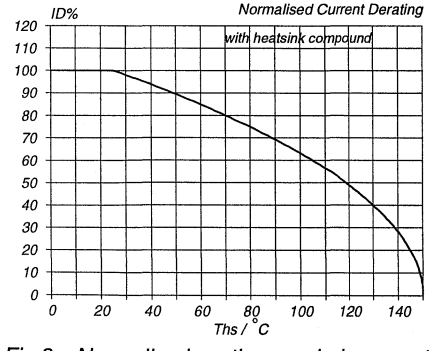


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

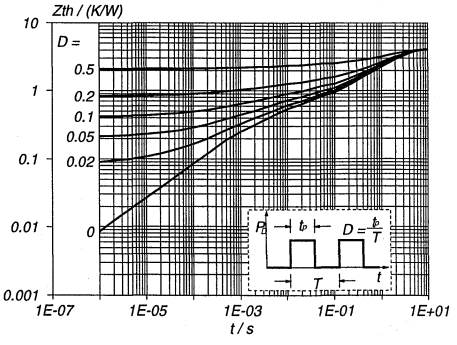


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

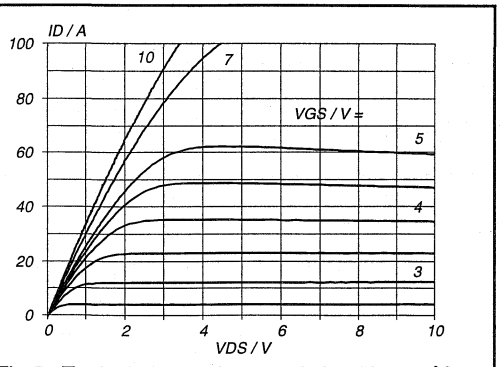


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

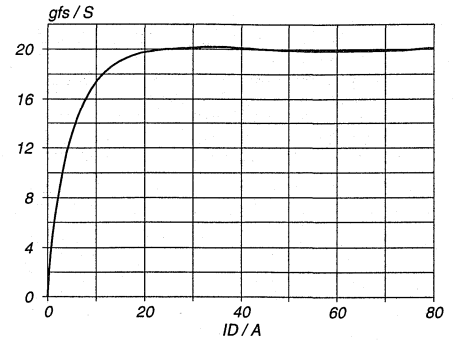


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

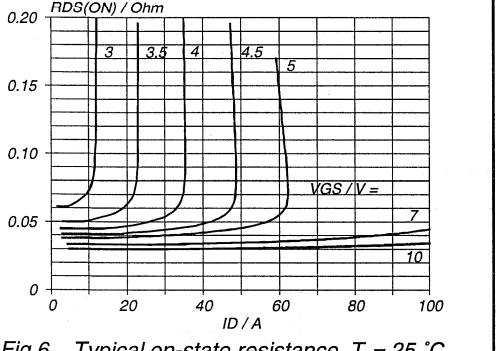


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

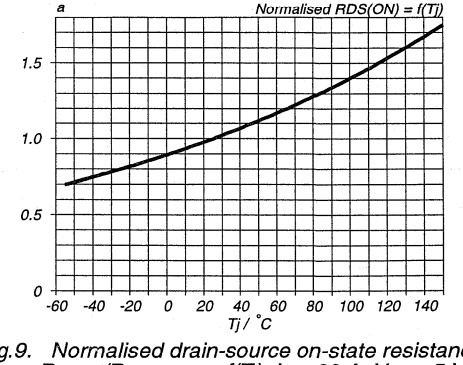


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

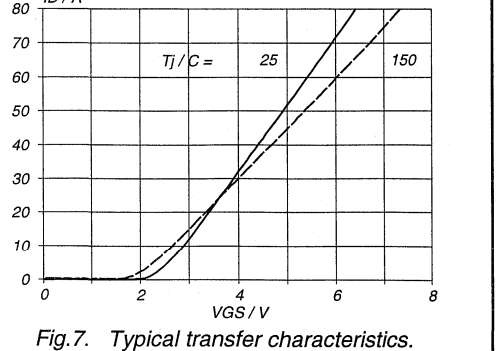


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

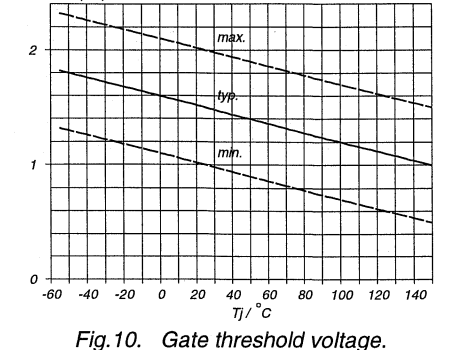


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

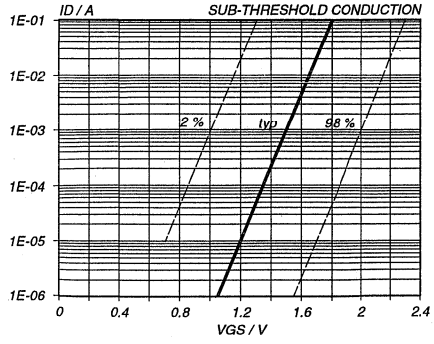


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

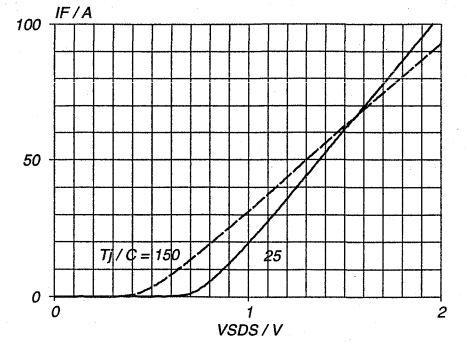


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

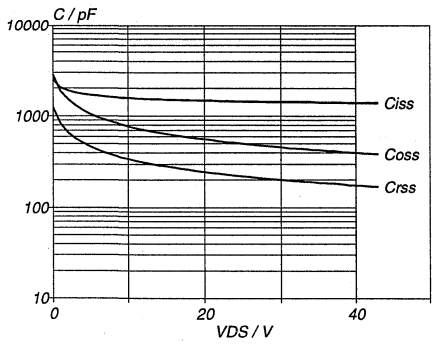


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

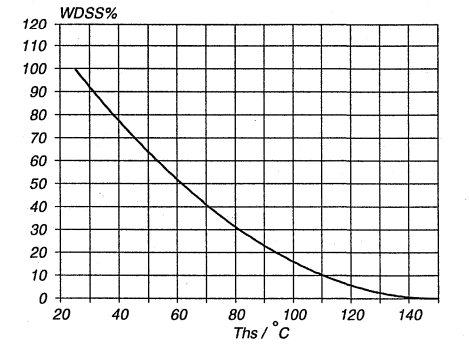


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 39$ A

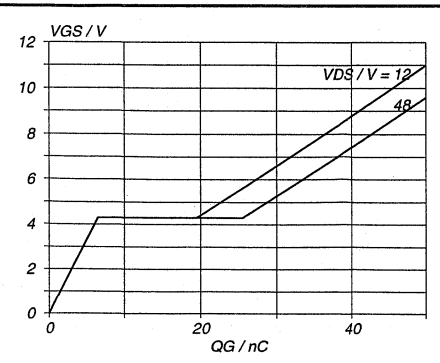


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 39$ A; parameter V_{DS}

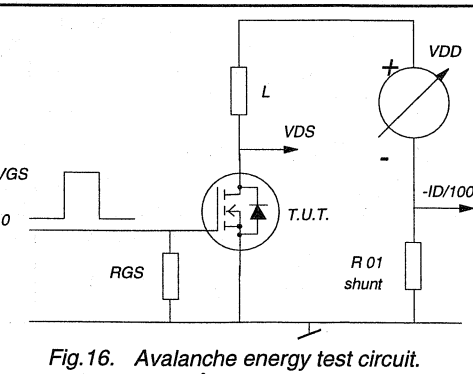


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK545-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

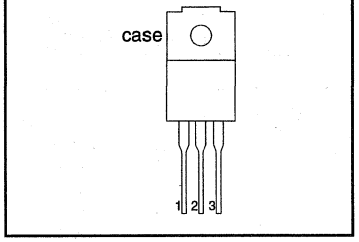
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	21	A
P_{tot}	Total power dissipation	30	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	38	mΩ

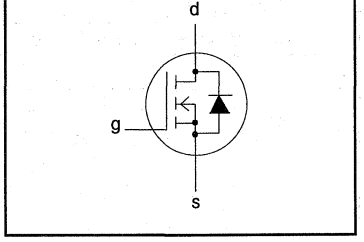
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	21	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	13.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	82	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	With heatsink compound	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	25	38	mΩ

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	11	20	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1200	1750	pF
C_{oss}	Output capacitance		-	470	600	pF
C_{rss}	Feedback capacitance		-	180	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	120	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	160	220	ns
t_f	Turn-off fall time		-	110	145	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	21	A
I_{DRM}	Pulsed reverse drain current	-	-	-	84	A
V_{SD}	Diode forward voltage	I_F = 21 A ; V_{GS} = 0 V	-	0.9	2.0	V
t_{rr}	Reverse recovery time	I_F = 21 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; $V_{DD} \leq$ 25 V ; T_{hs} = 25 °C V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

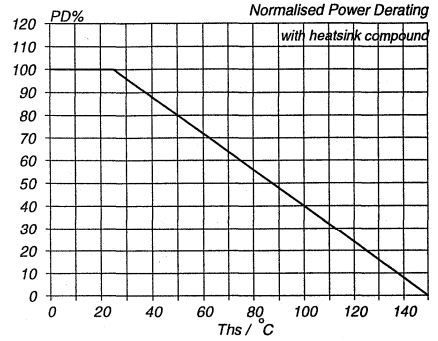


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

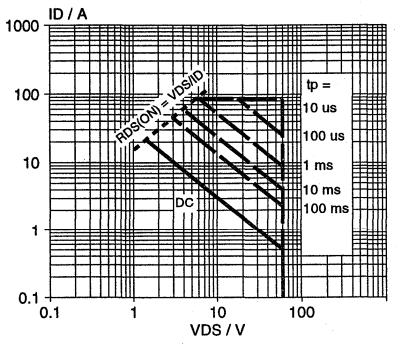


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

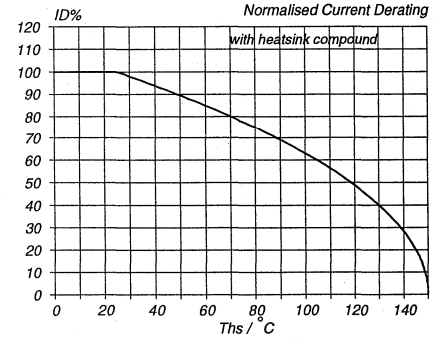


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

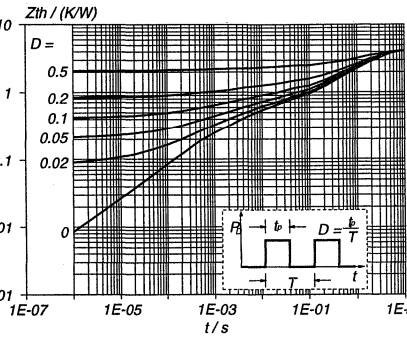


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

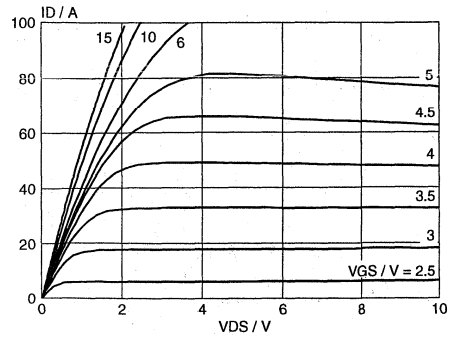


Fig.5. Typical output characteristics, $T_j = 25$ °C. $I_D = f(V_{DS})$; parameter V_{GS}

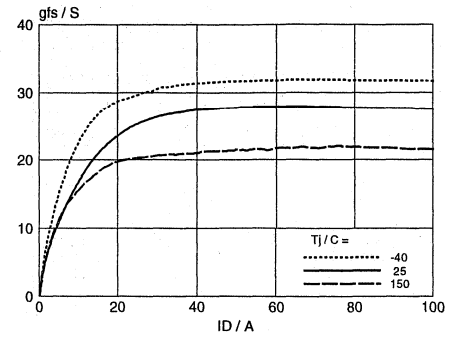


Fig.8. Typical transconductance, $T_j = 25$ °C. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 10$ V

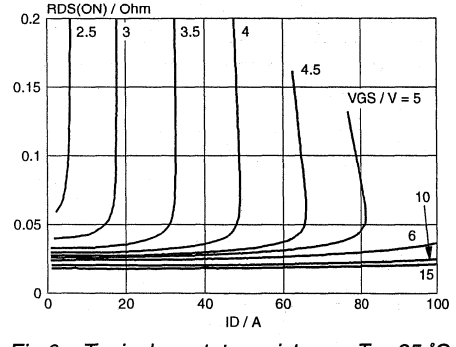


Fig.6. Typical on-state resistance, $T_j = 25$ °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

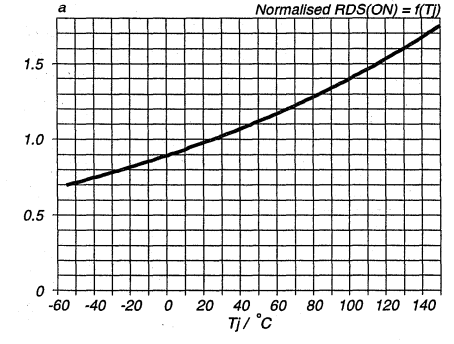


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 20$ A; $V_{GS} = 5$ V

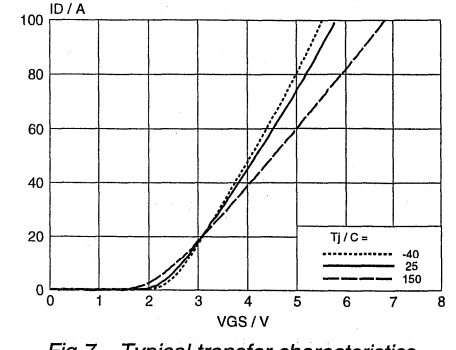


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

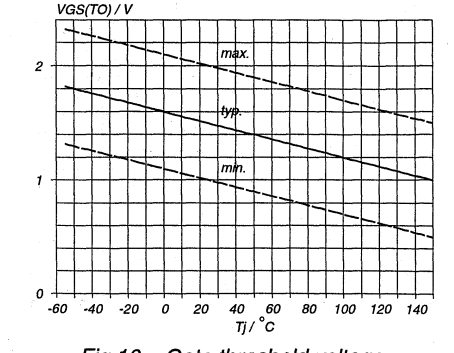


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

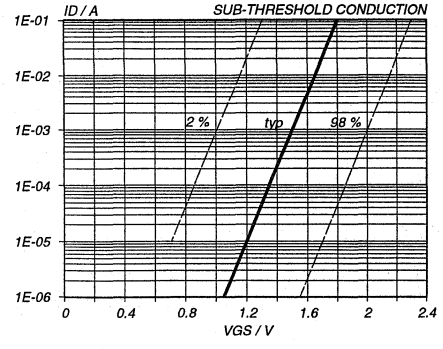


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

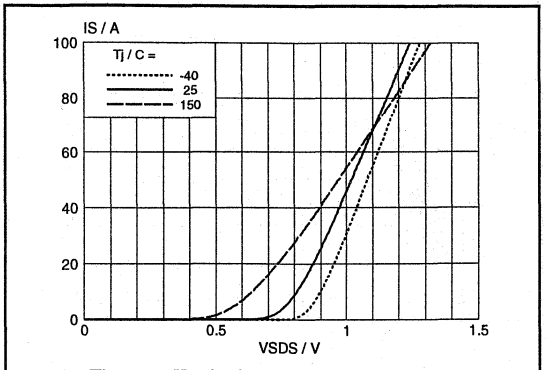


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

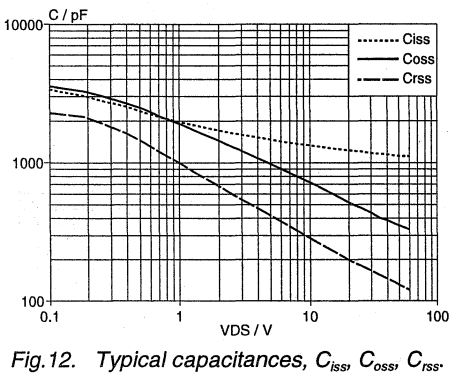


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

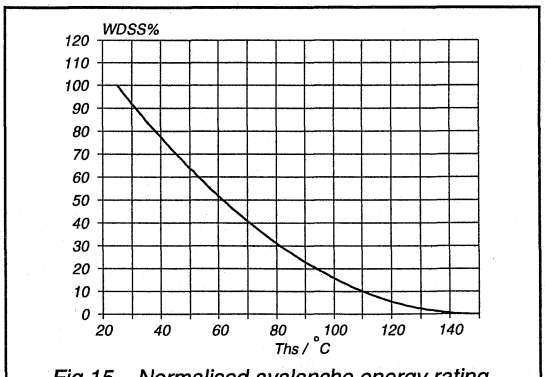


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 41$ A

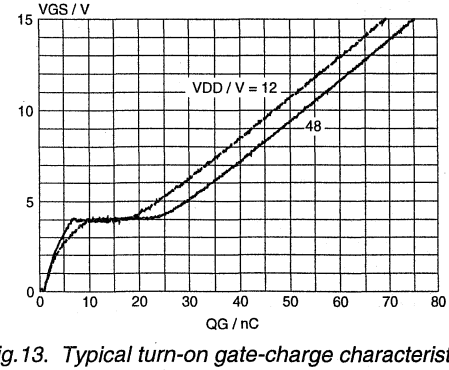


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

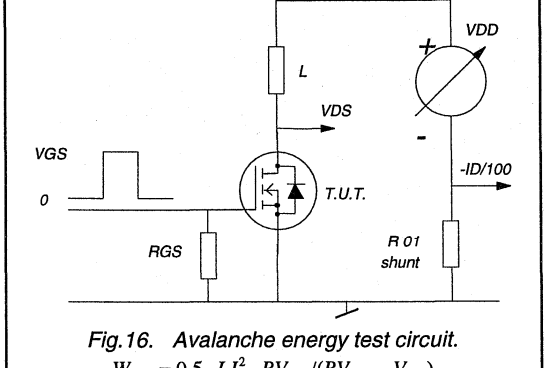


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK545-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

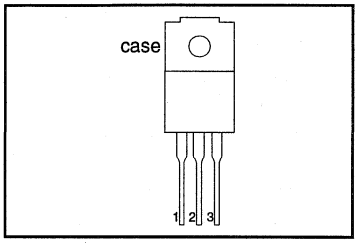
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK545	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	13	12	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.085	0.11	Ω

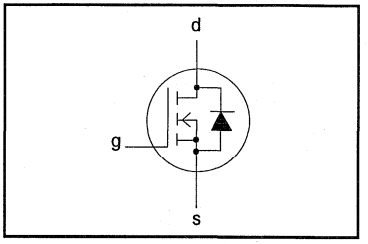
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	13	12	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	8.2	7.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	52	48	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK545-100A**	-	0.075	0.085	Ω
		I_D = 13 A **BUK545-100B**	-	0.09	0.11	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	10	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	280	350	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	65	85	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	135	180	ns
t_f	Turn-off fall time		-	80	110	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.70	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; $V_{DD} \leq$ 50 V ; V_{gs} = 5 V ; R_{gs} = 50 Ω	-	-	140	mJ

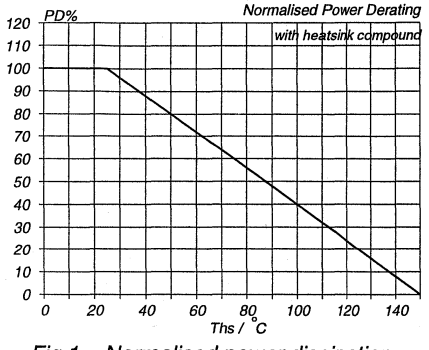


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

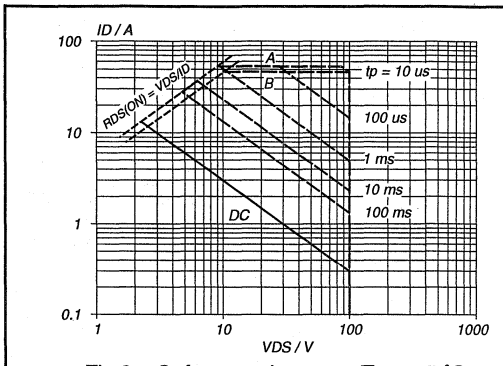


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

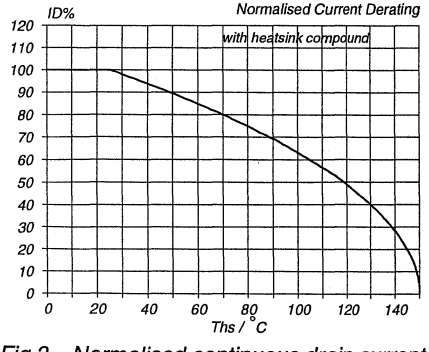


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 5 V

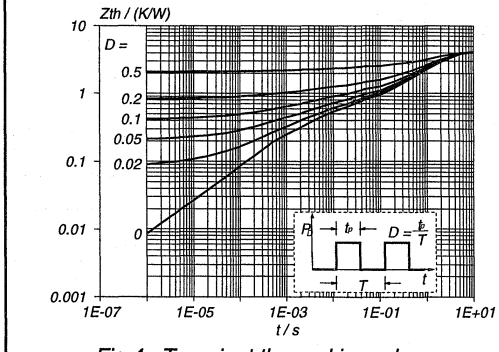


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

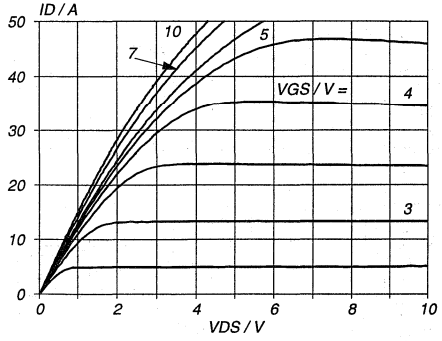


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

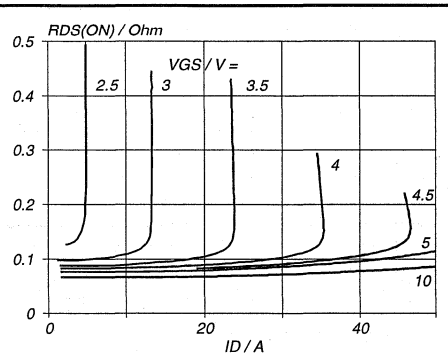


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

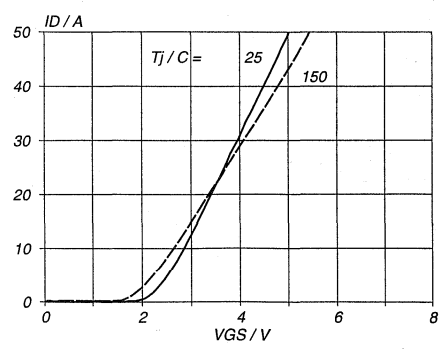


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

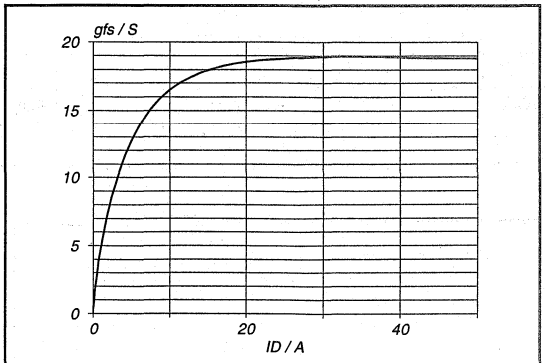


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

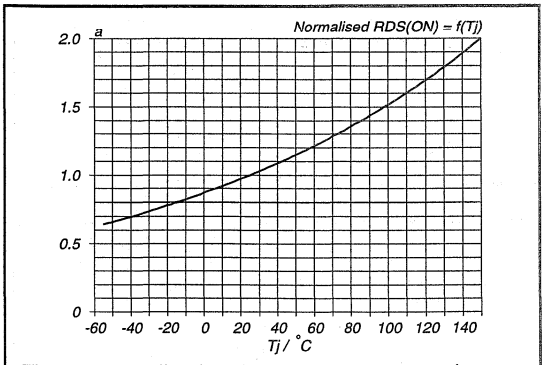


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 13 A; V_{GS} = 5 V

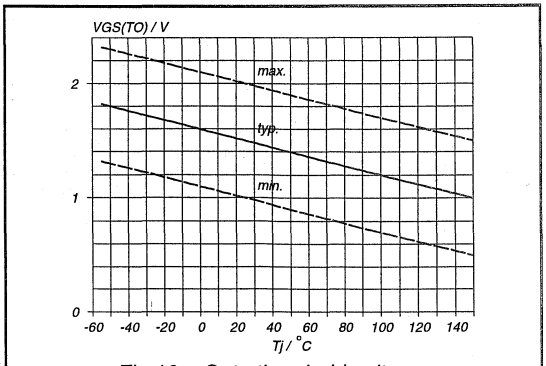


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

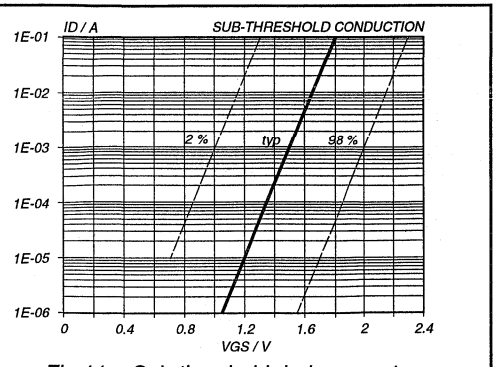


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

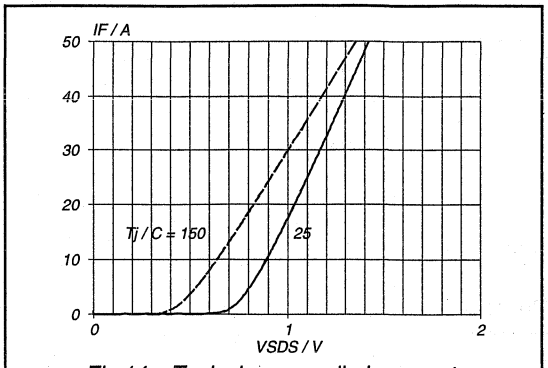


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

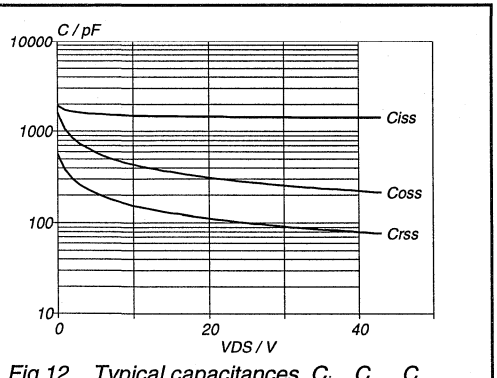


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

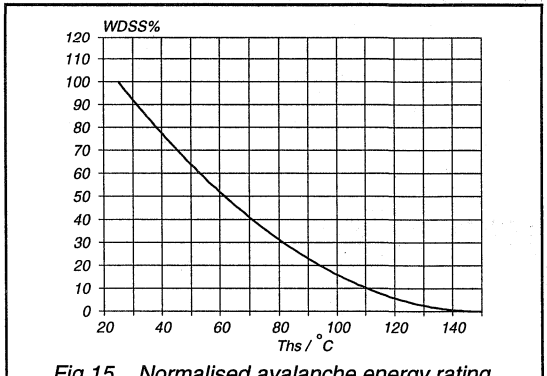


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 25$ A

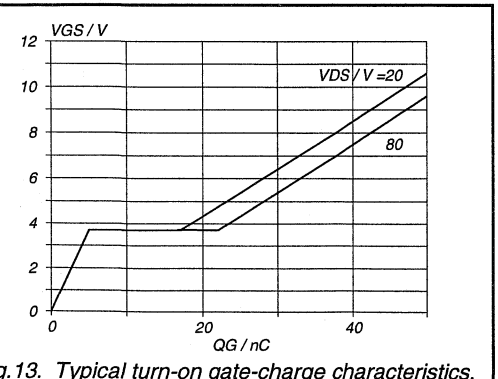


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 25$ A; parameter V_{DS}

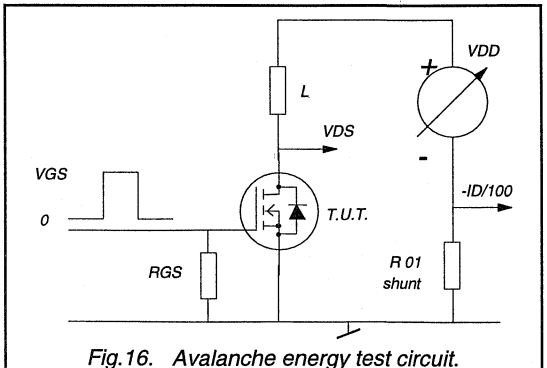


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK545-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

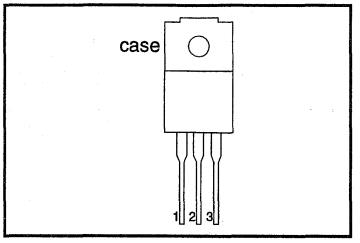
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK545	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	7.6	7	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.23	0.28	Ω

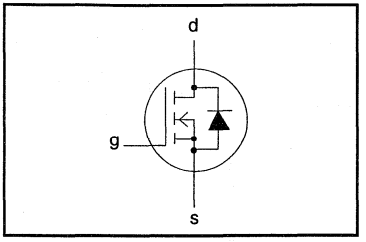
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-200A	-200B	
I_D	Drain current (DC)	T_{hs} = 25 °C	-	7.6	7	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	4.8	4.4	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	30	28	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30		W
T_{stg}	Storage temperature	-	- 55	150		°C
T_j	Junction Temperature	-	-	150		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK545-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK545-200B**	-	0.24	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	8.0	15	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1600	2000	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	75	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	140	180	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	7.6	A
I_{DRM}	Pulsed reverse drain current	-	-	-	30	A
V_{SD}	Diode forward voltage	I_F = 7.6 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 7.6 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.3	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; $V_{DD} \leq 100$ V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	100	mJ

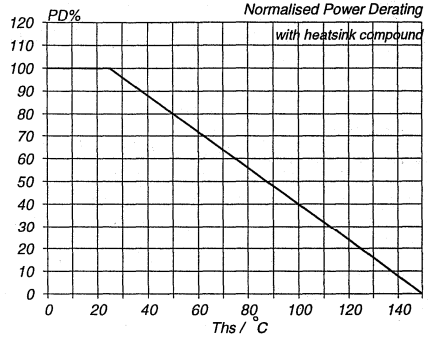


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

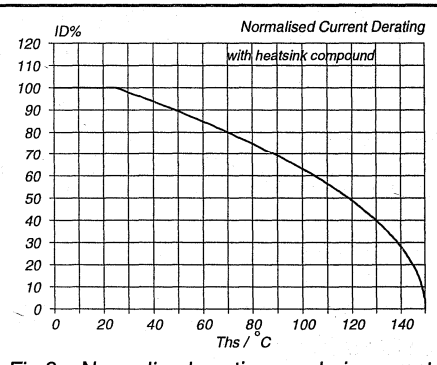


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq 5$ V

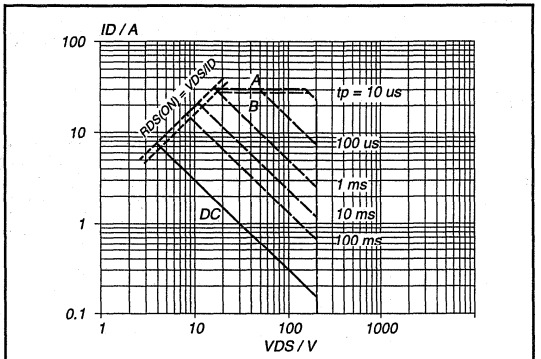


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

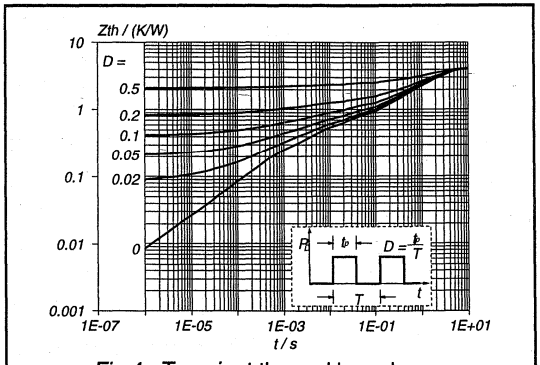


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

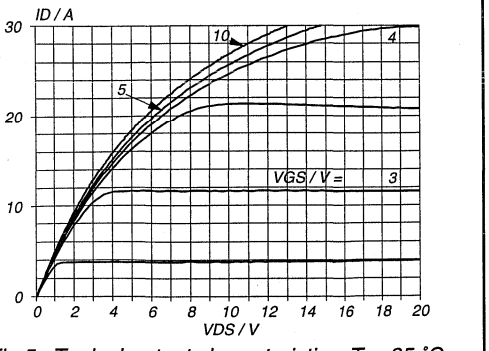


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

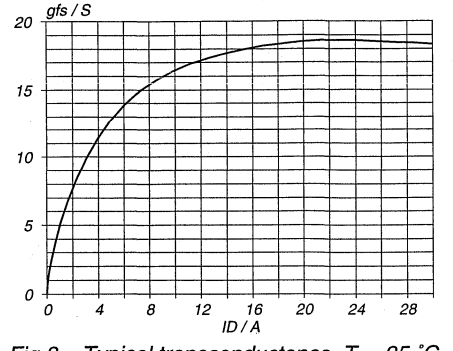


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

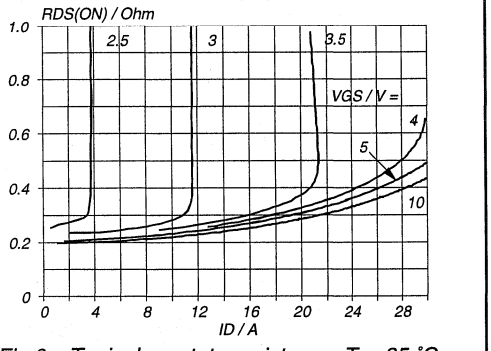


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

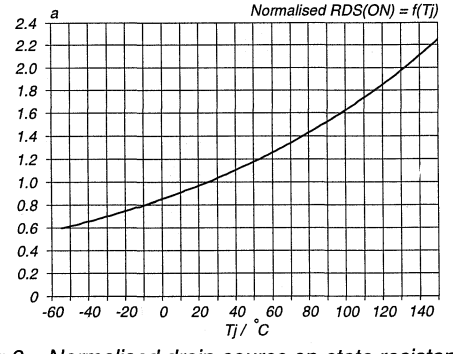


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 7 A; V_{GS} = 5 V

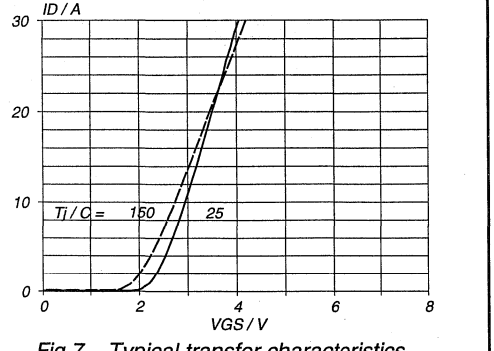


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

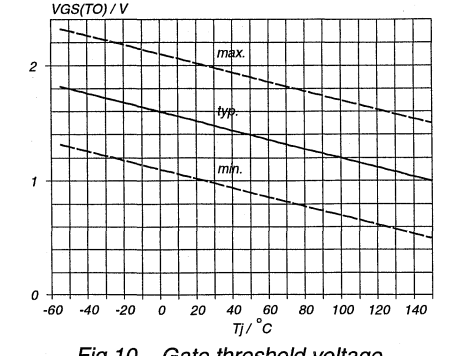


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

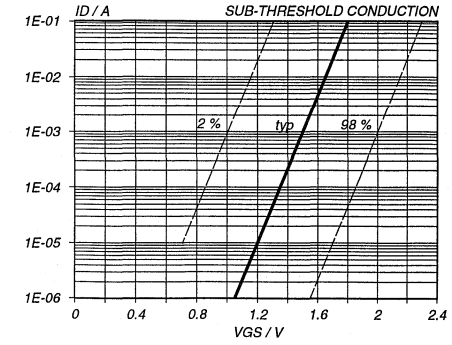


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

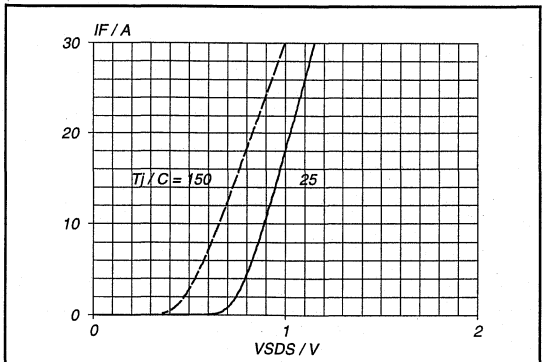


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

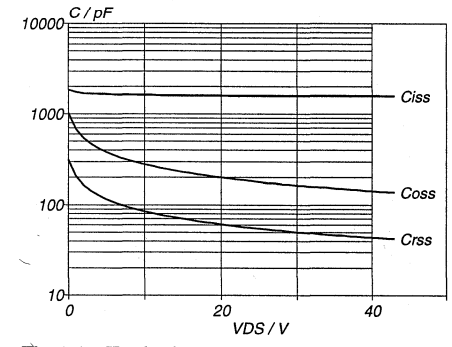


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

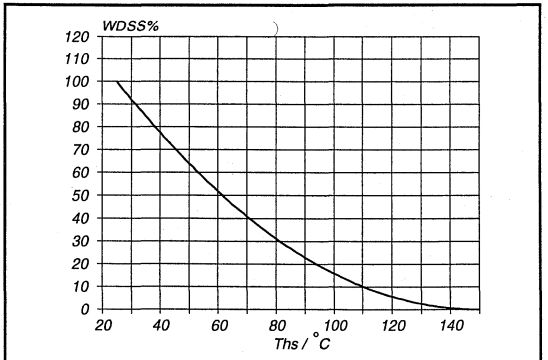


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 14$ A

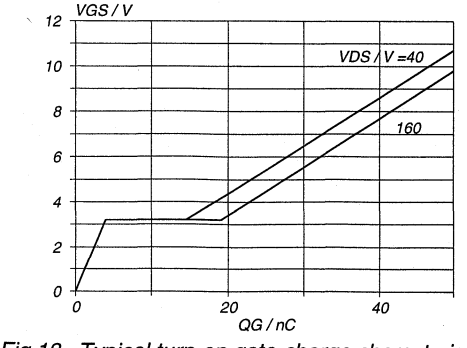


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 14$ A; *parameter* V_{DS}

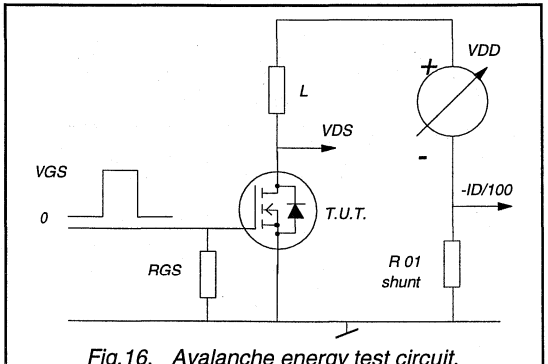


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK552-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

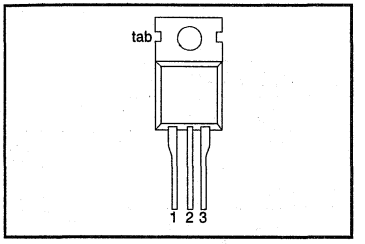
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK552	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.15	0.18	Ω

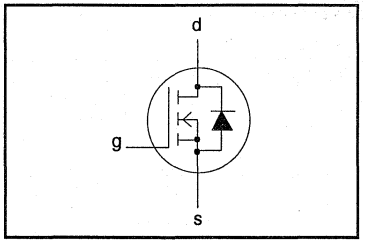
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK552-60A**	-	0.12	0.15	Ω
		I_D = 8.5 A **BUK552-60B**	-	0.15	0.18	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	5	6.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	65	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	60	80	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	45	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

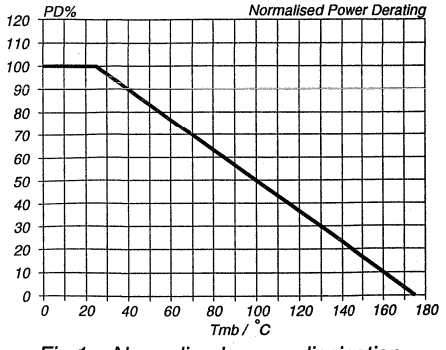


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

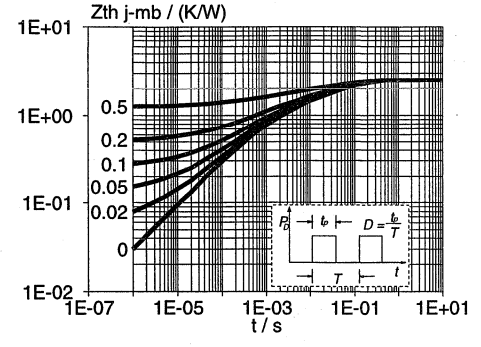


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

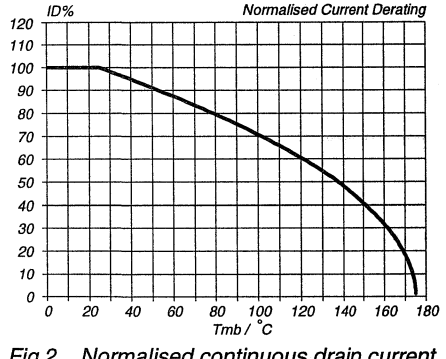


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

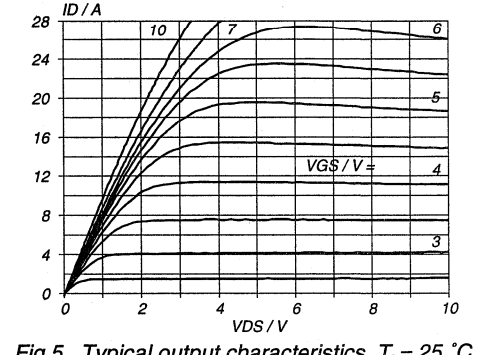


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

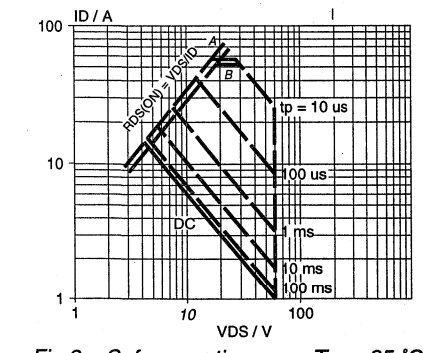


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

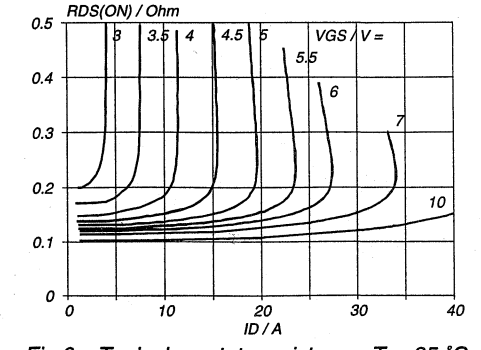


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

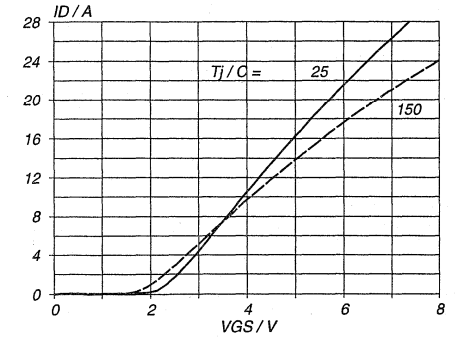


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

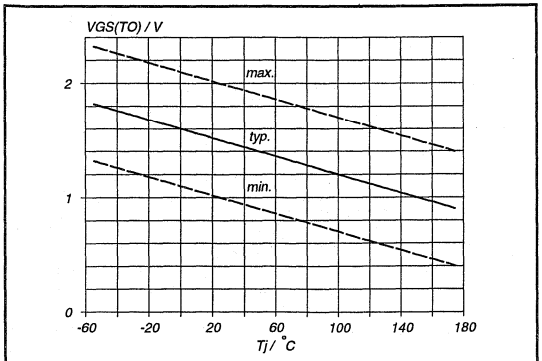


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

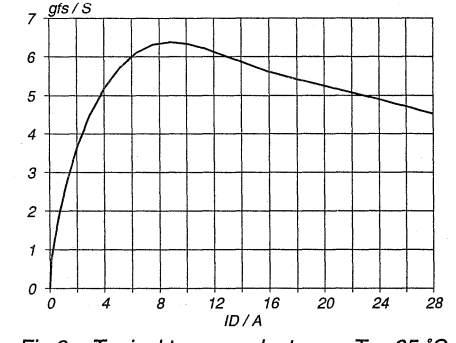


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

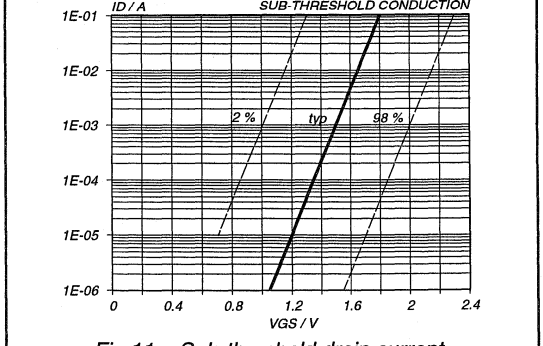


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

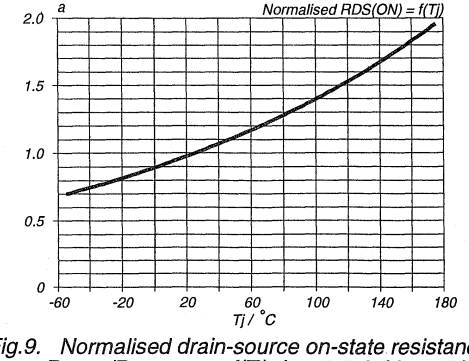


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 8.5$ A; $V_{GS} = 5$ V

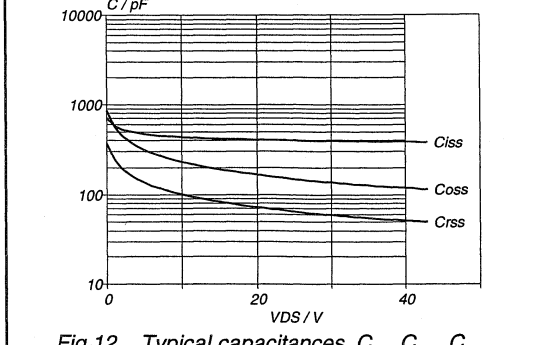


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

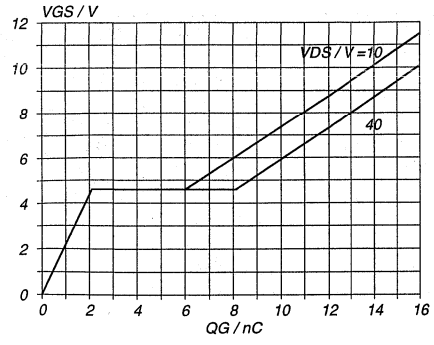


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

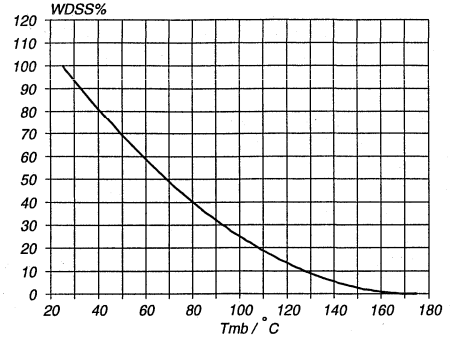


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

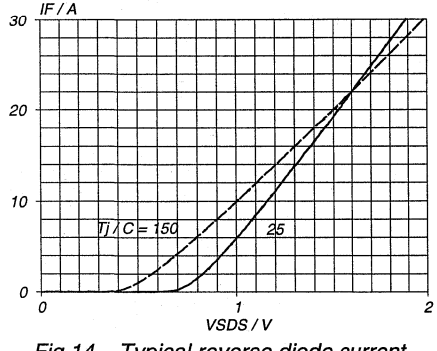


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

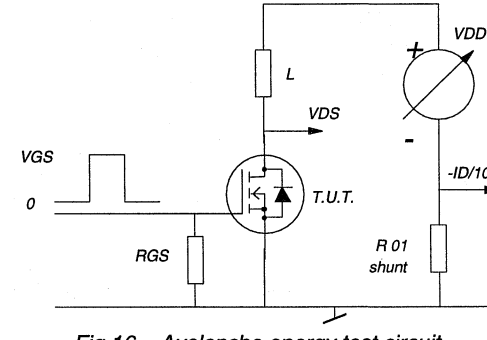


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK552-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

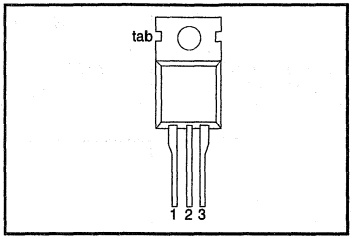
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK552	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	10	8.5	A
P_{tot}	Total power dissipation	60	60	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.28	0.35	Ω

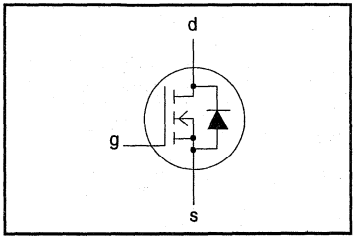
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	10	8.5	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7	6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	40	34	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK552-100A**	-	0.25	0.28	Ω
		I_D = 5.5 A **BUK552-100B**	-	0.3	0.35	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	4.5	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	10	A
I_{DRM}	Pulsed reverse drain current	-	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 10 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

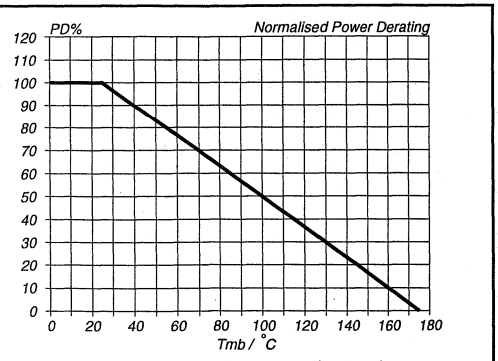


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

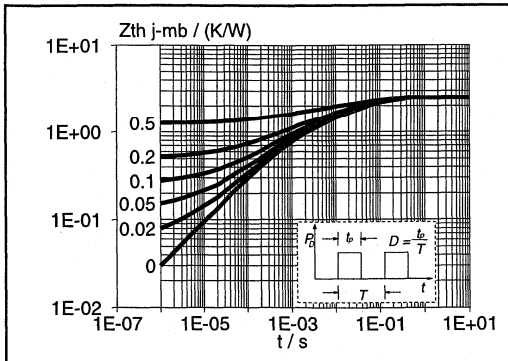


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

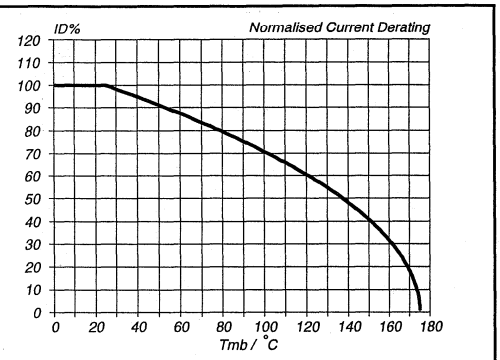


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

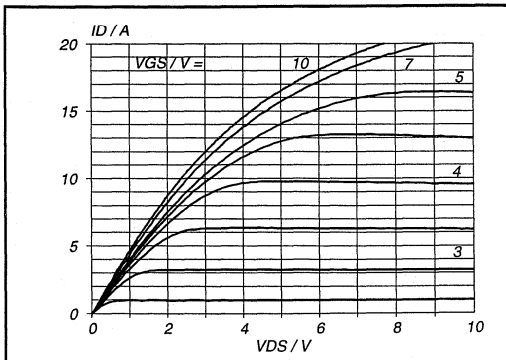


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

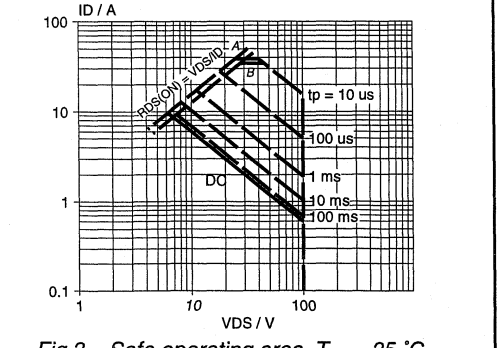


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

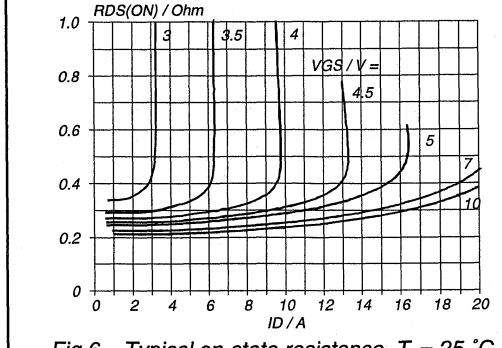


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

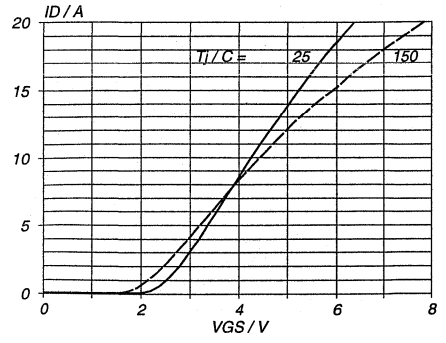


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

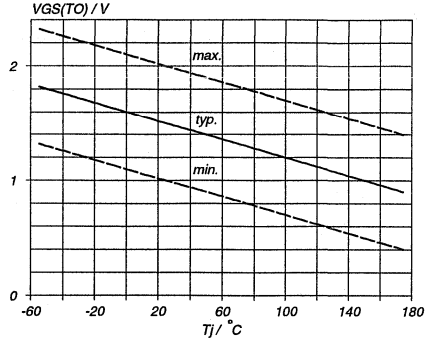


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

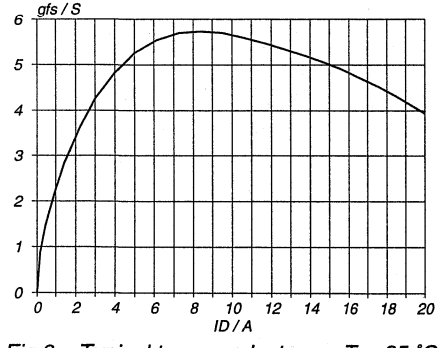


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

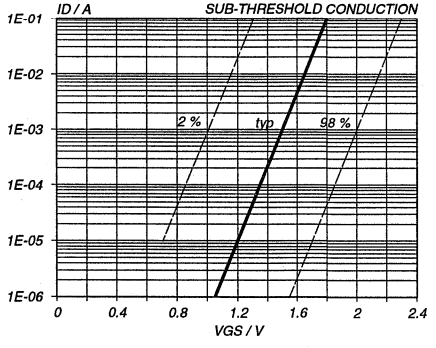


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

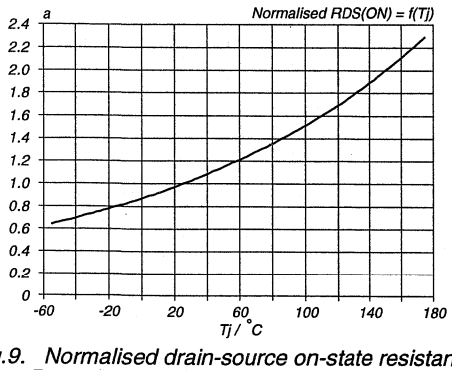


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 5 V

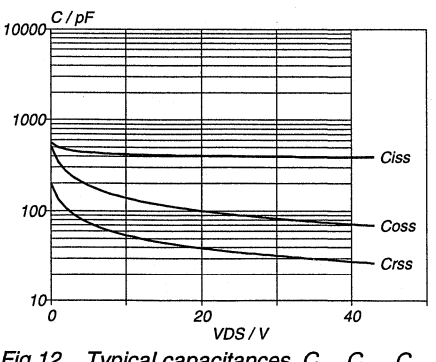


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

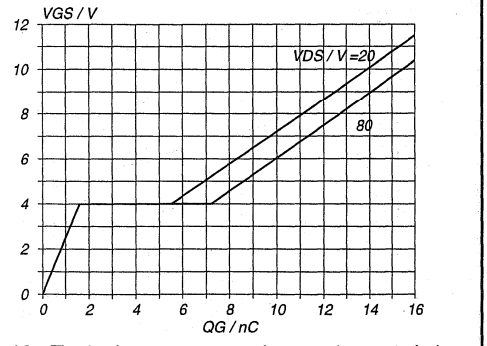


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 10$ A; parameter V_{DS}

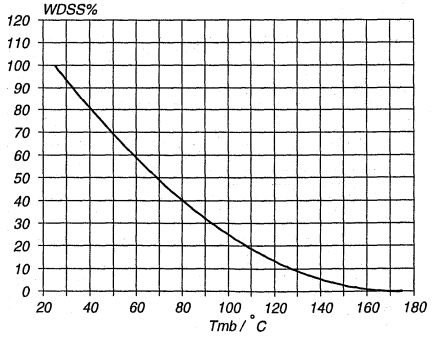


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 10$ A

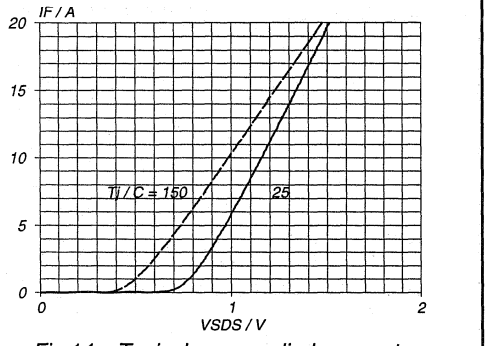


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

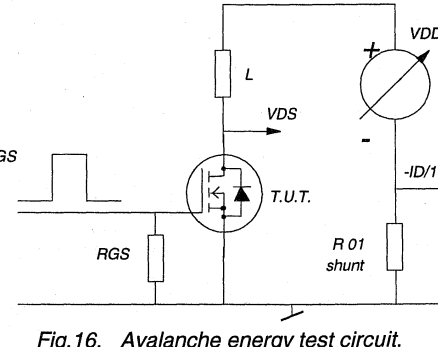


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Voltage clamped logic level FET

BUK553-48C

GENERAL DESCRIPTION

Protected N-channel enhancement mode logic level field-effect power transistor in a plastic envelope.
The device is intended for use in automotive applications. It has built-in zener diodes providing active drain voltage clamping.

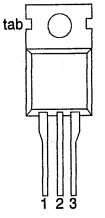
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamp voltage	40	48	58	V
I_D	Drain current (DC)			21	A
P_{tot}	Total power dissipation			75	W
T_j	Junction temperature			175	°C
W_{DSRR}	Repetitive clamped turn off energy; T_j = 150°C			50	mJ
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V			85	mΩ

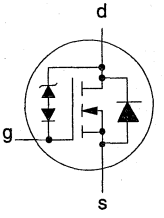
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	continuous	-	30	V
V_{DG}	Drain-gate voltage	continuous	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	21	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	15	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	84	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DG}$	Drain-gate zener voltage	$0.2 \leq -I_G \leq 0.4$ mA; $-55°C \leq T_j \leq 150°C$	38	45	54	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	1.0	1.5	2.0	V
$V_{GS(ON)}$	Gate voltage	V_{DS} = 10 V; I_D = 10 A; $-55°C \leq T_j \leq 150°C$	2.0	3.1	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	0.01	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V; T_j = 150 °C	-	0.1	10	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A	-	65	85	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain source clamp voltage (peak value)	R_G = 10 kΩ; I_D = 10 A; $-55 \leq T_j \leq 150°C$; Inductive load.	40	48	58	V
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	7	12	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	550	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	100	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 12 V; I_D = 5 A;	-	3.5	-	µs
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 kΩ;	-	22	-	µs
$t_{d\,off}$	Turn-off delay time		-	16	-	µs
t_f	Turn-off fall time		-	18	-	µs
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	21	A
I_{DRM}	Pulsed reverse drain current	-	-	-	84	A
V_{SD}	Diode forward voltage	I_F = 21 A ; V_{GS} = 0 V	-	1.3	1.7	V

CLAMPED ENERGY LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSRS}	Non-repetitive drain-source clamped inductive turn off energy	T_j = 25°C prior to clamping; I_D = 10 A; $V_{DD} \leq$ 16 V; V_{GS} = 5 V; R_G = 10 kΩ; inductive load	-	200	mJ
W_{DSRR}	Drain-source repetitive clamped inductive turn off energy	T_j = 150°C prior to clamping; I_D = 10 A; $V_{DD} \leq$ 16 V; V_{GS} = 5 V; R_G = 10 kΩ; inductive load	-	50	mJ

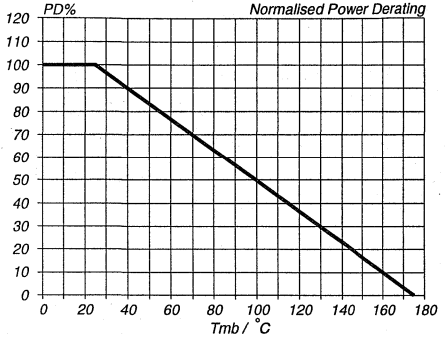


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

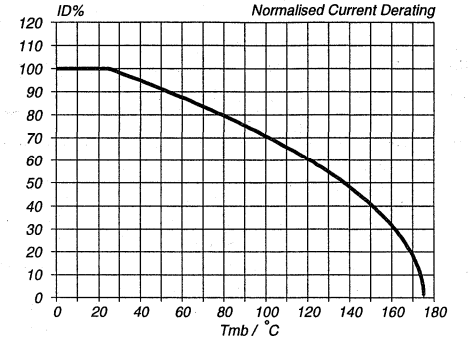


Fig.3. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

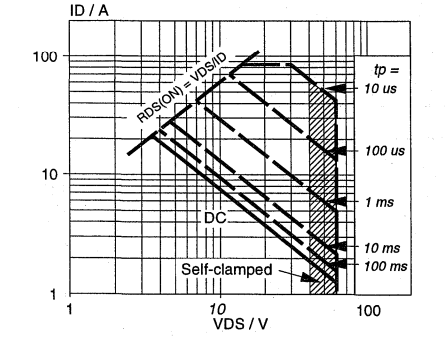


Fig.2. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

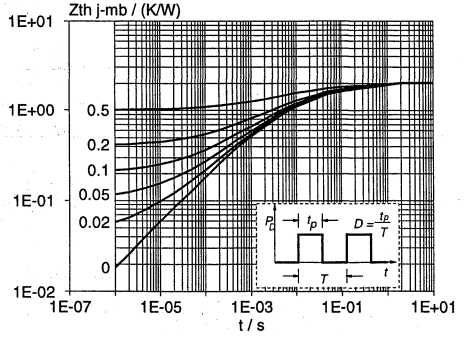


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

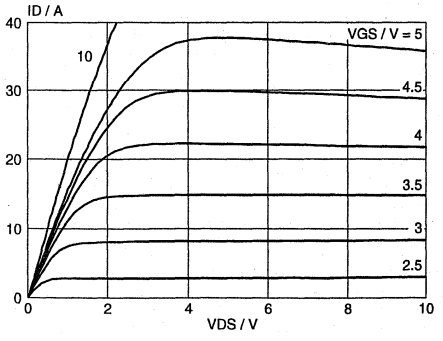


Fig.5. Typical output characteristics, $T_j = 25$ °C. $I_D = f(V_{DS})$; parameter V_{GS}

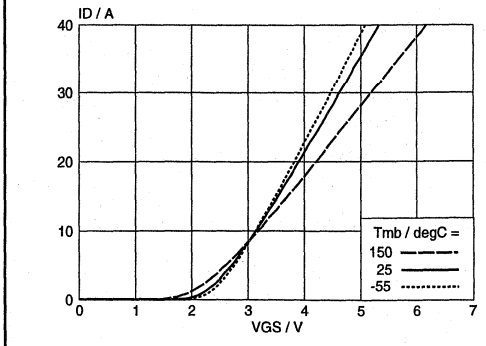


Fig.8. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V.

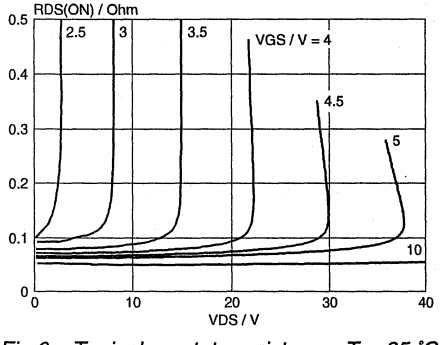


Fig.6. Typical on-state resistance, $T_j = 25$ °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

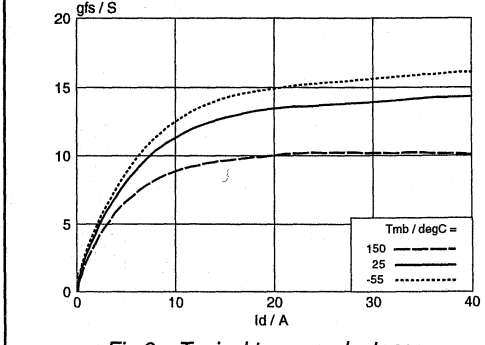


Fig.9. Typical transconductance. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

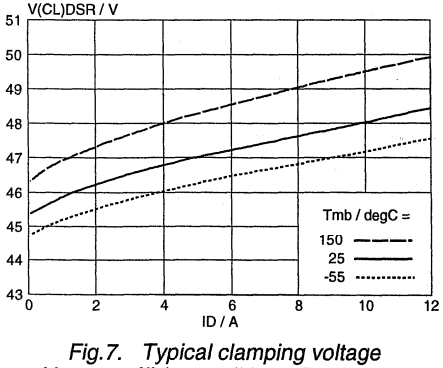


Fig.7. Typical clamping voltage $V_{(CL)DSR} = f(I_D)$; conditions: $R_G = 10$ kΩ

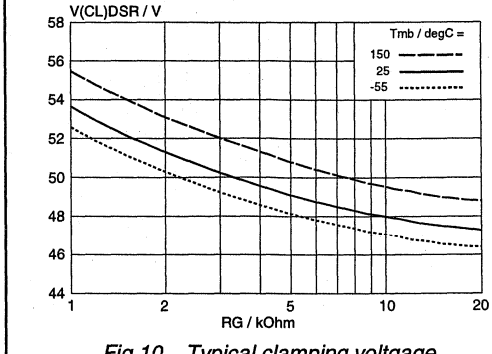


Fig.10. Typical clamping voltgage $V_{(CL)DSR} = f(R_G)$; conditions: $I_D = 10$ A.

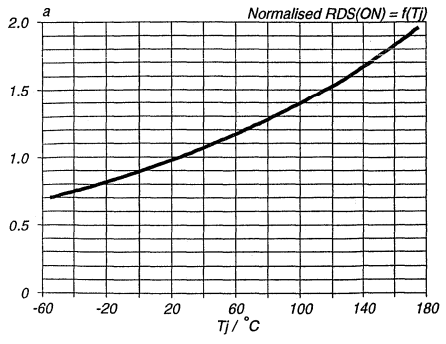


Fig.11. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 5 V

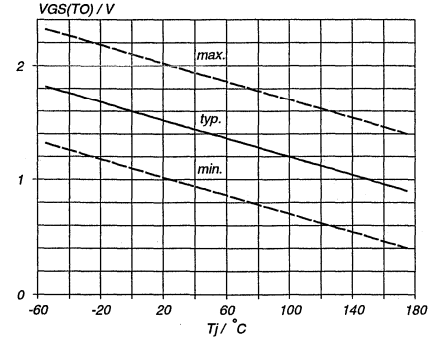


Fig.14. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

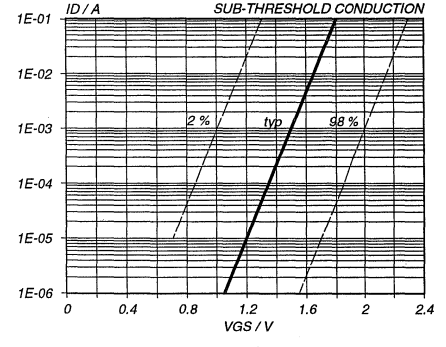


Fig.12. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

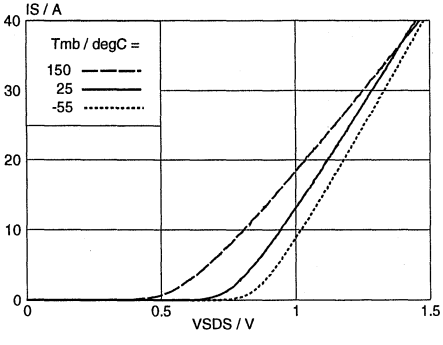


Fig.15. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

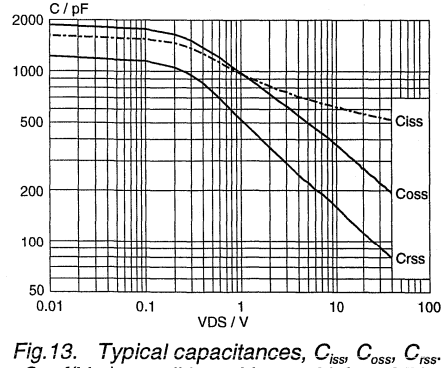


Fig.13. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

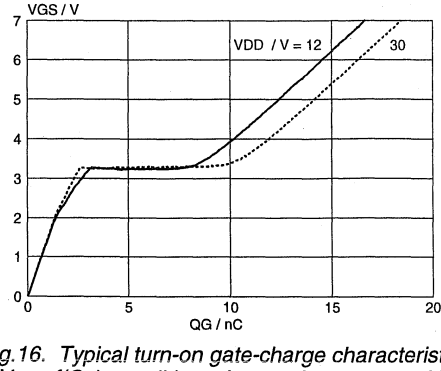


Fig.16. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 10 A; parameter V_{DS}

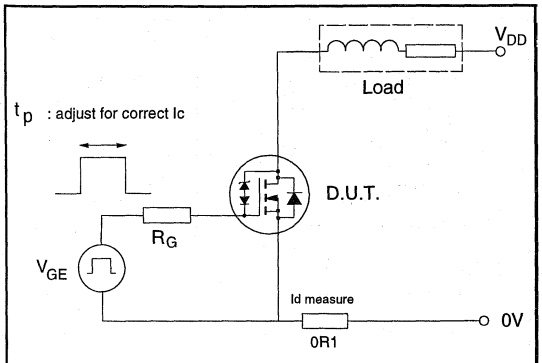


Fig.17. Inductive clamping test circuit.

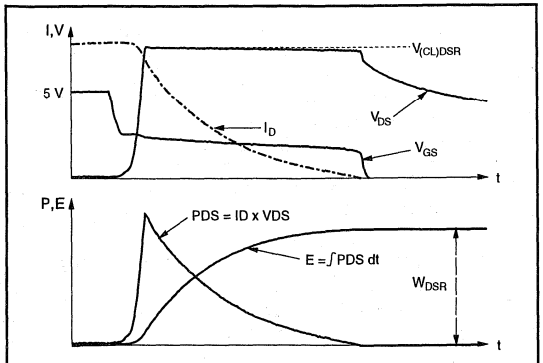


Fig.18. Typical Inductive Clamping waveforms

PowerMOS transistor Logic level FET

BUK553-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

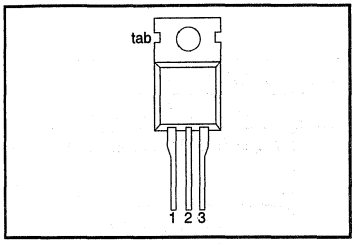
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK553	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	21	20	A
P_{tot}	Total power dissipation	75	75	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.085	0.10	Ω

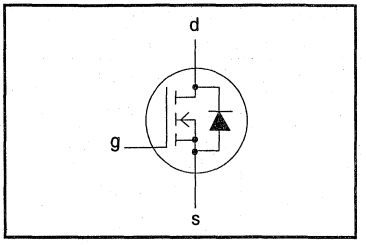
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	21	20	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	15	14	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	84	80	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK553-60A**	-	0.075	0.085	Ω
		I_D = 10 A **BUK553-60B**	-	0.08	0.10	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	7	10	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	130	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	95	120	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	110	ns
t_f	Turn-off fall time		-	65	85	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	21	A
I_{DRM}	Pulsed reverse drain current	-	-	-	84	A
V_{SD}	Diode forward voltage	I_F = 21 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 21 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	45	mJ

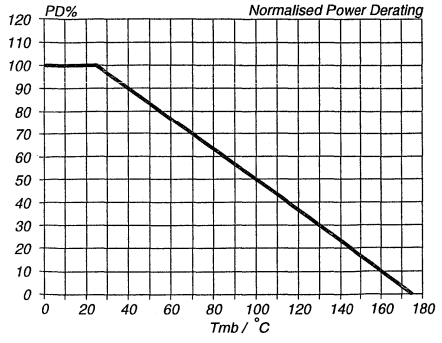


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

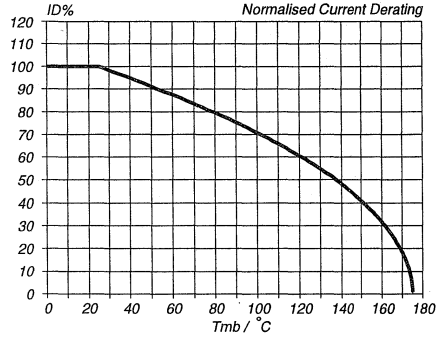


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

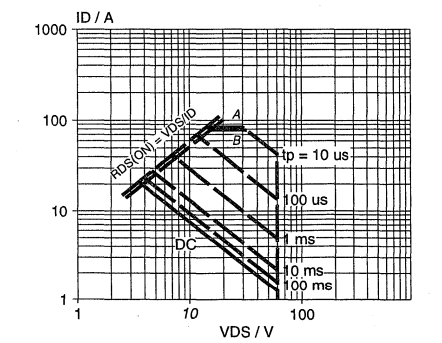


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

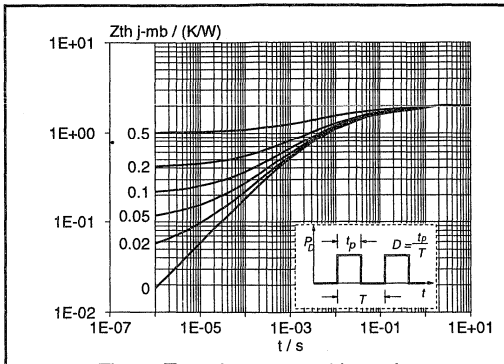


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

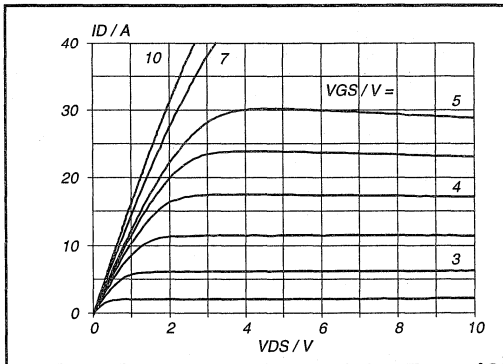


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

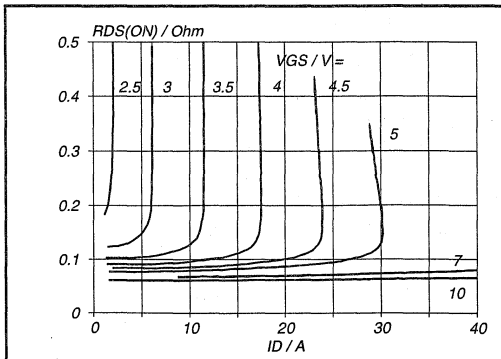


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

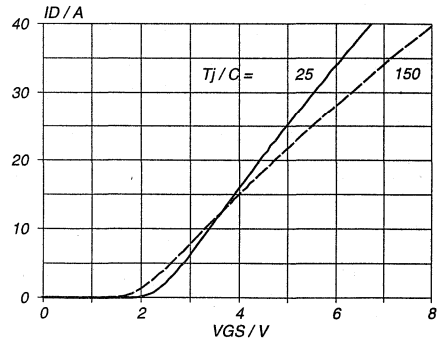


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

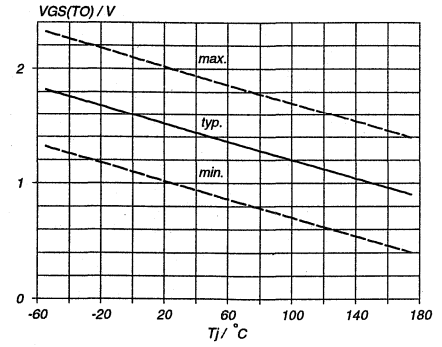


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

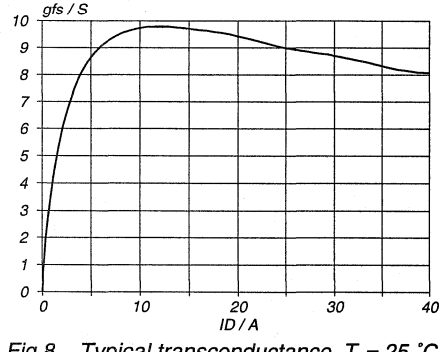


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

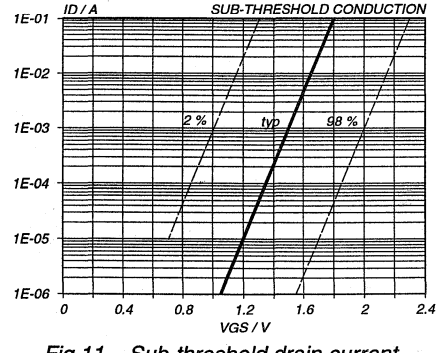


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

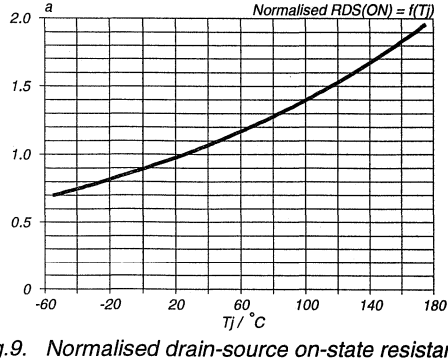


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 5 V

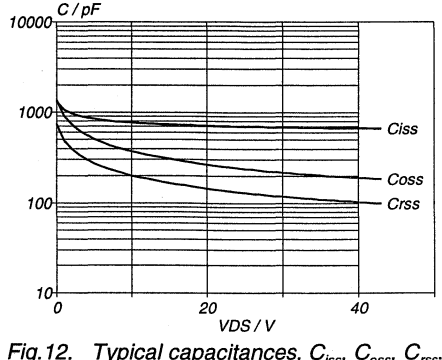


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

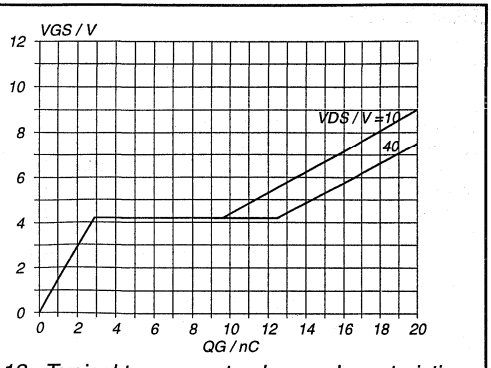


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 20$ *A; parameter* V_{DS}

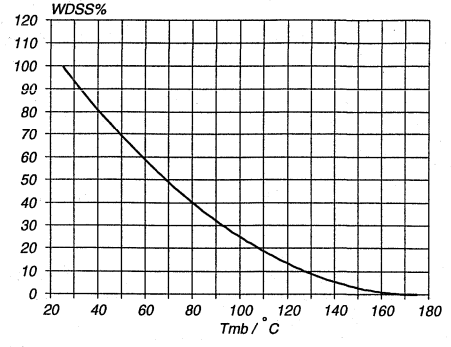


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; *conditions:* $I_D = 20$ *A*

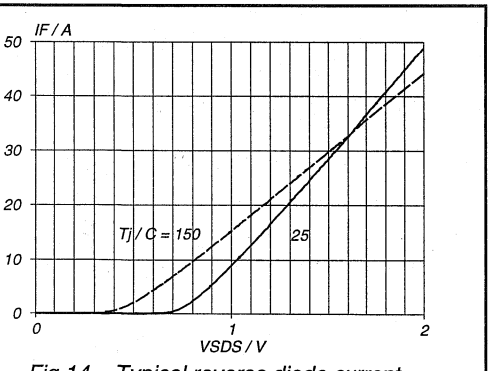


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ *V; parameter* T_j

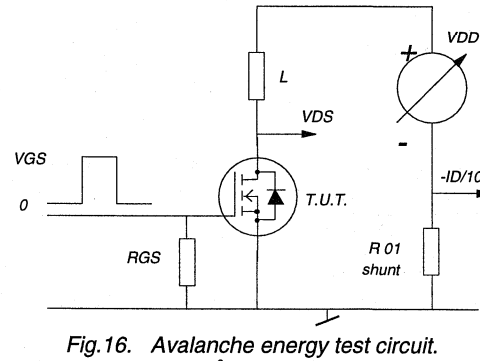


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK553-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

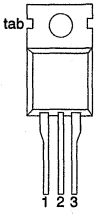
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK553	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	13	12	A
P_{tot}	Total power dissipation	75	75	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.18	0.22	Ω

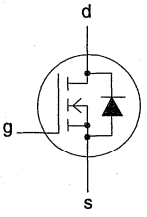
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	13	12	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	9	8.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	52	48	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK553-100A**	-	0.17	0.18	Ω
		I_D = 6.5 A **BUK553-100B**	-	0.20	0.22	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6.5 A	6.0	8.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	825	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	90	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	90	115	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 13 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	70	mJ

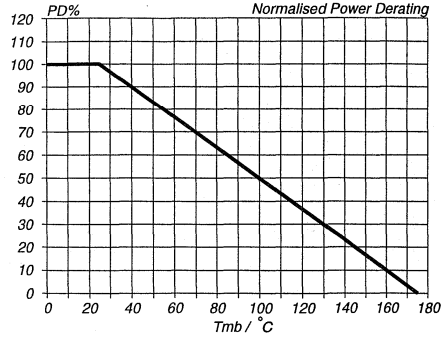


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

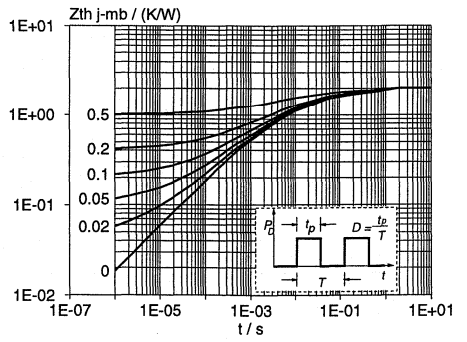


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

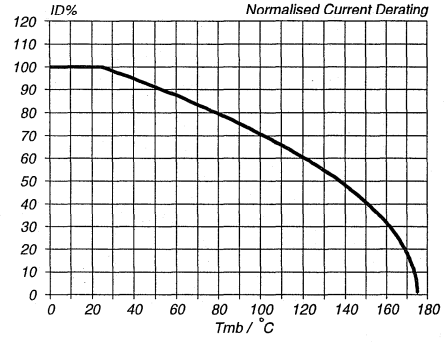


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

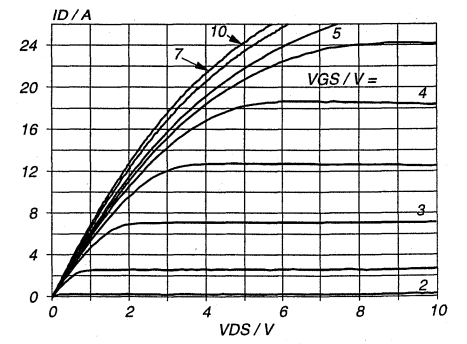


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

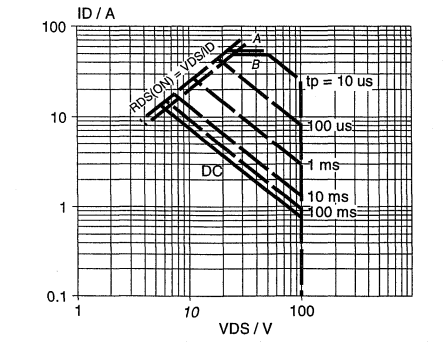


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

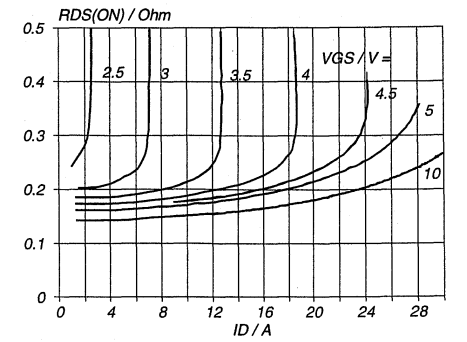


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

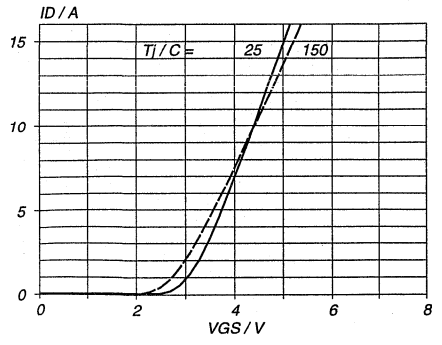


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

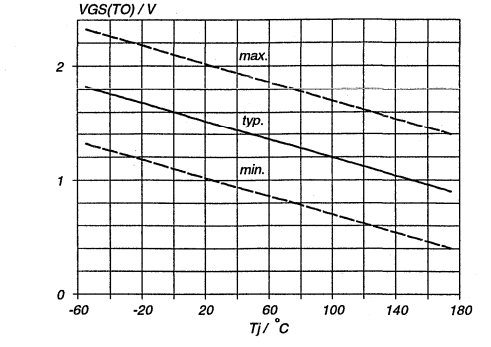


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

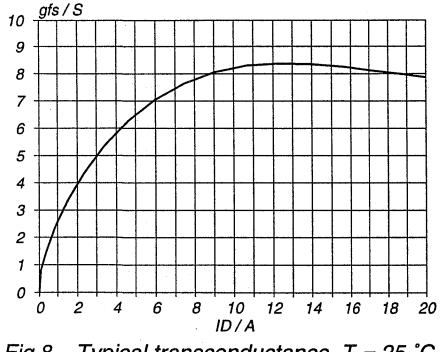


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

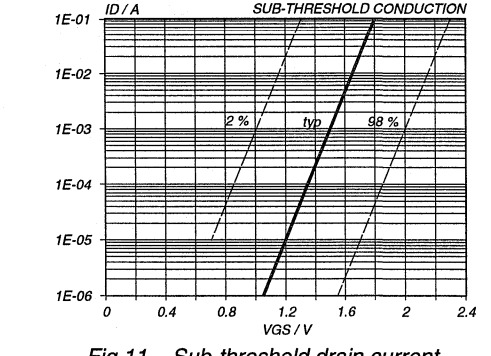


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

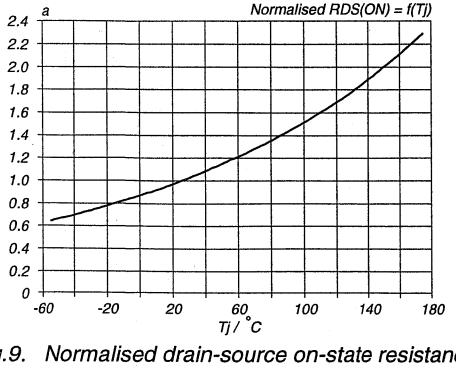


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 6.5$ A; $V_{GS} = 5$ V

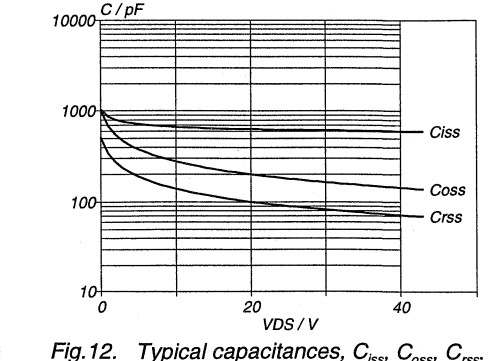


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

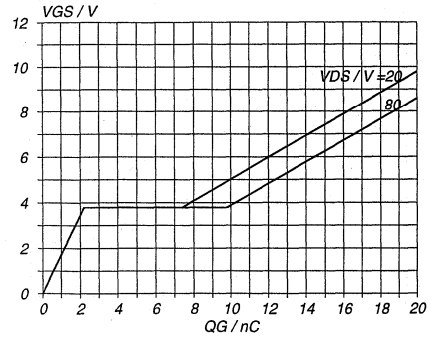


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 13 A; parameter V_{DS}

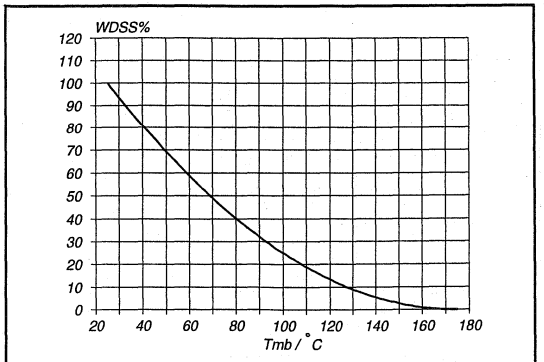


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: I_D = 13 A

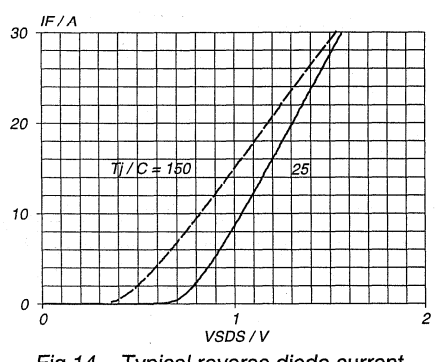


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

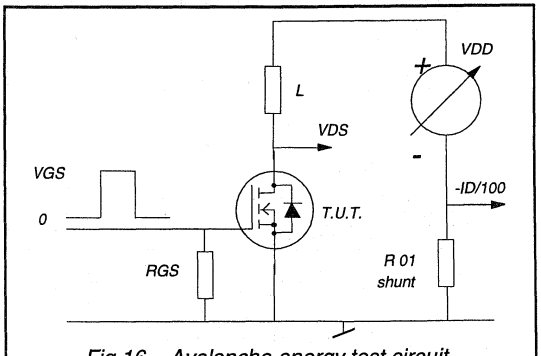


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK554-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope
The device is intended for use in automotive and general purpose switching applications.

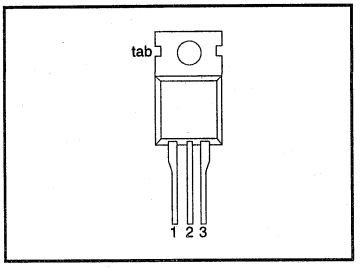
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	39	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	42	mΩ

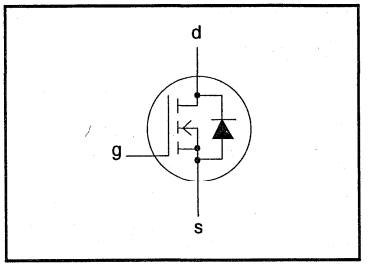
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	39	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	156	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	35	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	10	18	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	1750	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	110	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	150	220	ns
t_f	Turn-off fall time		-	100	145	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	39	A
I_{DRM}	Pulsed reverse drain current	-	-	-	156	A
V_{SD}	Diode forward voltage	I_F = 39 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 39 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 39 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

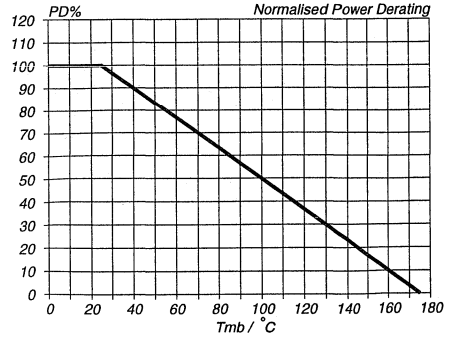


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

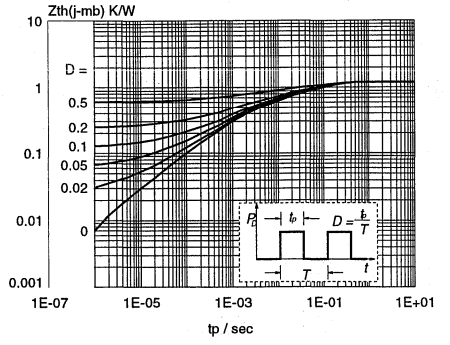


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

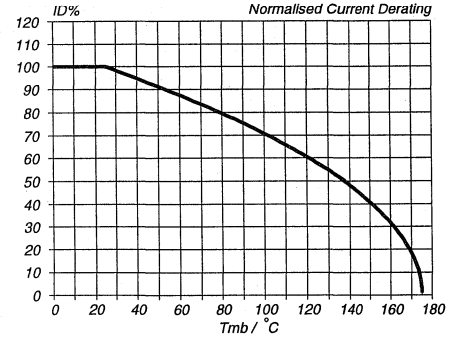


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

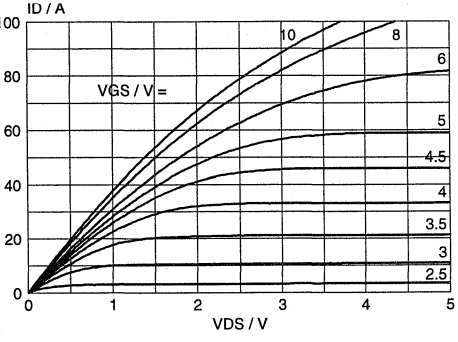


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

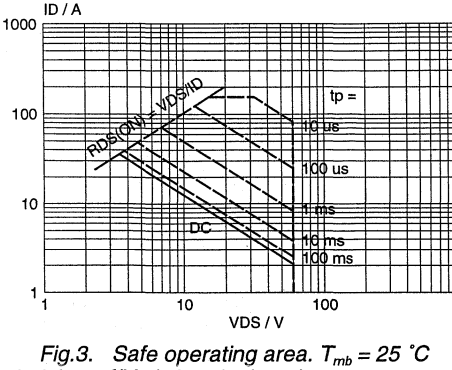


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

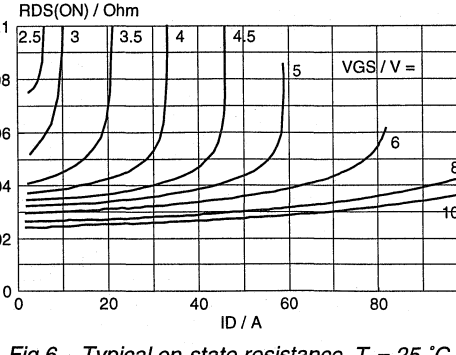


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

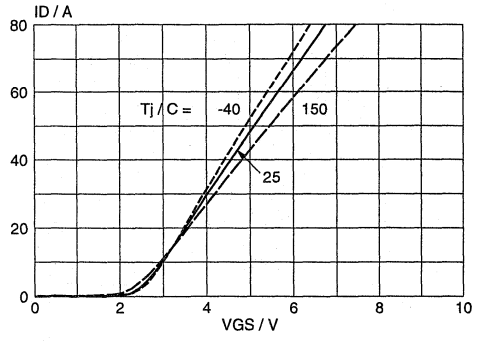


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

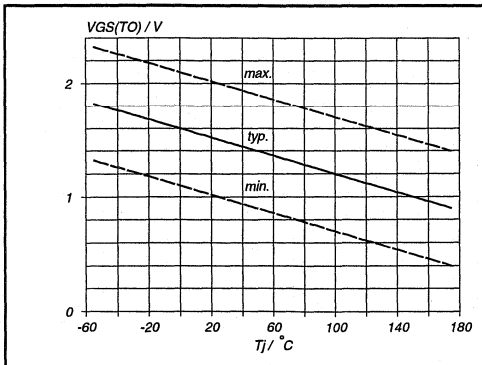


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

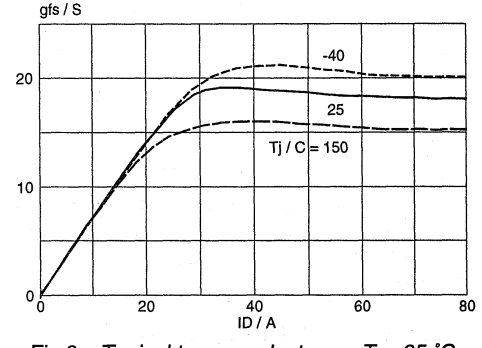


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

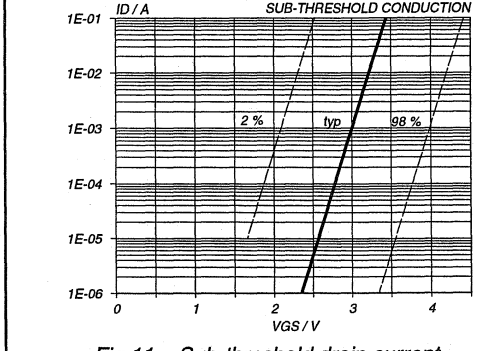


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

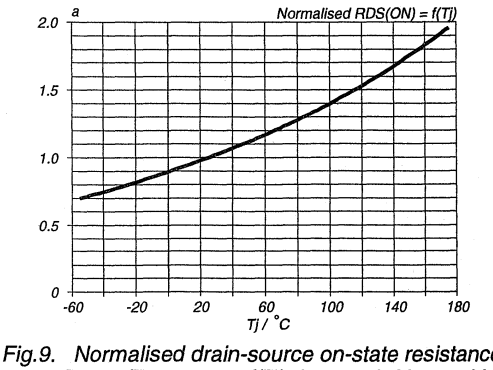


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

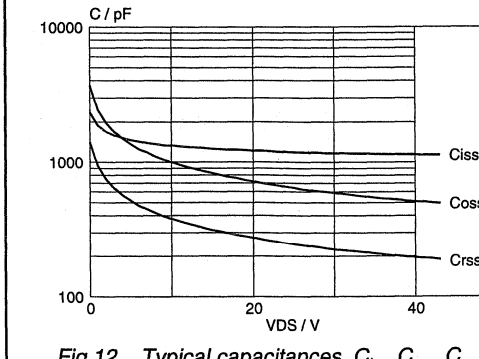


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

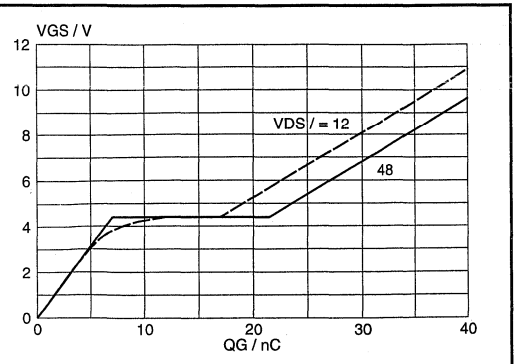


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 39$ A; parameter V_{DS}

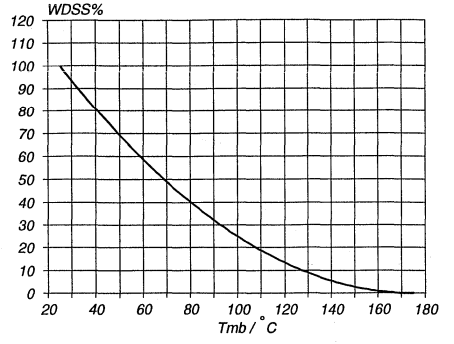


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 39$ A

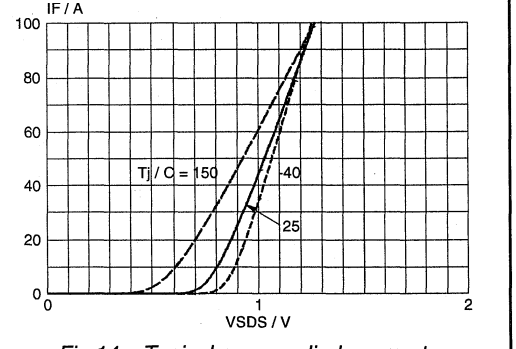


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

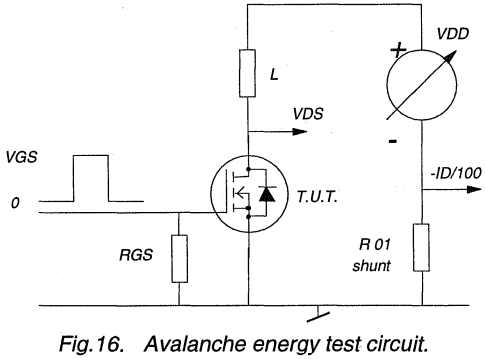


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK554-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

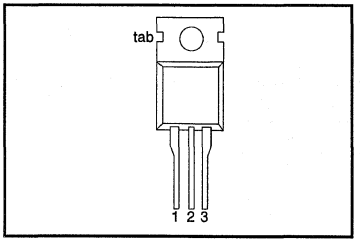
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK554	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	9.2	8.2	A
P_{tot}	Total power dissipation	90	90	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.4	0.5	Ω

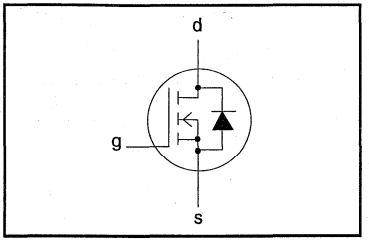
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-200A	-200B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	8.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	5.8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	33	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK554-200A**	-	0.35	0.4	Ω
		I_D = 3.5 A **BUK554-200B**	-	0.4	0.5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	6.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	800	1000	pF
C_{oss}	Output capacitance		-	120	160	pF
C_{rss}	Feedback capacitance		-	65	90	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	16	30	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	75	110	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	120	180	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; V_{DD} ≤ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	50	mJ

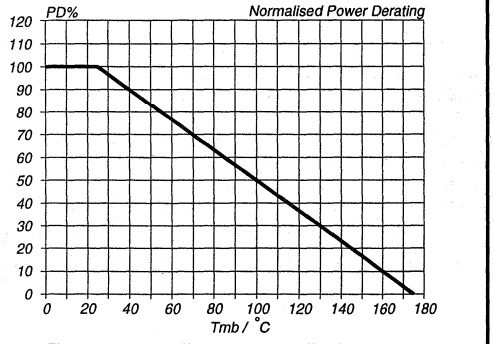


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\,25\,°C} = f(T_{mb})$

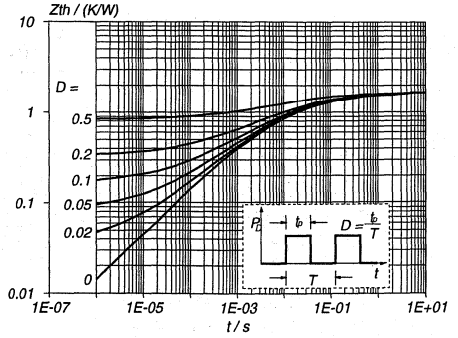


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

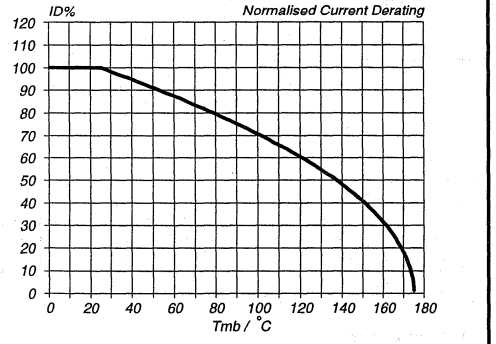


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\,25\,°C} = f(T_{mb})$; *conditions:* $V_{GS} \geq 5$ *V*

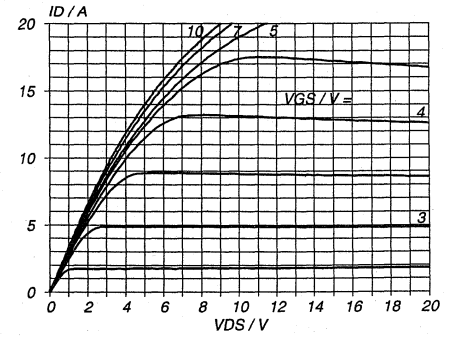


Fig.5. Typical output characteristics, $T_j = 25$ *°C.*
$I_D = f(V_{DS})$; *parameter* V_{GS}

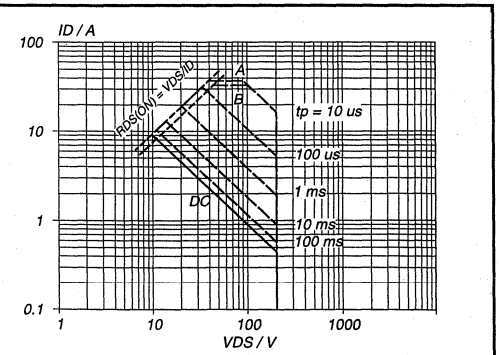


Fig.3. Safe operating area. $T_{mb} = 25$ *°C*
I_D *&* $I_{DM} = f(V_{DS})$; I_{DM} *single pulse; parameter* t_p

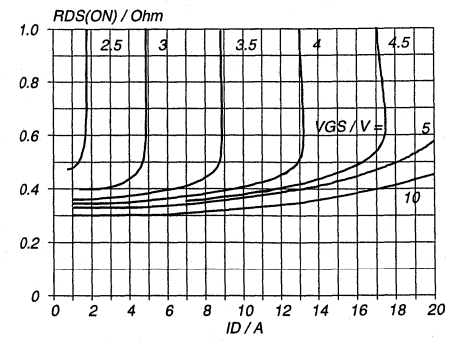


Fig.6. Typical on-state resistance, $T_j = 25$ *°C.*
$R_{DS(ON)} = f(I_D)$; *parameter* V_{GS}

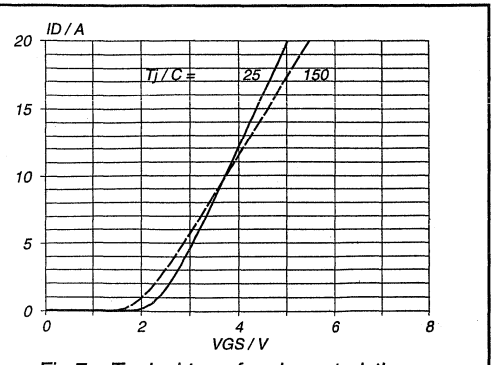


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

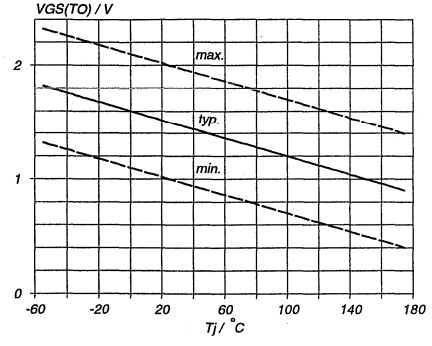


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

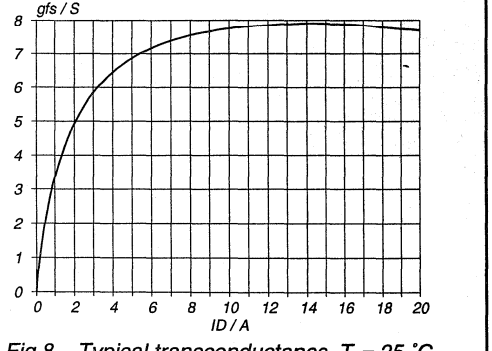


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

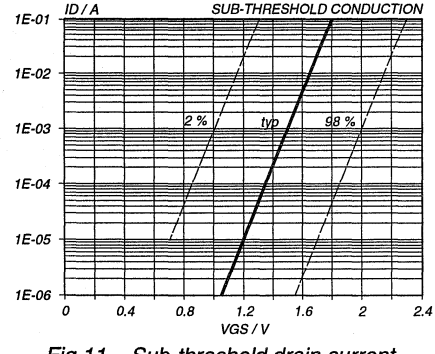


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

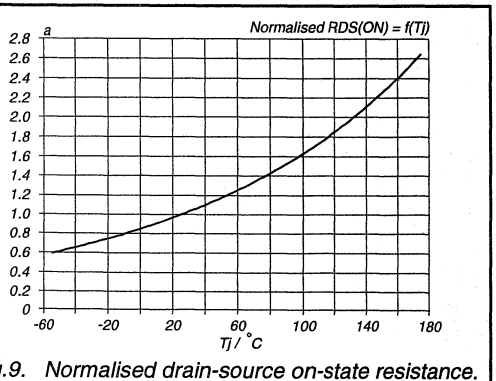


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 5 V

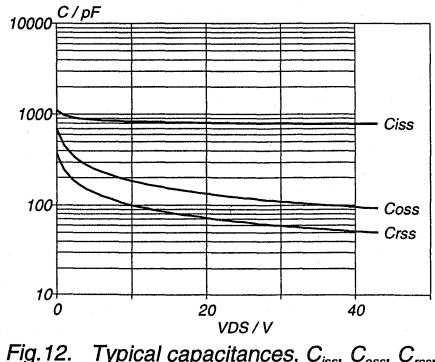


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

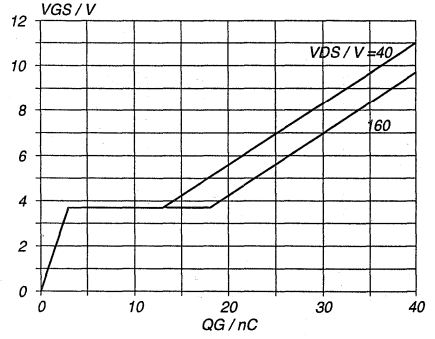


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9.2$ A; parameter V_{DS}

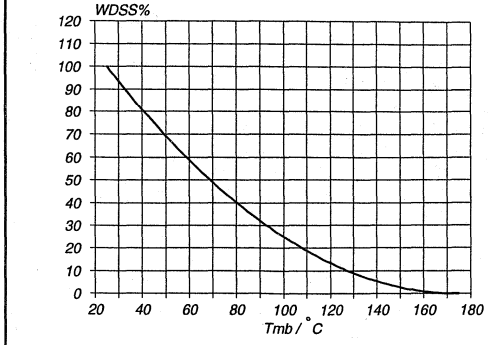


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

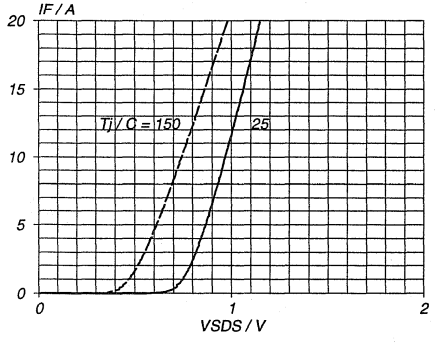


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

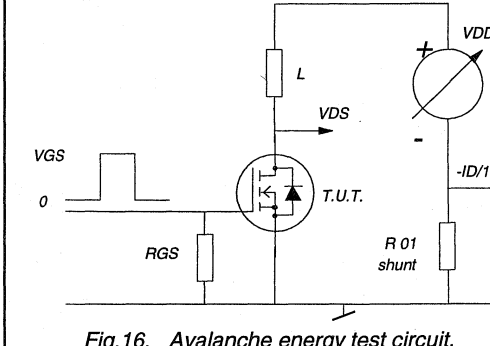


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK555-60A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

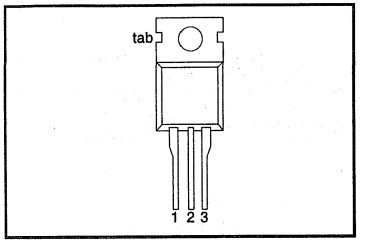
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK555	-60A	-60B	
V_{DS}	Drain-source voltage	60	60	V
I_D	Drain current (DC)	39	35	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.042	0.055	Ω

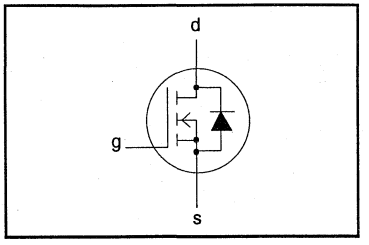
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	60		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-60A	-60B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	39	35	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	25	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	156	140	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK555-60A**	-	0.035	0.042	Ω
		I_D = 20 A **BUK555-60B**	-	0.045	0.055	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	11	20	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	220	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	120	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	160	220	ns
t_f	Turn-off fall time		-	110	145	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	39	A
I_{DRM}	Pulsed reverse drain current	-	-	-	156	A
V_{SD}	Diode forward voltage	I_F = 39 A ; V_{GS} = 0 V	-	1.4	2.0	V
t_{rr}	Reverse recovery time	I_F = 39 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 39 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

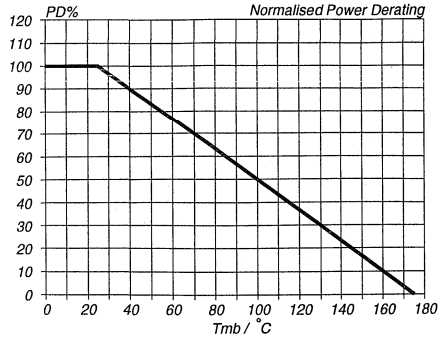


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

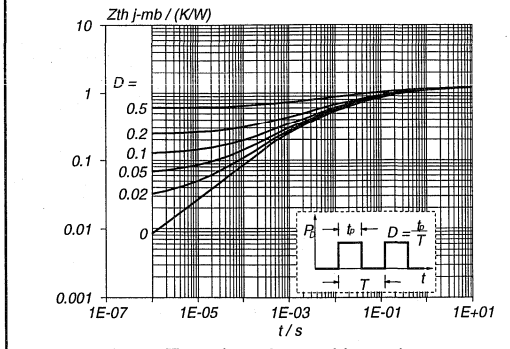


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

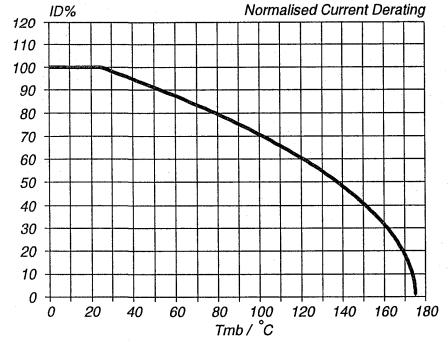


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

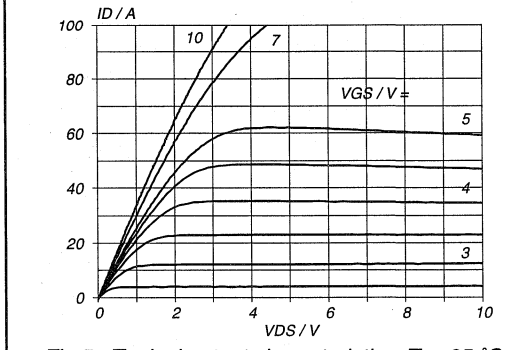


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

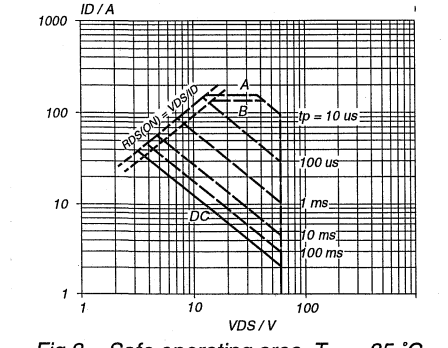


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

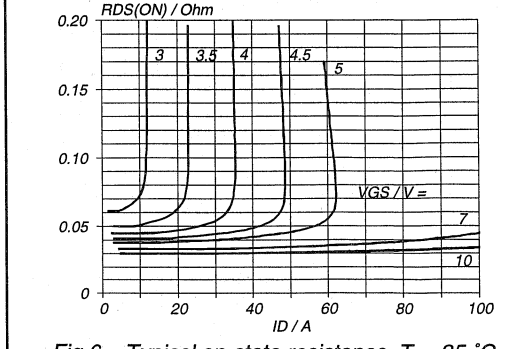


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

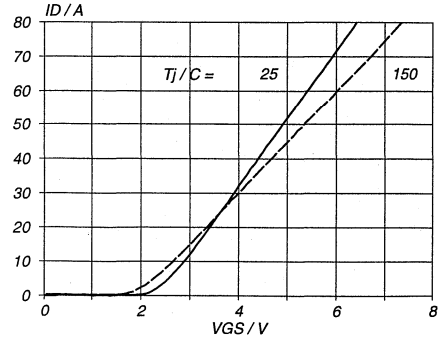


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

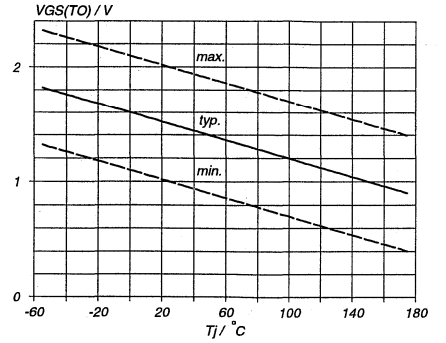


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

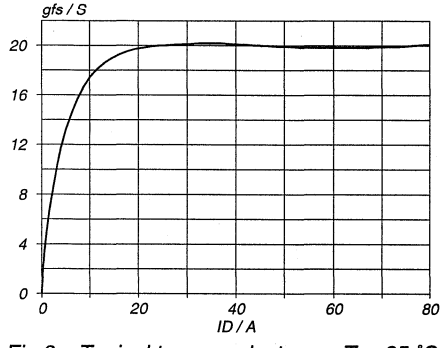


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

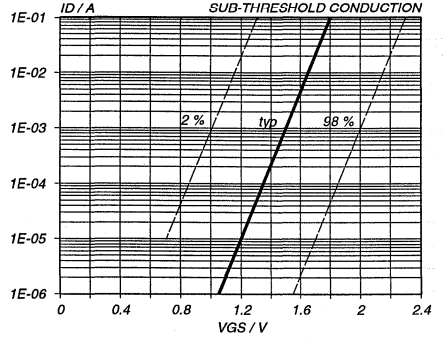


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

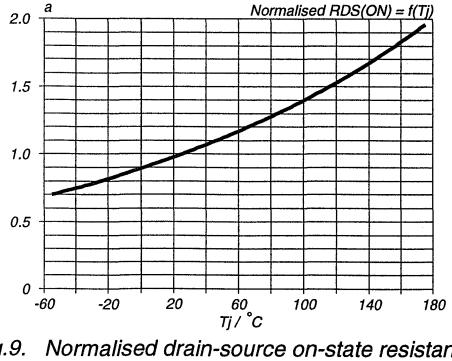


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; $I_D = 20$ A; $V_{GS} = 5$ V

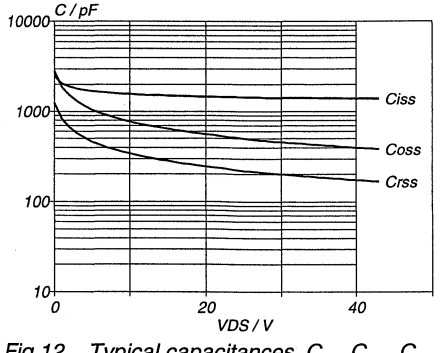


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

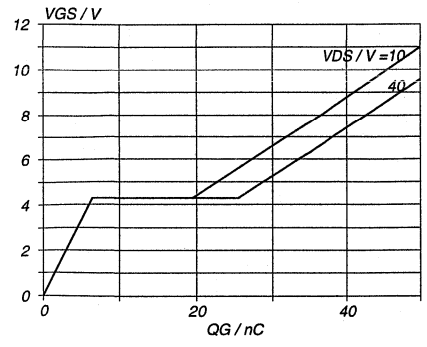


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 39$ A; parameter V_{DS}

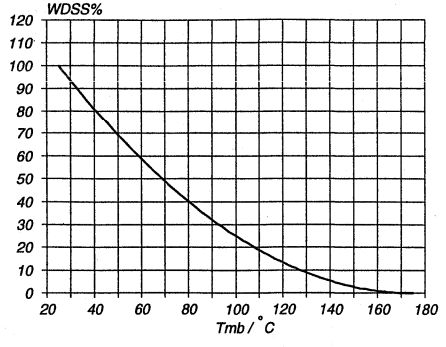


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 39$ A

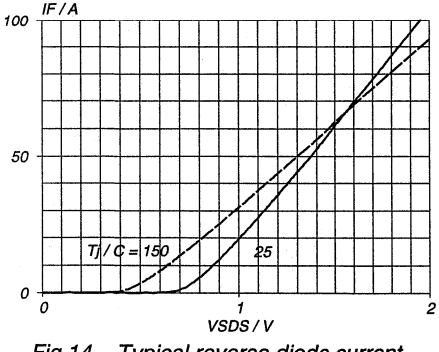


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

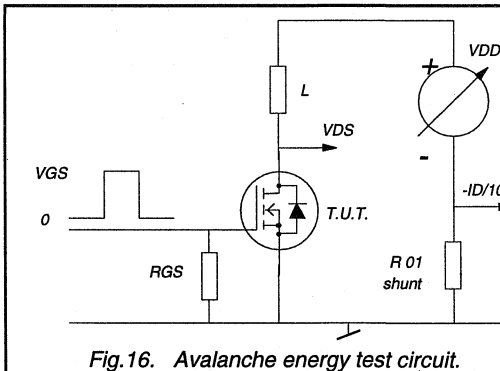


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Logic level FET

BUK555-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope.
The device is intended for use in Automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

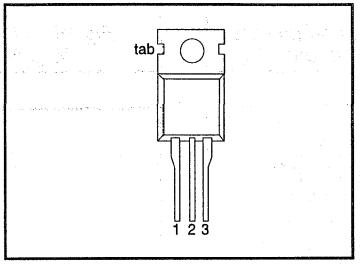
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	41	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	38	mΩ

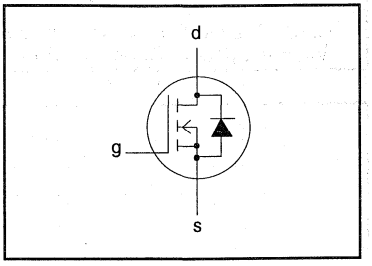
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	25	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	11	20	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1200	1750	pF
C_{oss}	Output capacitance		-	470	600	pF
C_{rss}	Feedback capacitance		-	180	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	120	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	160	220	ns
t_f	Turn-off fall time		-	110	145	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

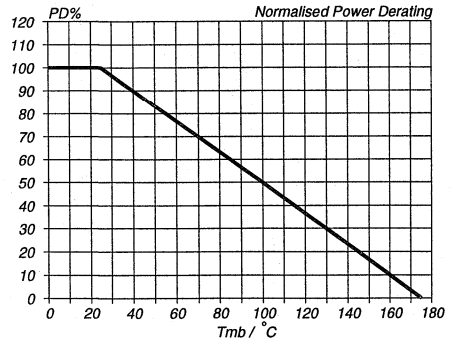


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

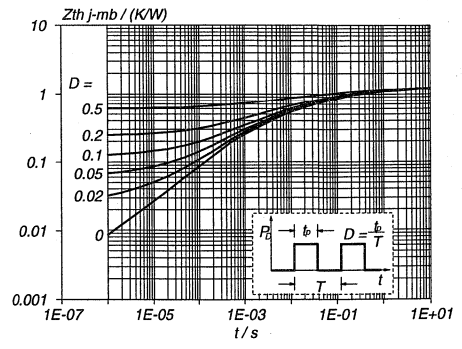


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

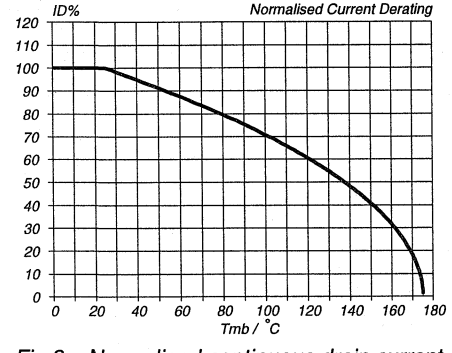


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

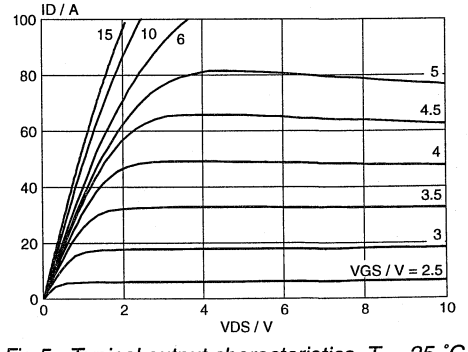


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

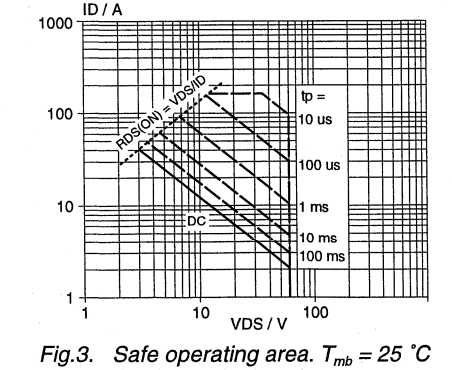


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

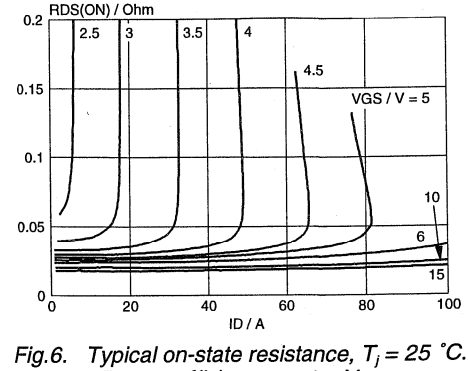


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

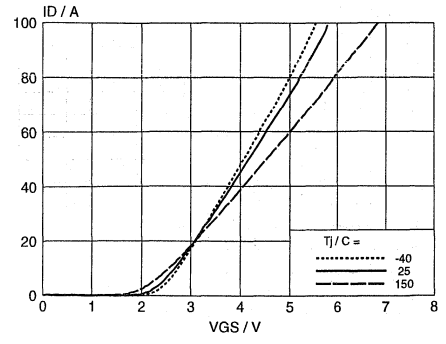


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

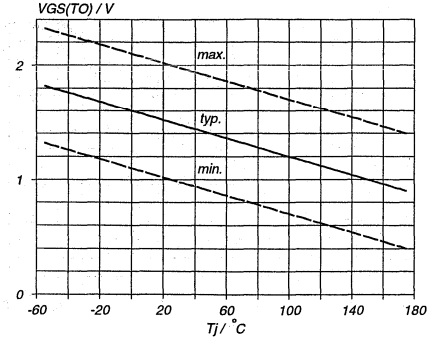


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

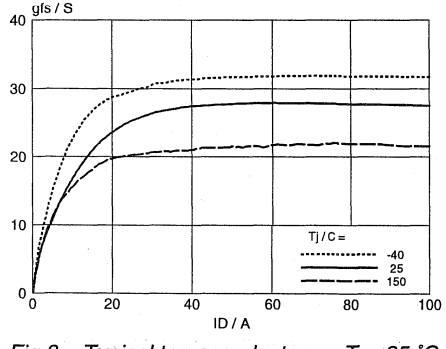


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V

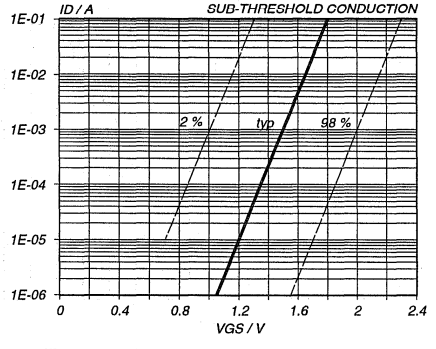


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

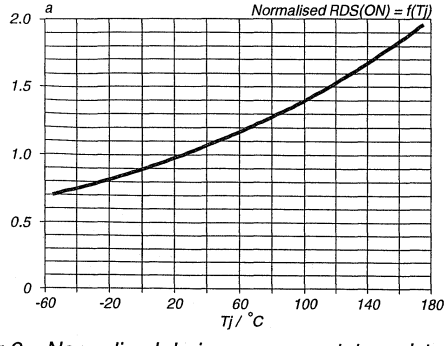


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

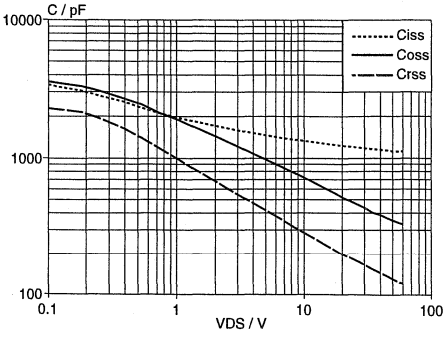


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

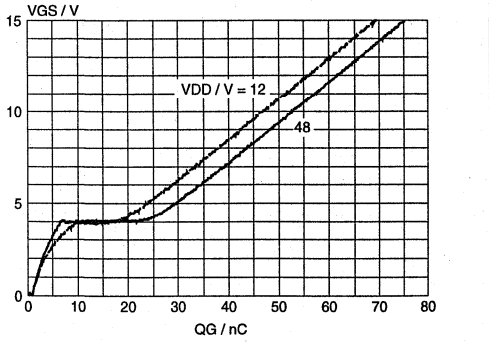


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

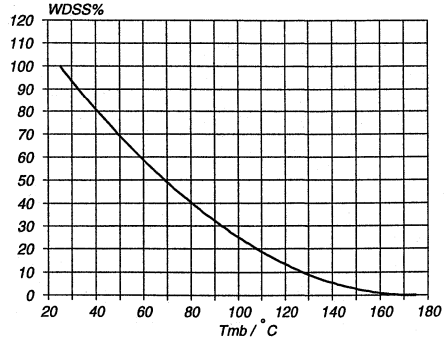


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

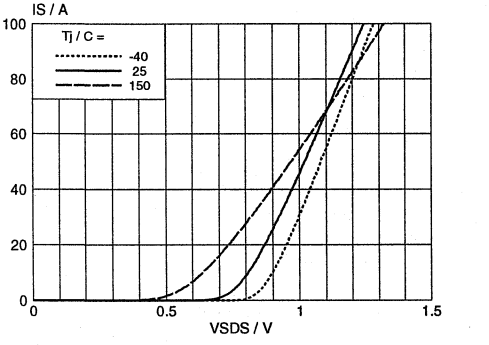


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

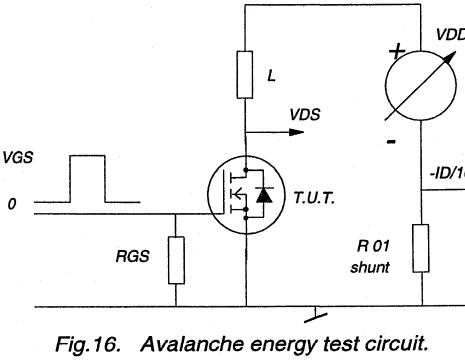


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK555-100A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

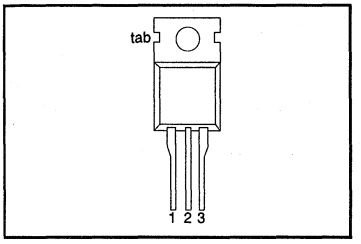
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK555	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	25	22	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5$ V	0.085	0.11	Ω

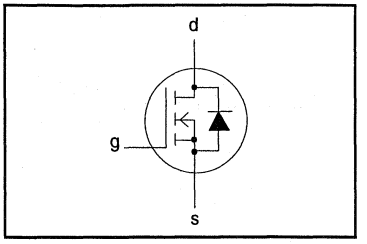
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	100		V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-100A	-100B	
I_D	Drain current (DC)	T_{mb} = 25 °C	-	25	22	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	15	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	100	88	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK555-100A** I_D = 13 A **BUK555-100B**	- -	0.075 0.09	0.085 0.11	Ω Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	10	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	280	350	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	65	85	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	135	180	ns
t_f	Turn-off fall time		-	80	110	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	25	A
I_{DRM}	Pulsed reverse drain current	-	-	-	100	A
V_{SD}	Diode forward voltage	I_F = 25 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 25 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	140	mJ

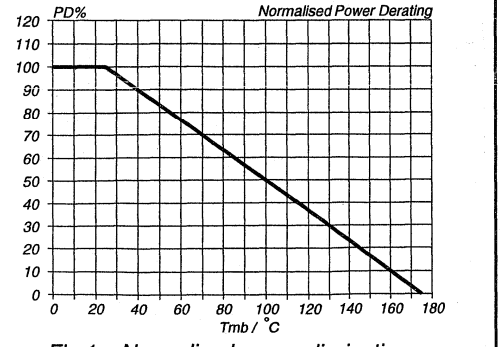


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

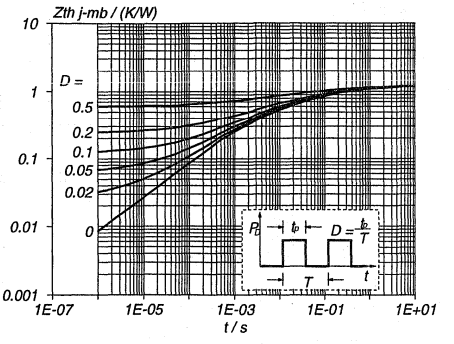


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

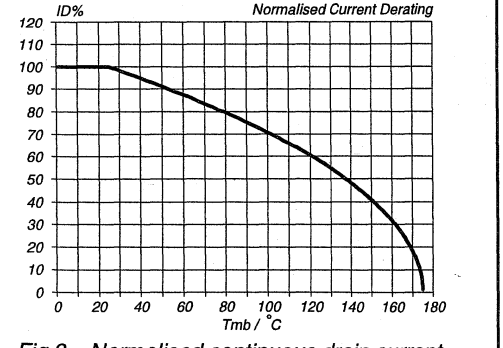


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

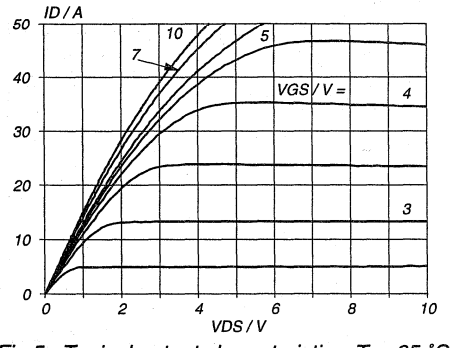


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

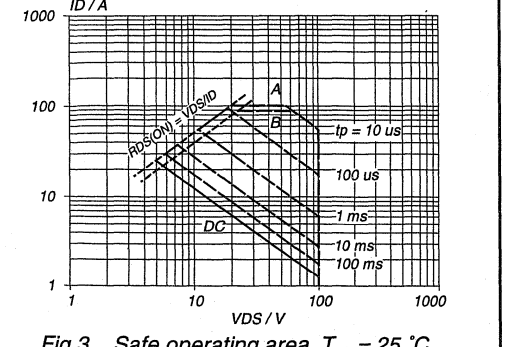


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

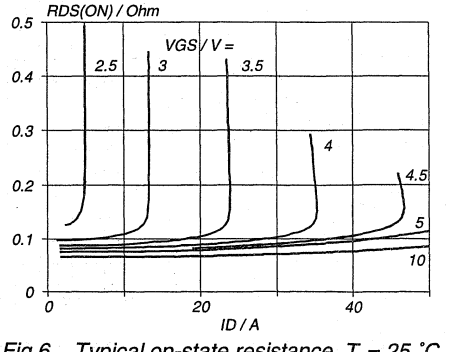


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

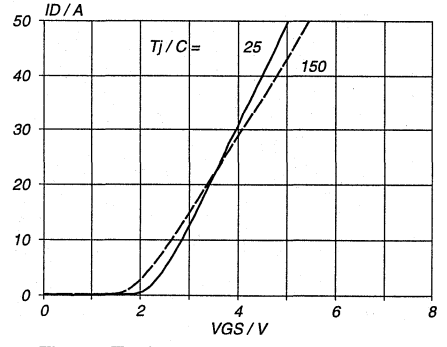


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

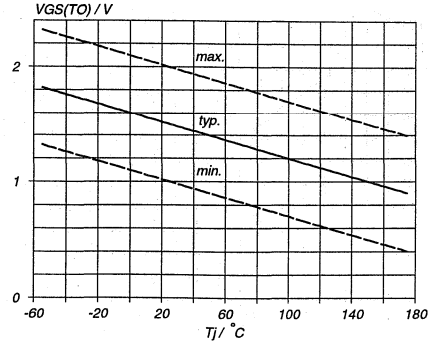


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

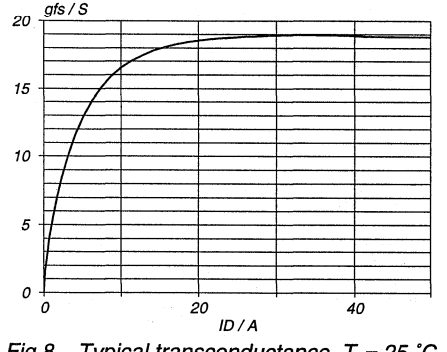


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

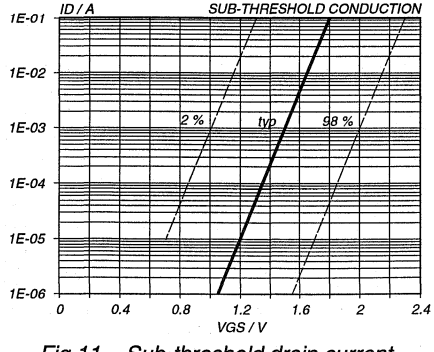


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

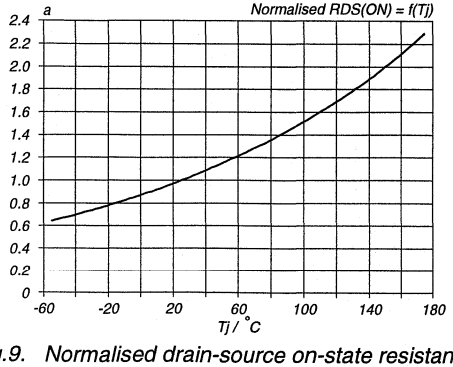


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 13 A; V_{GS} = 5 V

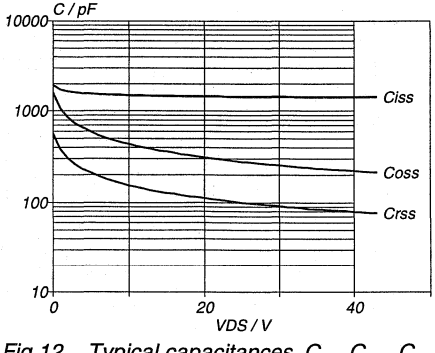


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

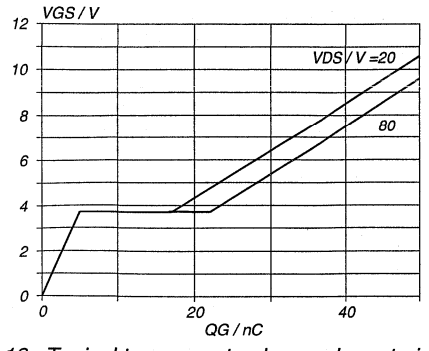


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 25$ A; parameter V_{DS}

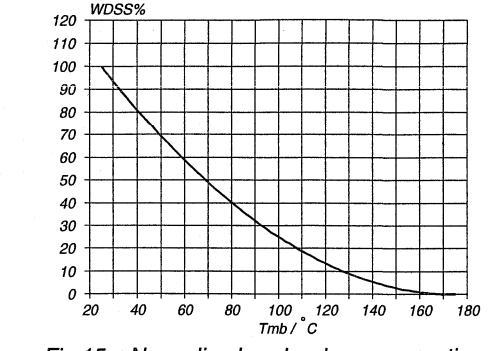


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 25$ A

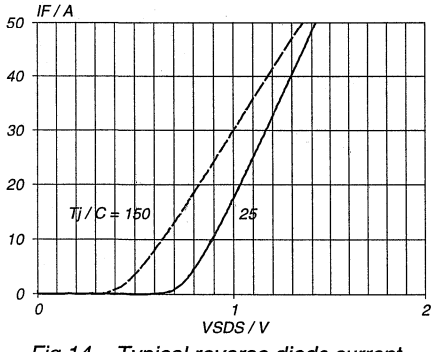


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

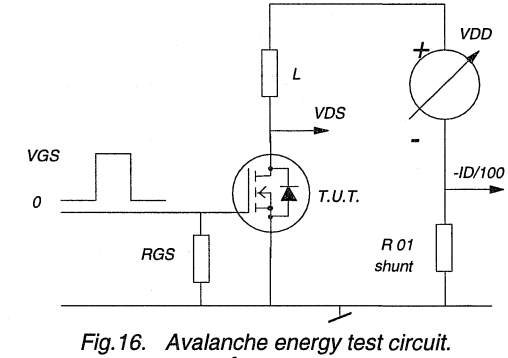


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK555-200A/B

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

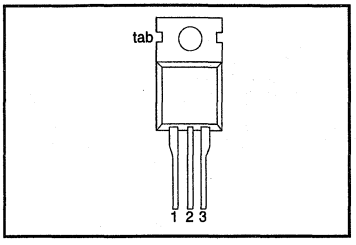
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK555	-200A	-200B	
V_{DS}	Drain-source voltage	200	200	V
I_D	Drain current (DC)	14	13	A
P_{tot}	Total power dissipation	125	125	W
T_j	Junction temperature	175	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5$ V	0.23	0.28	Ω

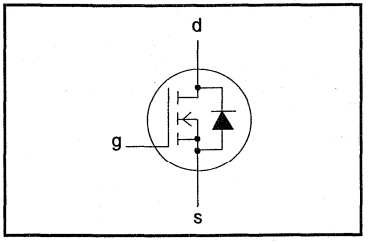
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
V_{DS}	Drain-source voltage	-	-	200		V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20$ kΩ	-	200		V
$\pm V_{GS}$	Gate-source voltage	-	-	15		V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20		V
				-200A	-200B	
I_D	Drain current (DC)	$T_{mb} = 25$ °C	-	14	13	A
I_D	Drain current (DC)	$T_{mb} = 100$ °C	-	10	9.2	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25$ °C	-	56	52	A
P_{tot}	Total power dissipation	$T_{mb} = 25$ °C	-	125		W
T_{stg}	Storage temperature	-	- 55	175		°C
T_j	Junction Temperature	-	-	175		°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; **BUK555-200A**	-	0.2	0.23	Ω
		I_D = 7 A **BUK555-200B**	-	0.24	0.28	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	8.0	15	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1600	2000	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	75	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	140	180	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	100	mJ

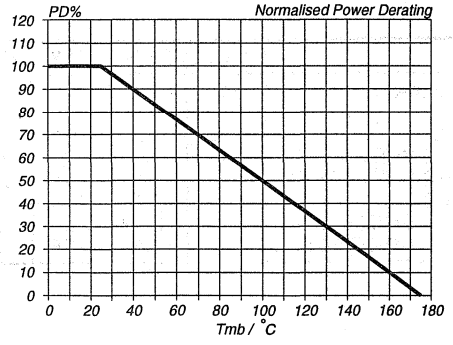


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

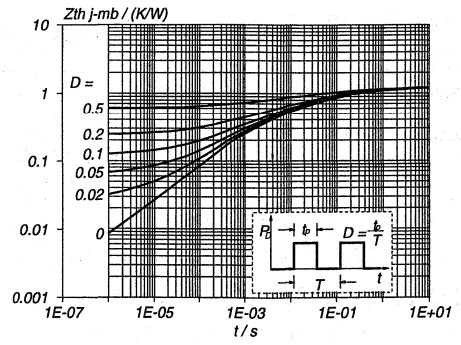


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

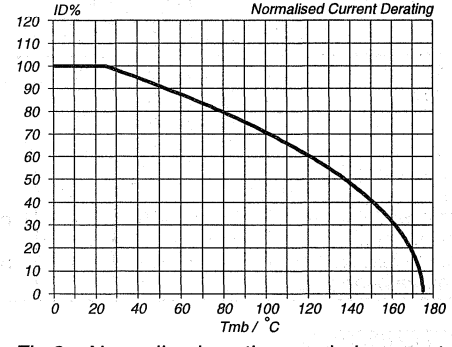


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

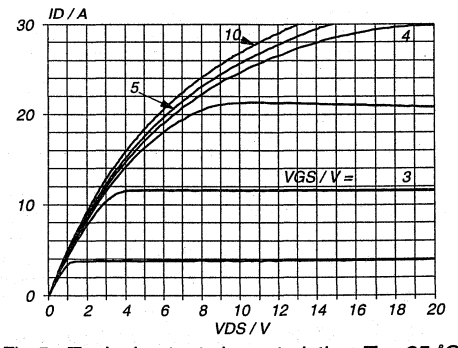


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

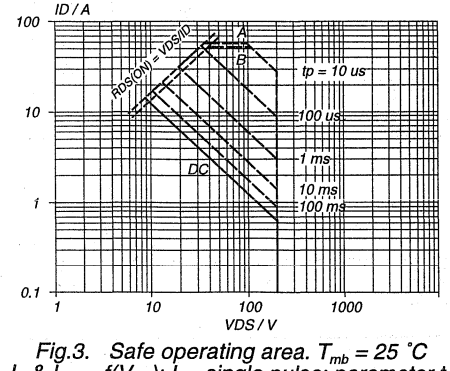


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

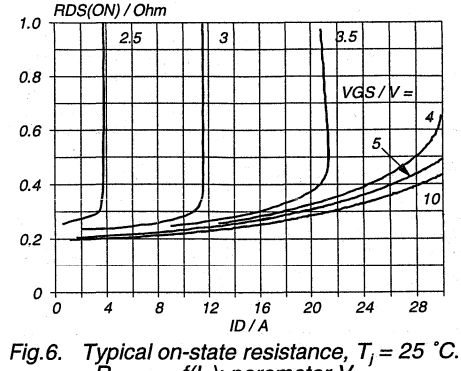


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

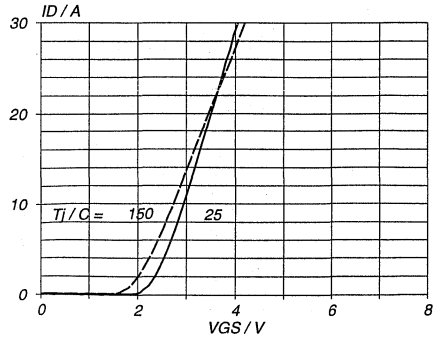


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

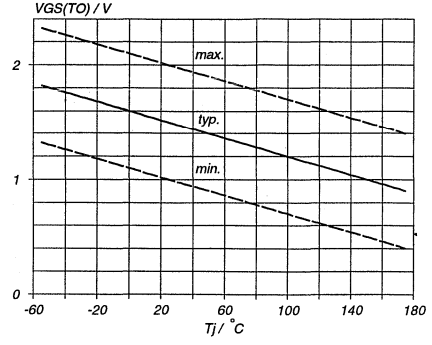


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

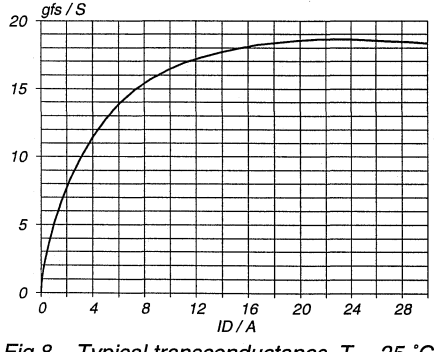


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

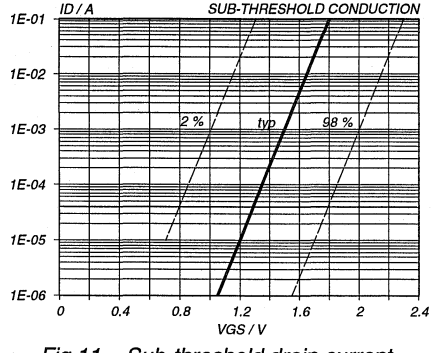


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

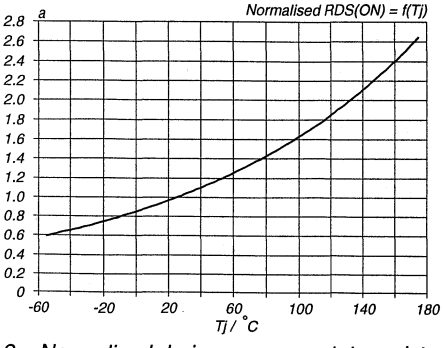


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 7$ A; $V_{GS} = 5$ V

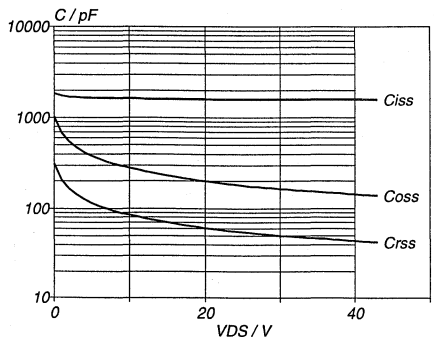


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

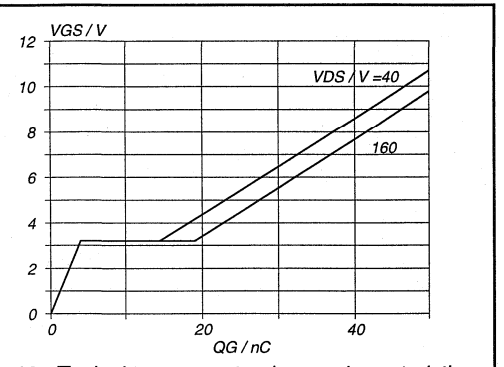


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

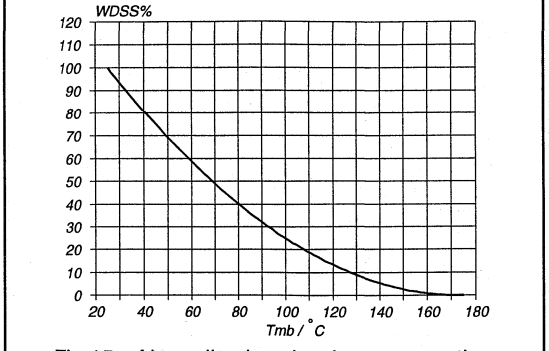


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

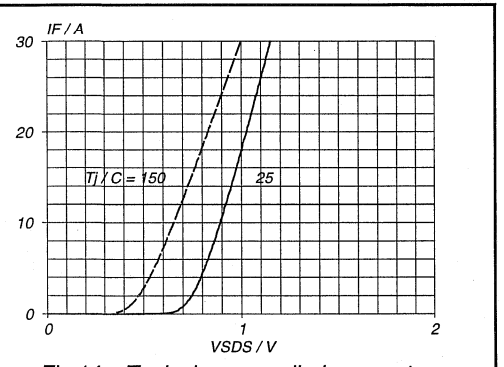


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

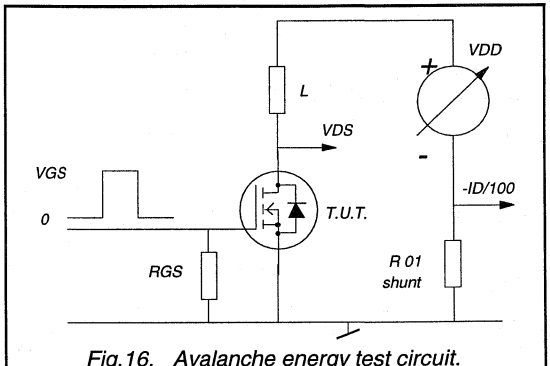


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK556-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

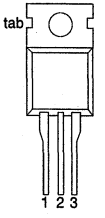
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	50	A
P_{tot}	Total power dissipation	150	W
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	26	mΩ

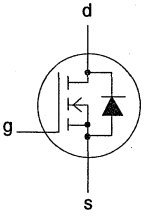
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	50	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	38	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	200	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	20	26	mΩ

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	17	30	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2800	pF
C_{oss}	Output capacitance		-	700	1000	pF
C_{rss}	Feedback capacitance		-	280	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	40	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V;	-	150	250	ns
$t_{d\,off}$	Turn-off delay time	R_{GS} = 50 Ω;	-	350	450	ns
t_f	Turn-off fall time	R_{gen} = 50 Ω	-	190	250	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	50	A
I_{DRM}	Pulsed reverse drain current	-	-	-	200	A
V_{SD}	Diode forward voltage	I_F = 50 A ; V_{GS} = 0 V	-	1.1	2.0	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	150	mJ

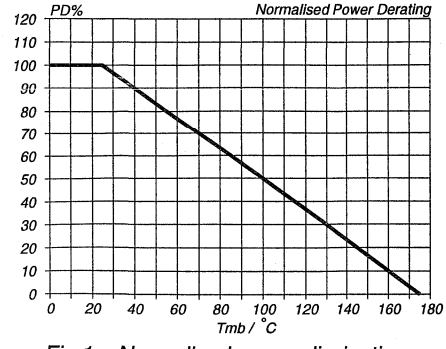


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

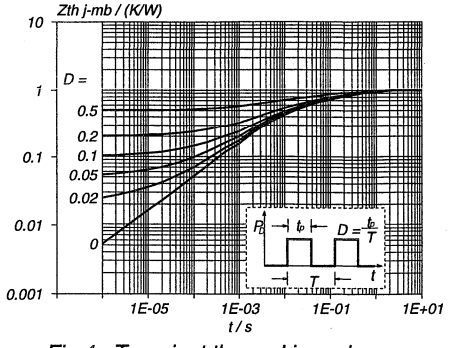


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

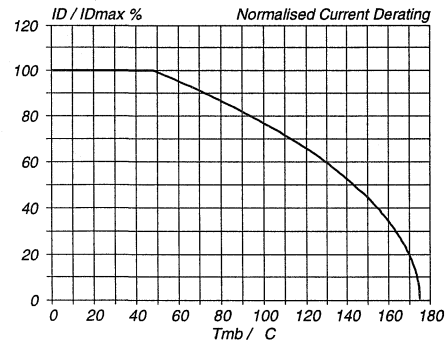


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

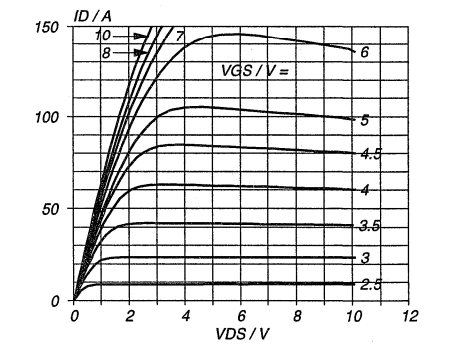


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

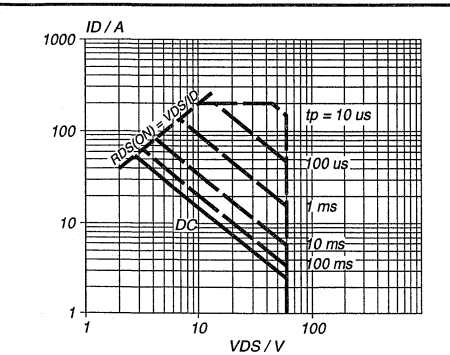


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

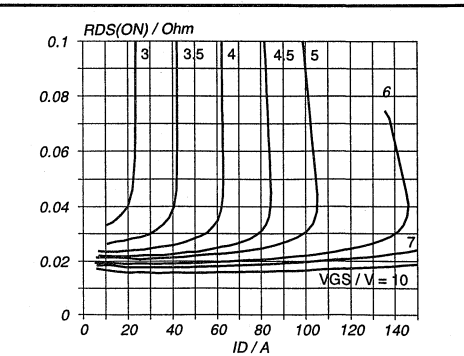


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

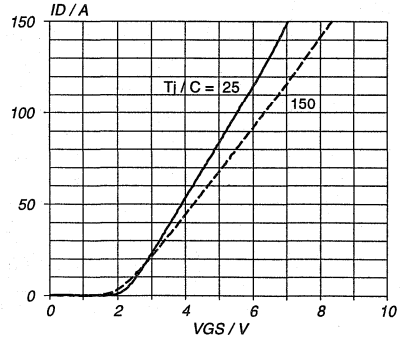


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

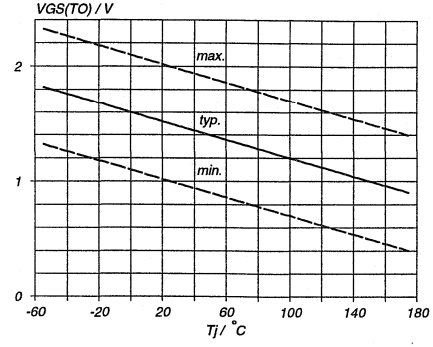


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

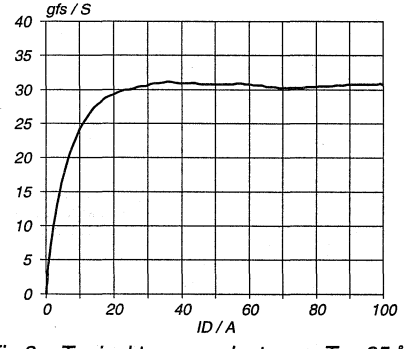


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 15$ V

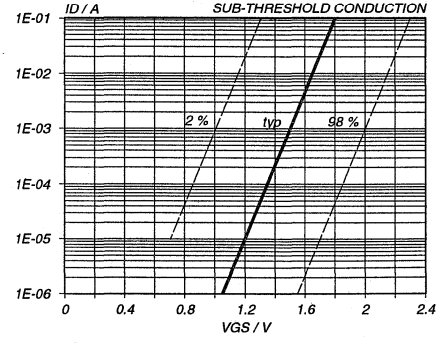


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

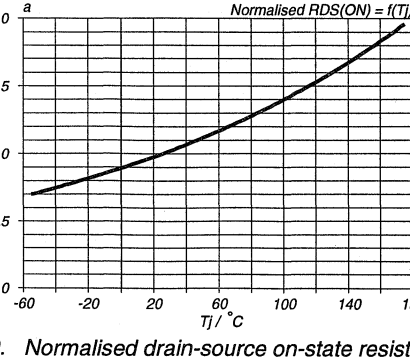


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 5$ V

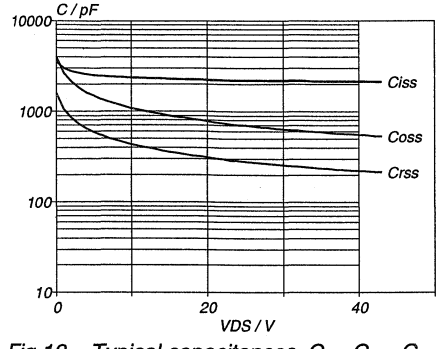


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

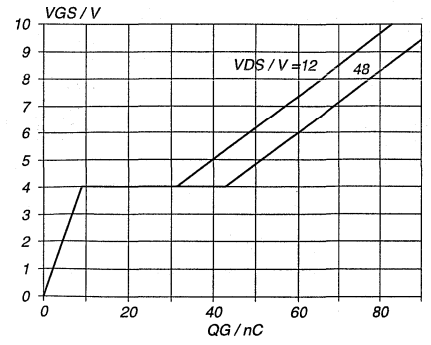


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

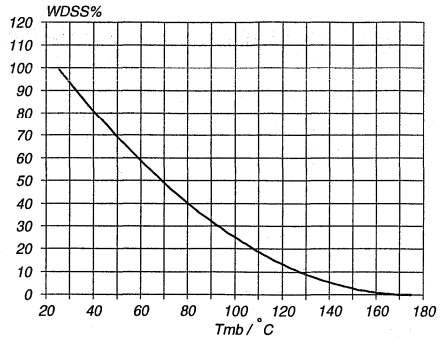


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 25$ A

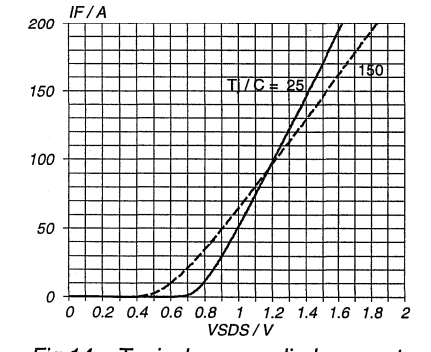


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

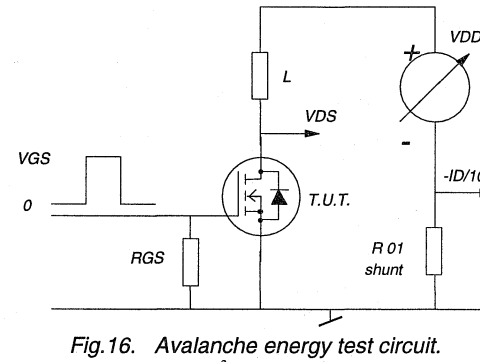


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK556-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope.
The device is intended for use in automotive and general purpose switching applications.

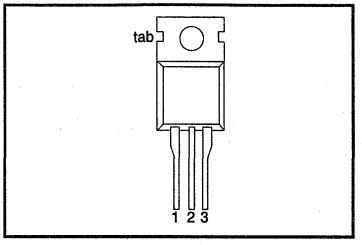
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	60	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	22	mΩ

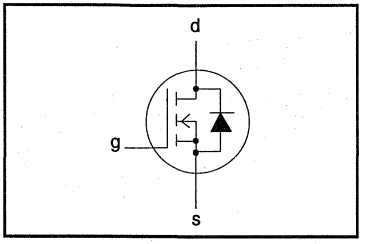
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	60	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	44	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	From junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	From junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	18	22	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	17	30	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2800	pF
C_{oss}	Output capacitance		-	700	1000	pF
C_{rss}	Feedback capacitance		-	280	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	40	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	150	250	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	350	450	ns
t_f	Turn-off fall time		-	190	250	ns
L_d	internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	60	A
I_{DRM}	Pulsed reverse drain current	-	-	-	240	A
V_{SD}	Diode forward voltage	I_F = 50 A; V_{GS} = 0 V	-	1.1	2.0	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; V_{DD} ≤ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	150	mJ

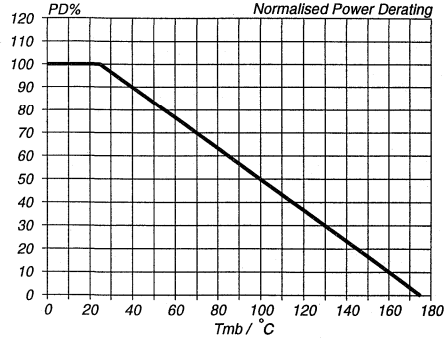


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

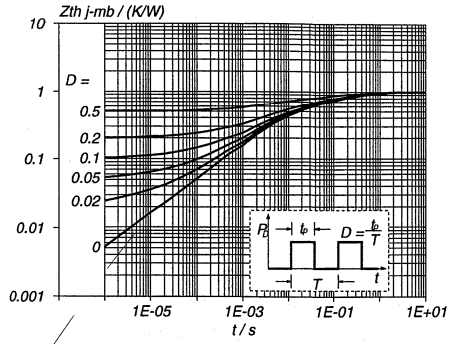


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

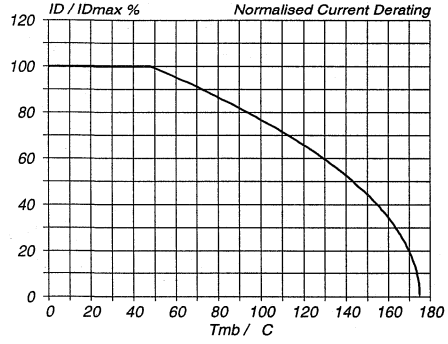


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

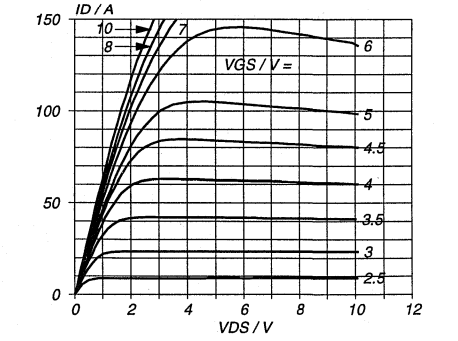


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

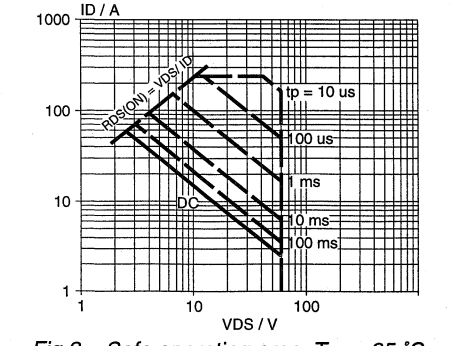


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

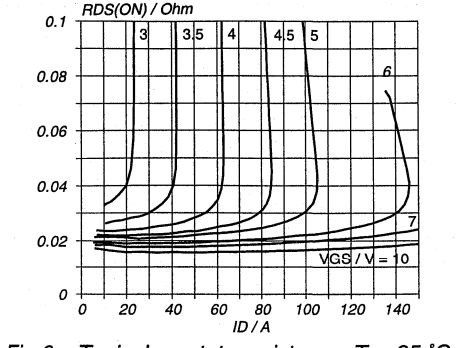


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

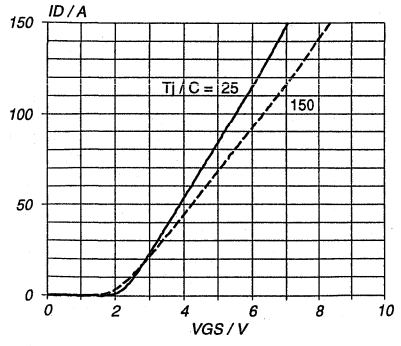


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

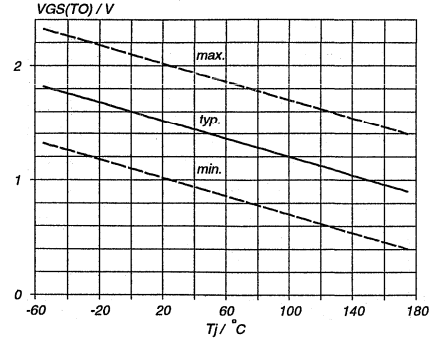


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

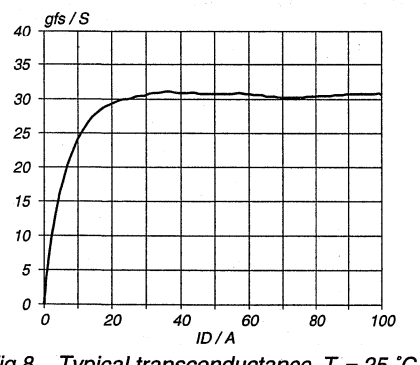


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

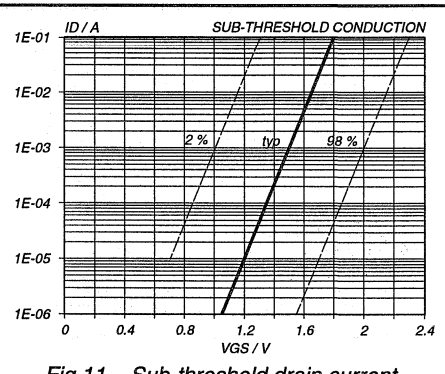


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

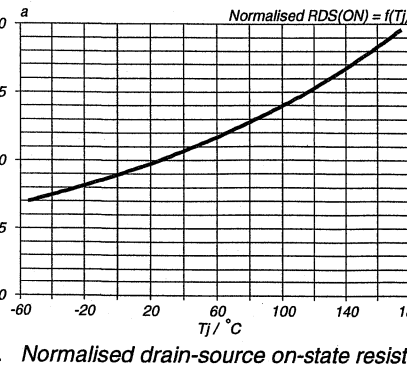


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

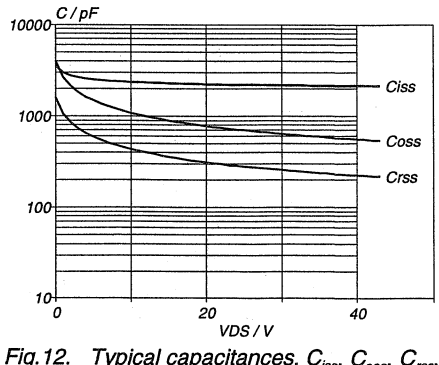


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

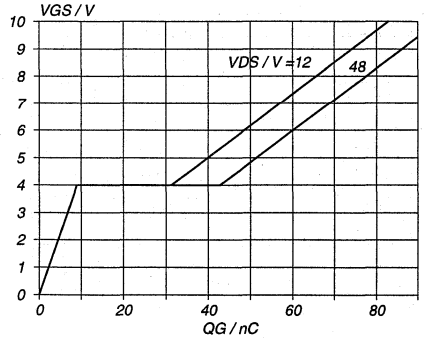


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

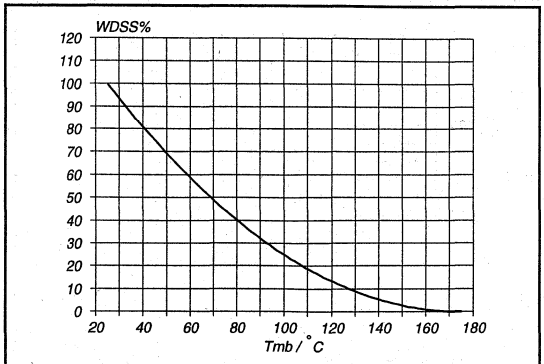


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 50$ A

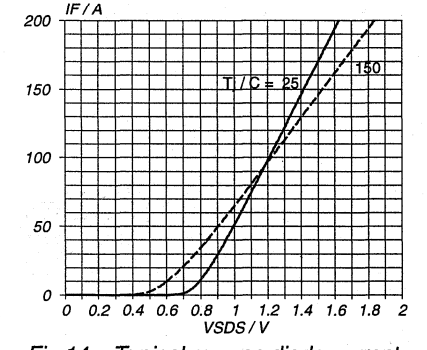


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

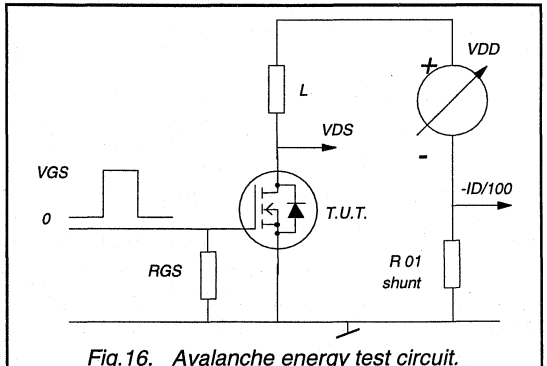


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK562-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

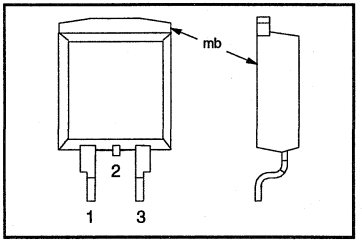
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.15	Ω

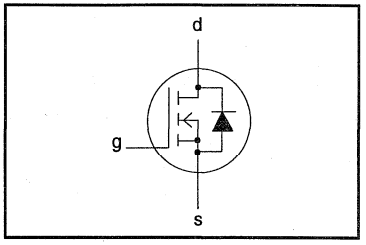
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 8.5 A	-	0.12	0.15	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	5	6.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	65	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	60	80	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	45	70	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

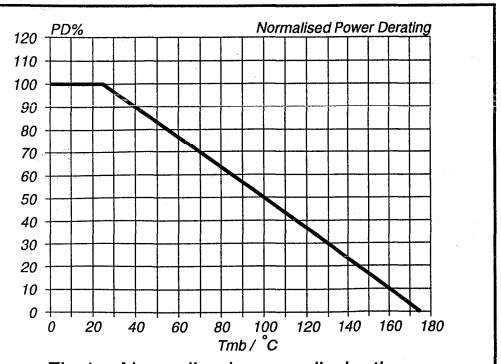


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

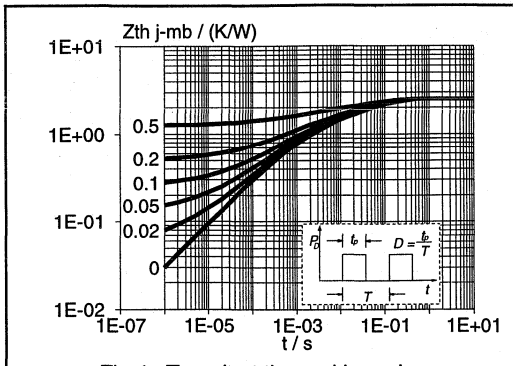


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

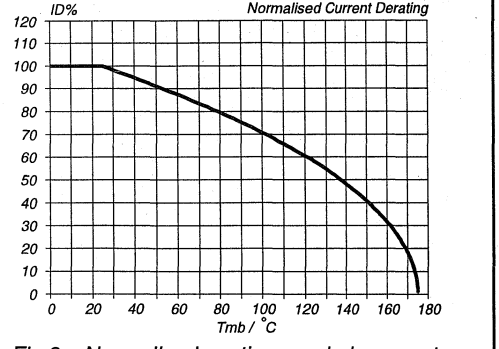


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

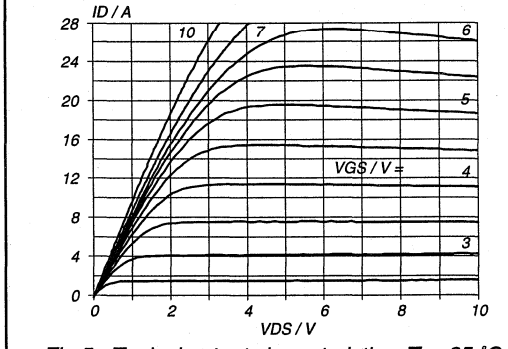


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

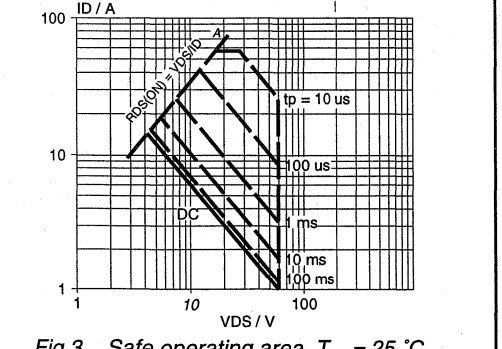


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

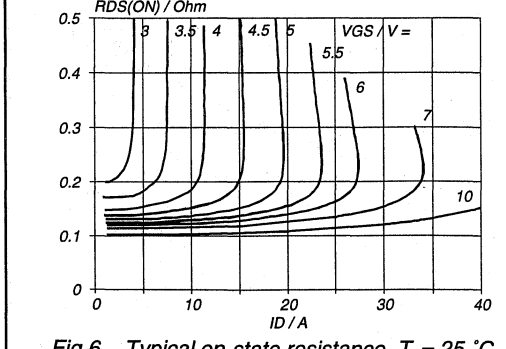


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

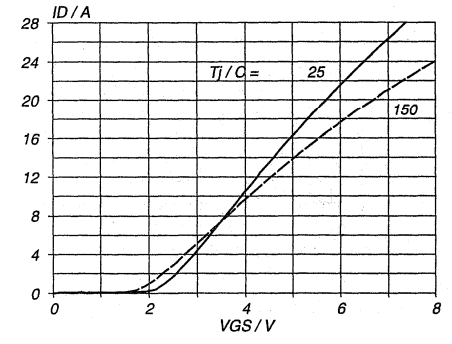


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

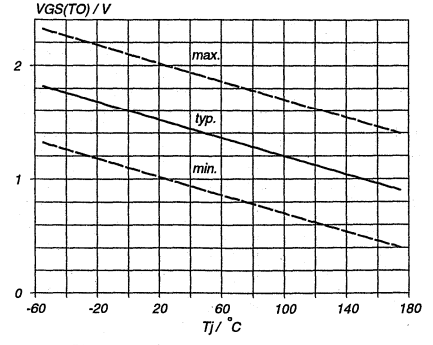


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

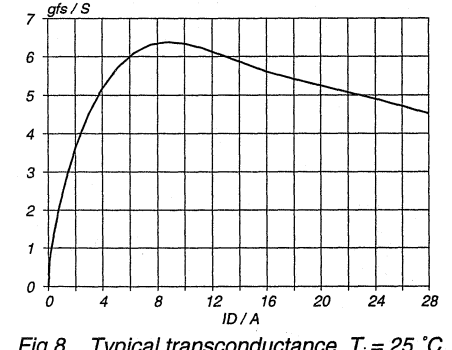


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

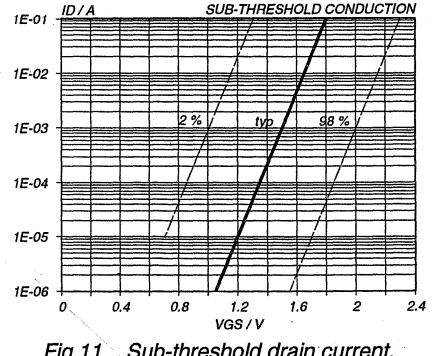


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

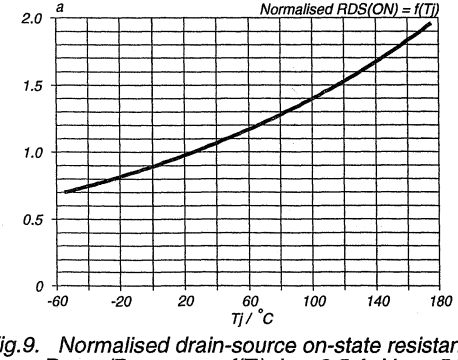


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 8.5 A; V_{GS} = 5 V

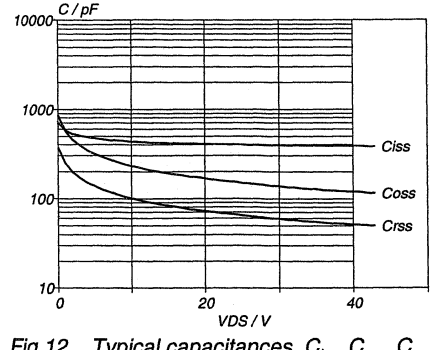


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

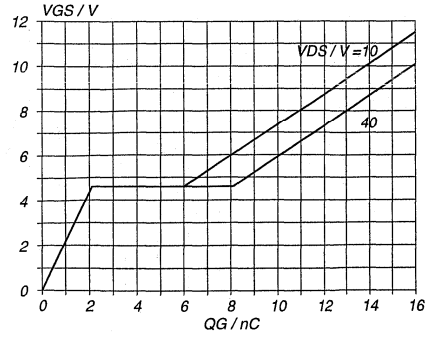


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

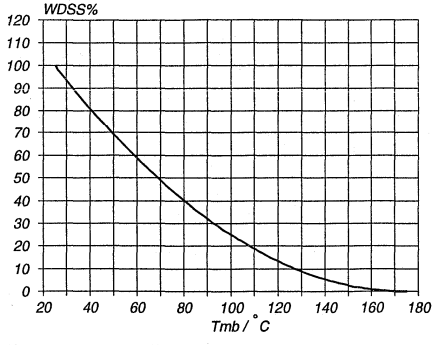


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

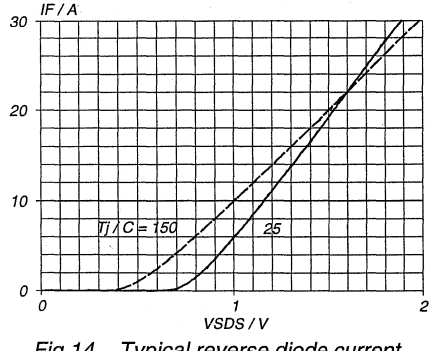


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

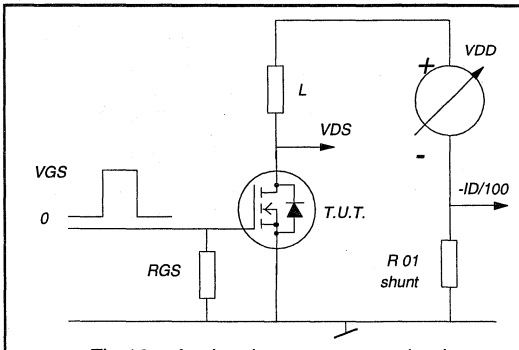


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK562-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

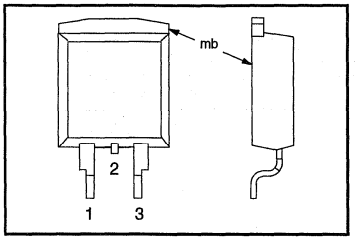
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	10	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.28	Ω

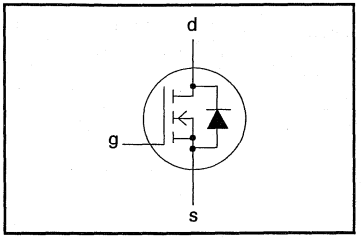
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	10	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 5.5 A	-	0.25	0.28	Ω Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	4.5	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	10	A
I_{DRM}	Pulsed reverse drain current	-	-	-	40	A
V_{SD}	Diode forward voltage	I_F = 10 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	30	mJ

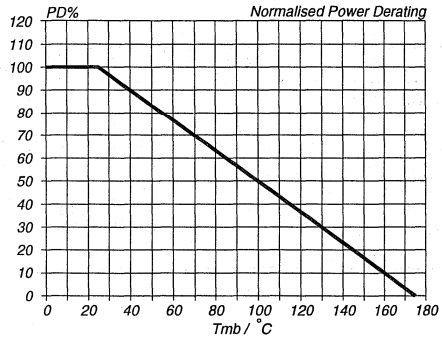


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

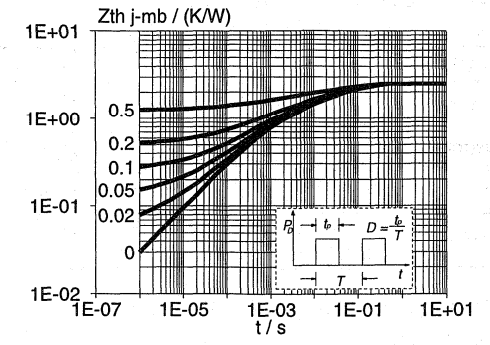


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

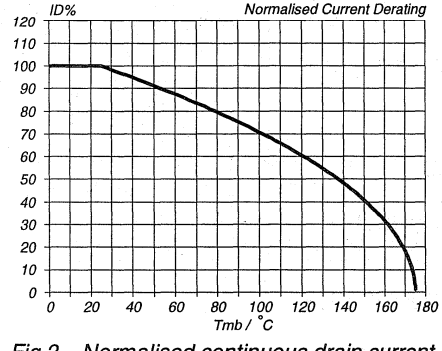


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

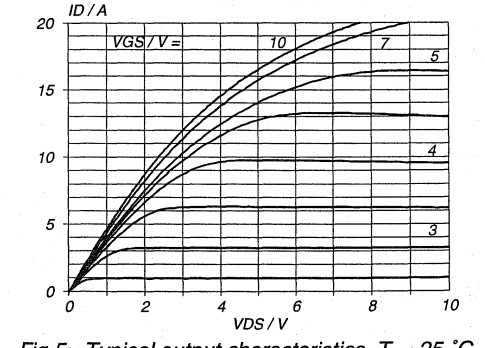


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

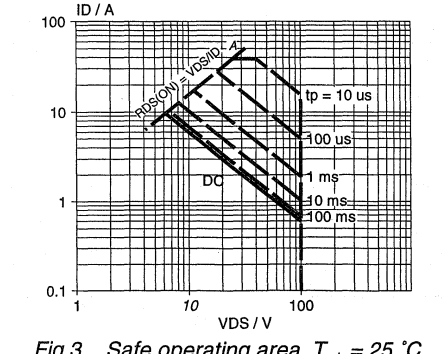


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

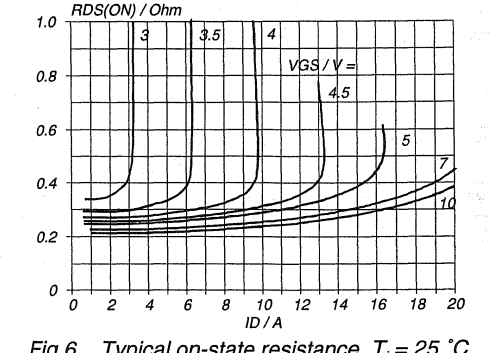


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

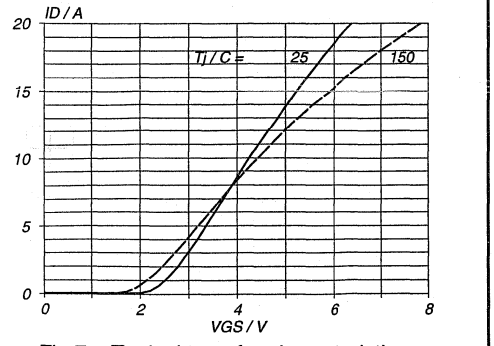


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

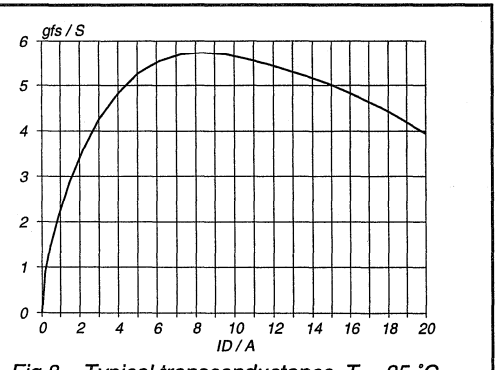


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

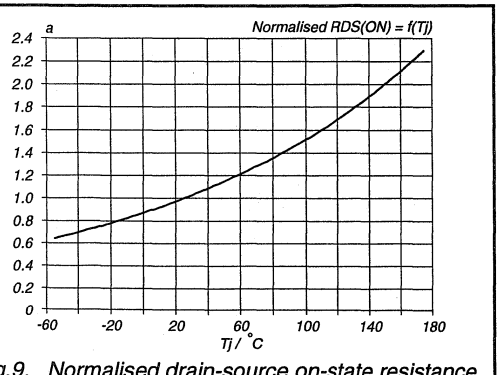


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 5.5$ A; $V_{GS} = 5$ V

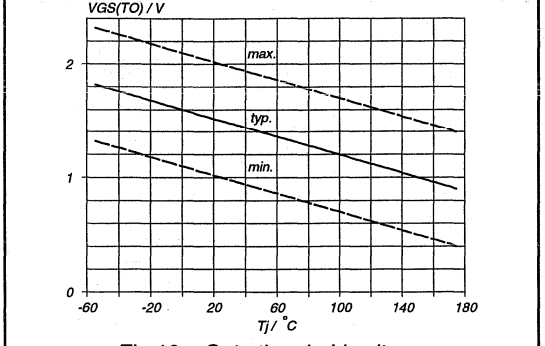


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

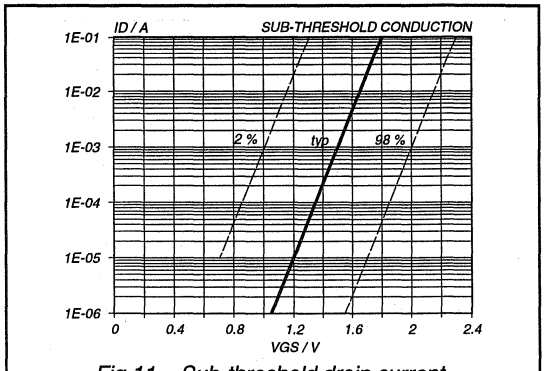


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

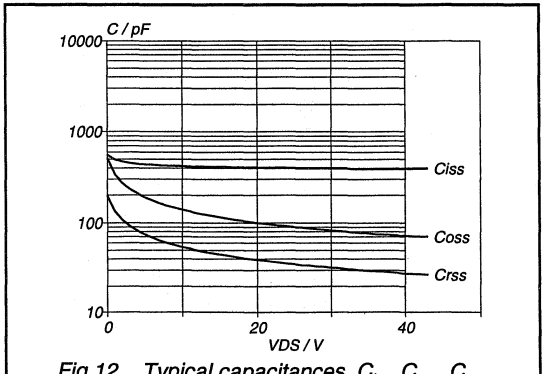


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

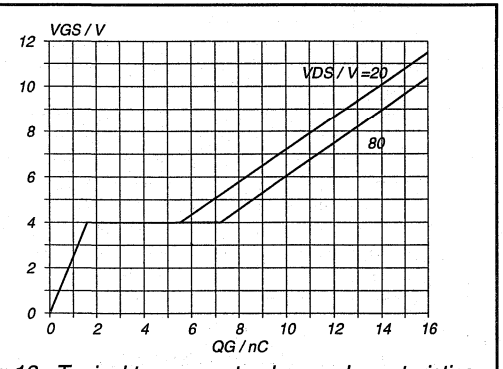


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 10$ A; parameter V_{DS}

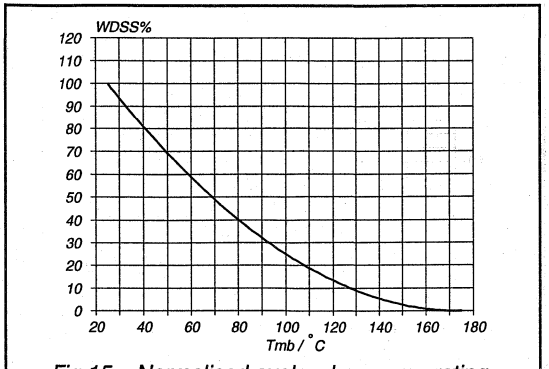


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 10$ A

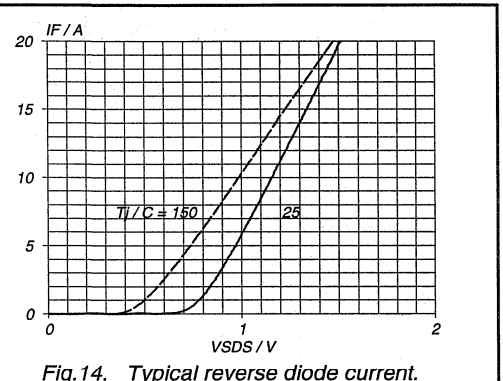


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

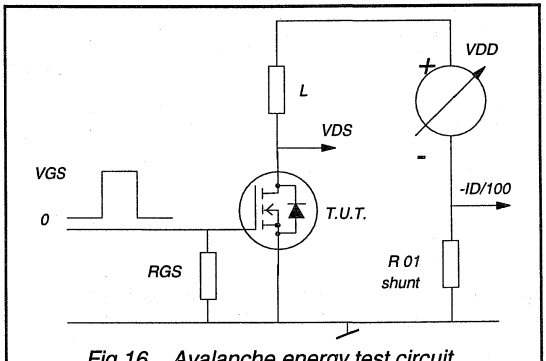


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor
Voltage clamped logic level FET

BUK563-48C

GENERAL DESCRIPTION

Protected N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive applications. It has built-in zener diodes providing active drain voltage clamping.

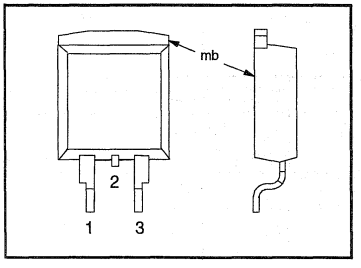
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamp voltage	40	48	58	V
I_D	Drain current (DC)			21	A
P_{tot}	Total power dissipation			75	W
T_j	Junction temperature			175	°C
W_{DSRR}	Repetitive clamped turn off energy; T_j = 150°C			50	mJ
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V			85	mΩ

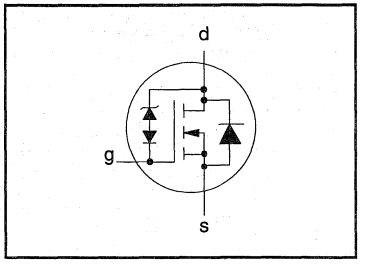
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	continuous	-	30	V
V_{DG}	Drain-gate voltage	continuous	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	21	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	15	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	84	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see fig. 18)	-	50	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DG}$	Drain-gate zener voltage	$0.2 \leq -I_G \leq 0.4$ mA; $-55°C \leq T_j \leq 150°C$	38	45	54	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	1.0	1.5	2.0	V
$V_{GS(ON)}$	Gate voltage	V_{DS} = 10 V; I_D = 10 A; $-55°C \leq T_j \leq 150°C$	2.0	3.1	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V; T_j =150 °C	-	0.01	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V; T_j =150 °C	-	0.1	10	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A	-	65	85	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain source clamp voltage (peak value)	R_G = 10 kΩ; I_D = 10 A; $-55 \leq T_j \leq 150°C$; Inductive load.	40	48	58	V
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	7	12	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	550	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	100	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 12 V; I_D = 5 A;	-	3.5	-	µs
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 kΩ;	-	22	-	µs
$t_{d\,off}$	Turn-off delay time		-	16	-	µs
t_f	Turn-off fall time		-	18	-	µs
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	21	A
I_{DRM}	Pulsed reverse drain current	-	-	-	84	A
V_{SD}	Diode forward voltage	I_F = 21 A ; V_{GS} = 0 V	-	1.3	1.7	V

CLAMPED ENERGY LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSRS}	Non-repetitive drain-source clamped inductive turn off energy	T_j = 25˚C prior to clamping; I_D = 10 A; $V_{DD} \leq$ 16 V; V_{GS} = 5 V; R_G = 10 kΩ; inductive load	-	200	mJ
W_{DSRR}	Drain-source repetitive clamped inductive turn off energy	T_j = 150˚C prior to clamping; I_D = 10 A; $V_{DD} \leq$ 16 V; V_{GS} = 5 V; R_G = 10 kΩ; inductive load	-	50	mJ

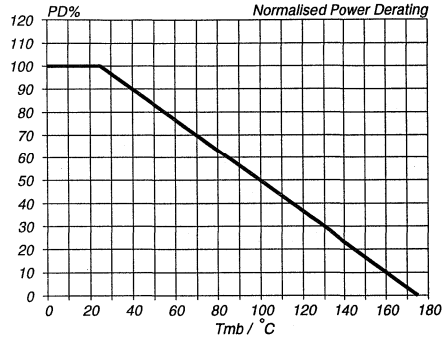


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

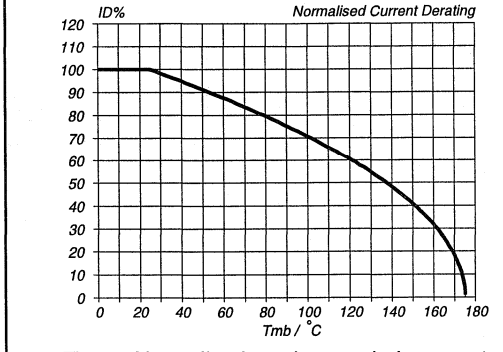


Fig.3. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

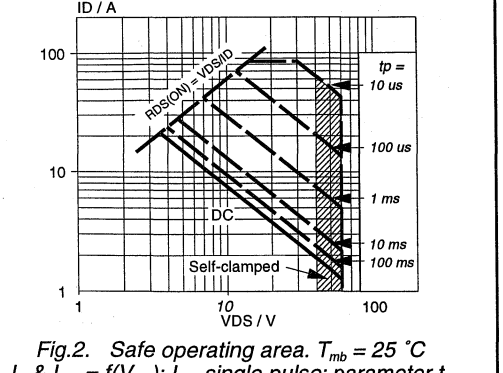


Fig.2. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

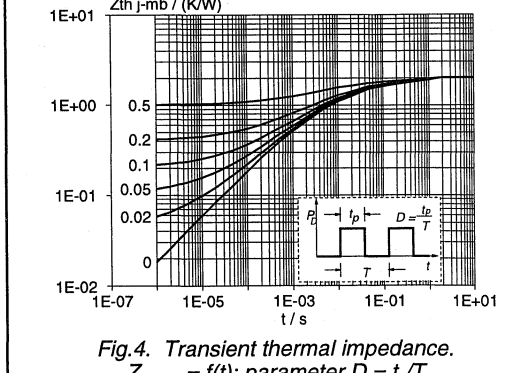


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

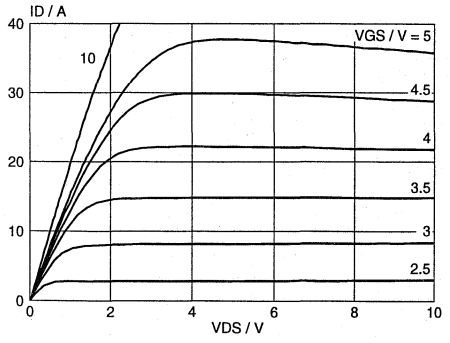


Fig.5. Typical output characteristics, $T_j = 25$ °C. $I_D = f(V_{DS})$; parameter V_{GS}

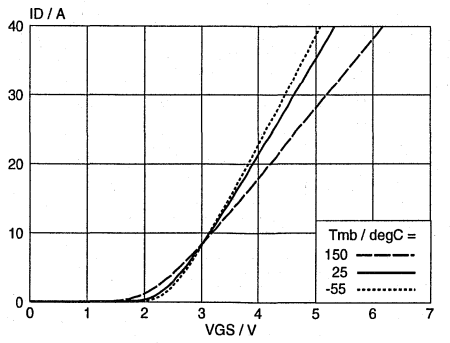


Fig.8. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V.

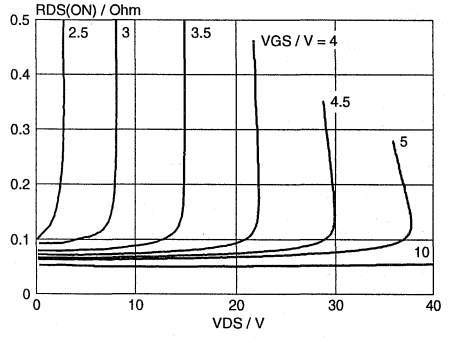


Fig.6. Typical on-state resistance, $T_j = 25$ °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

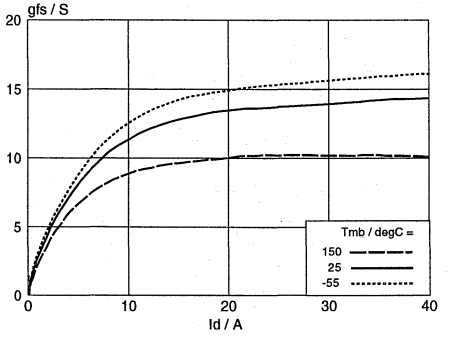


Fig.9. Typical transconductance. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

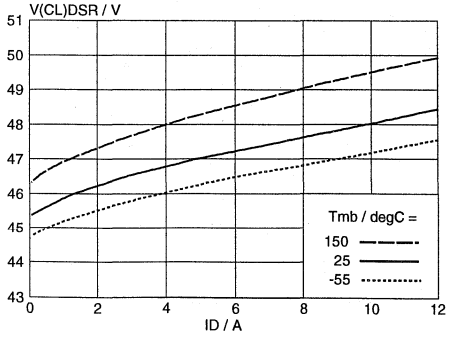


Fig.7. Typical clamping voltage $V_{(CL)DSR} = f(I_D)$; conditions: $R_G = 10$ kΩ

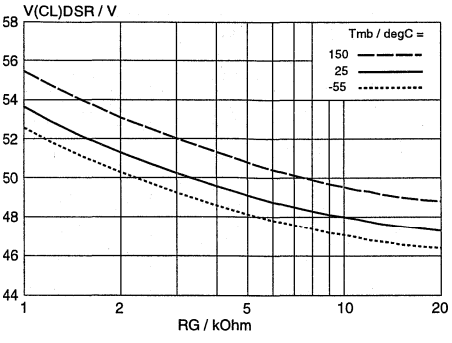


Fig.10. Typical clamping voltgage $V_{(CL)DSR} = f(R_G)$; conditions: $I_D = 10$ A.

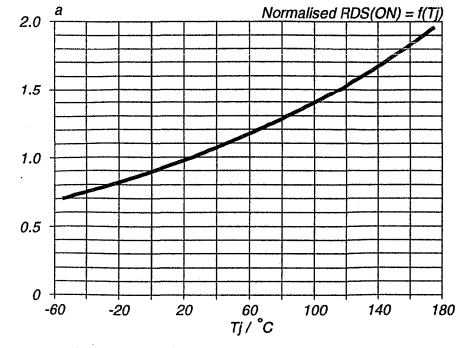


Fig.11. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 10 A; V_{GS} = 5 V

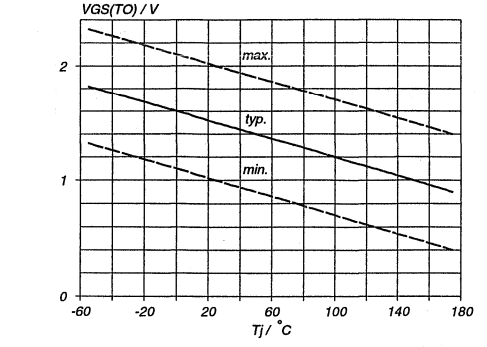


Fig.14. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

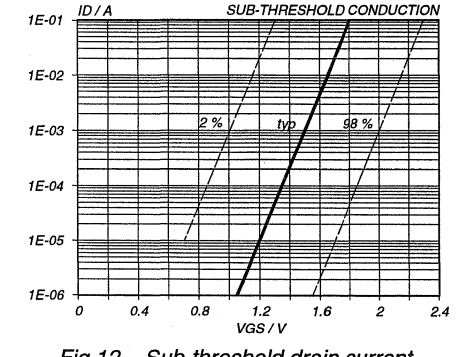


Fig.12. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

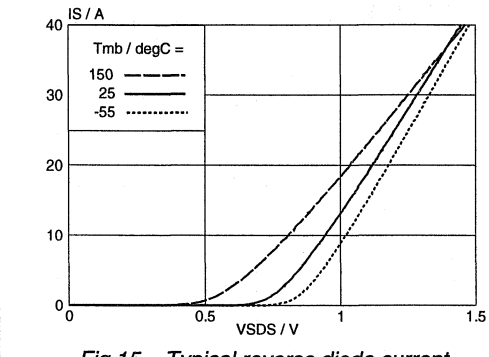


Fig.15. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

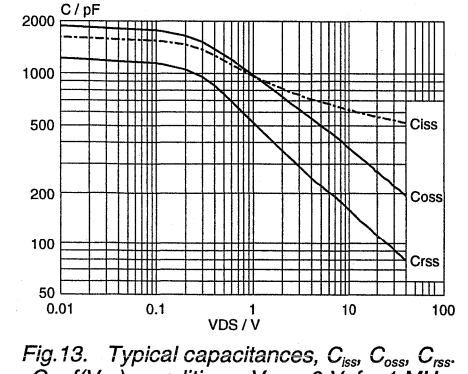


Fig.13. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

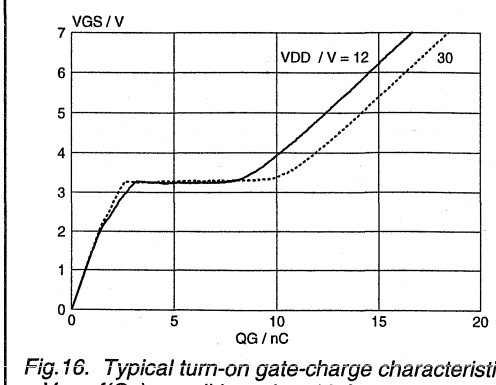


Fig.16. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 10 A; parameter V_{DS}

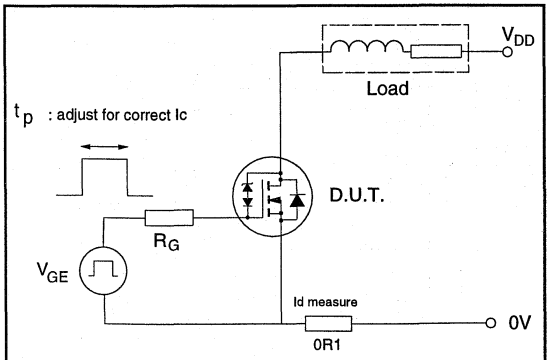


Fig.17. Inductive clamping test circuit.

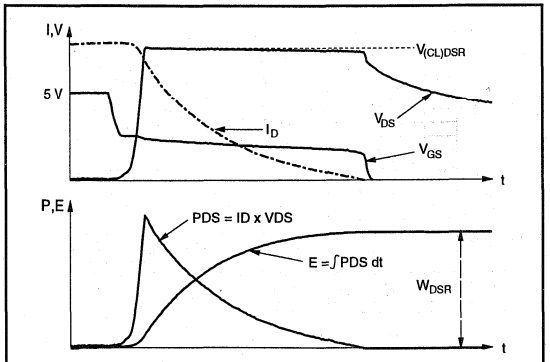


Fig.18. Typical Inductive Clamping waveforms

PowerMOS transistor Logic level FET

BUK563-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

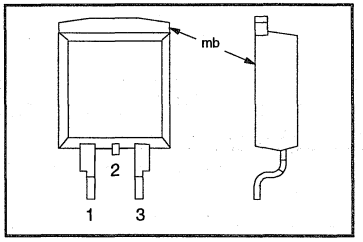
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	21	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	85	mΩ

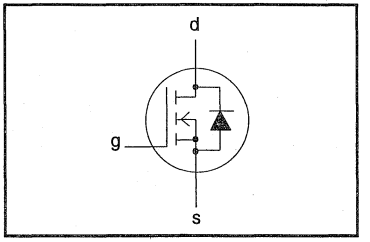
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	21	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	15	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	84	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A	-	65	85	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	7	10	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	550	825	pF
C_{oss}	Output capacitance		-	230	350	pF
C_{rss}	Feedback capacitance		-	95	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	30	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	60	120	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	110	ns
t_f	Turn-off fall time		-	65	85	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	21	A
I_{DRM}	Pulsed reverse drain current	-	-	-	84	A
V_{SD}	Diode forward voltage	I_F = 21 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 21 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	45	mJ

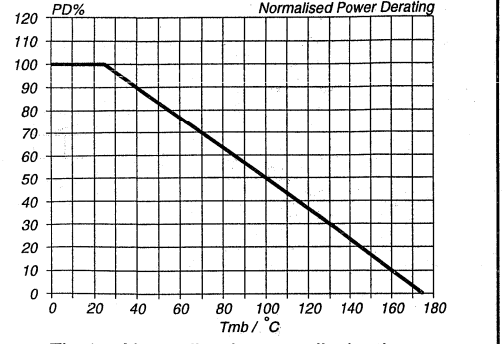


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

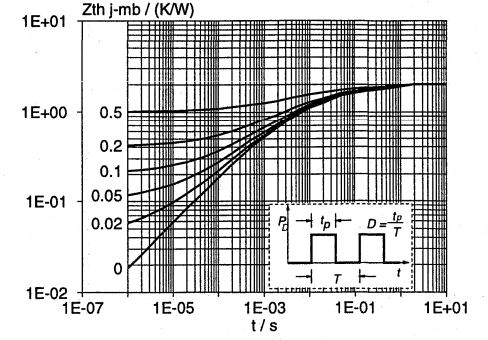


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

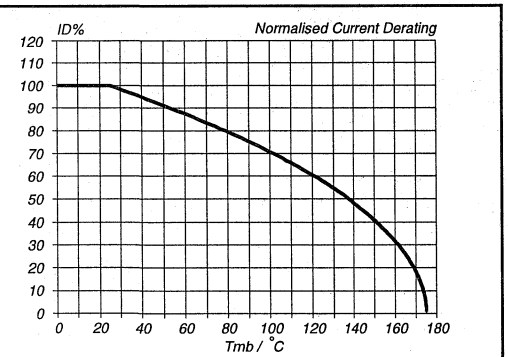


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

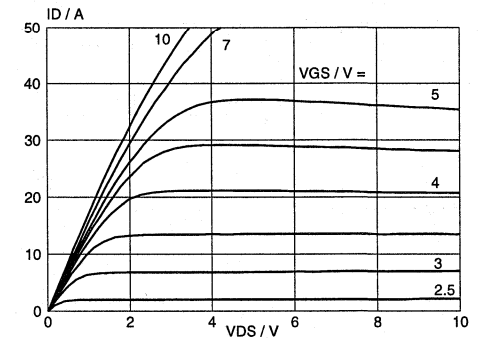


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

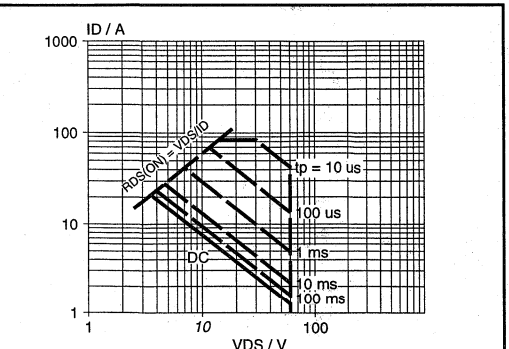


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

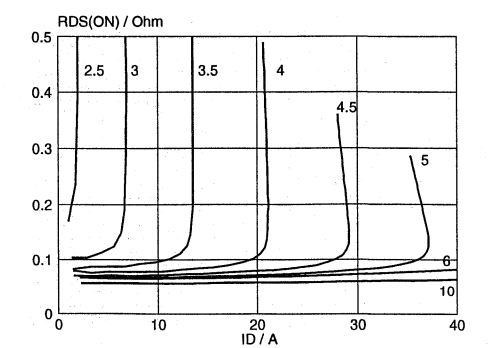


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

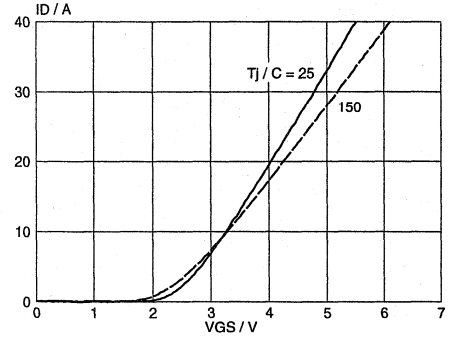


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

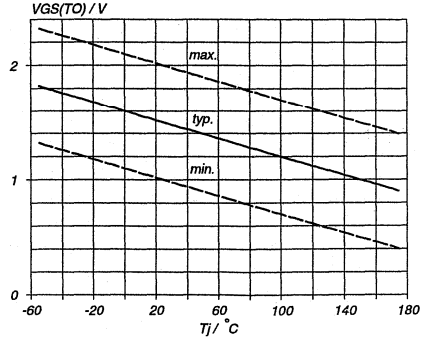


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

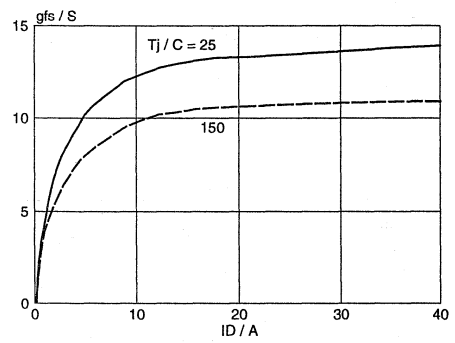


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

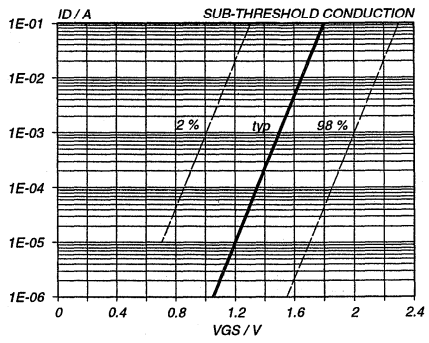


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

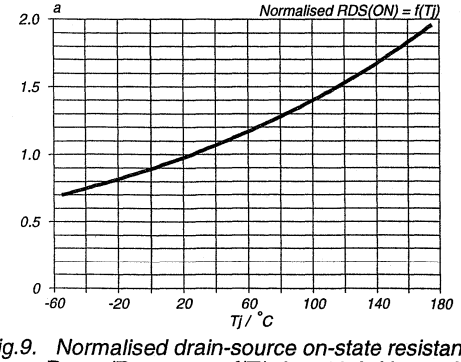


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 10$ A; $V_{GS} = 5$ V

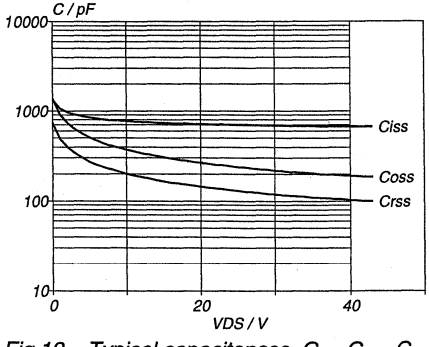


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

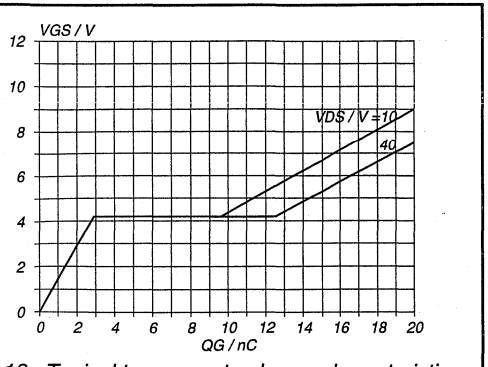


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 20$ A; parameter V_{DS}

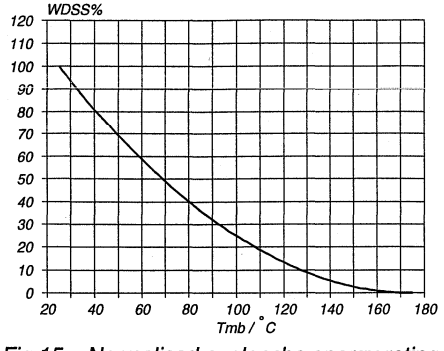


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 20$ A

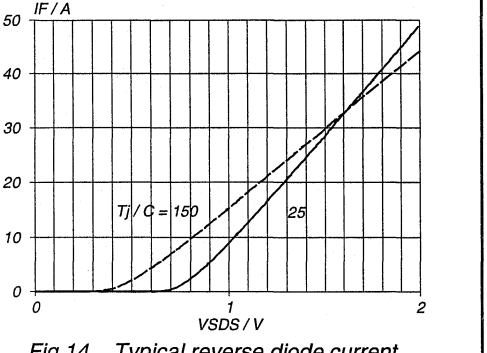


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

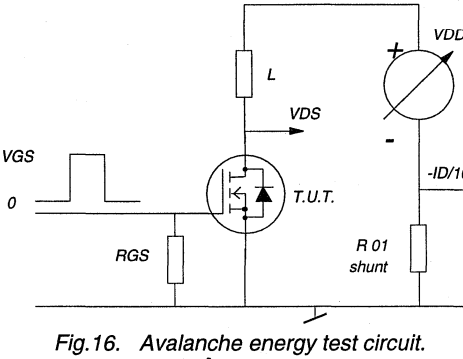


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK563-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

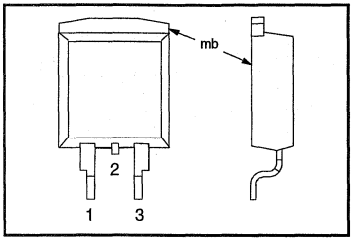
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	13	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.18	Ω

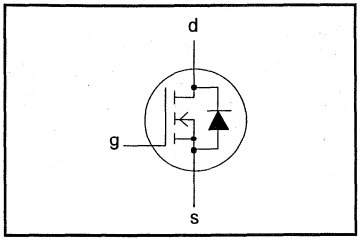
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 boards (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 6.5 A	-	0.17	0.18	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6.5 A	6.0	8.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	620	825	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	90	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	90	115	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 13 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	70	mJ

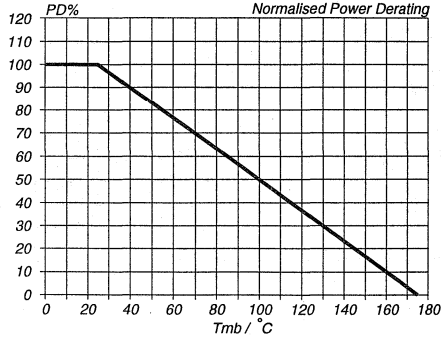


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

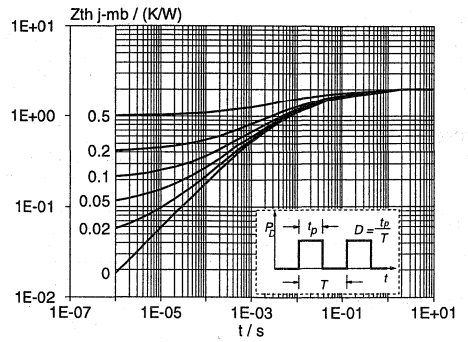


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

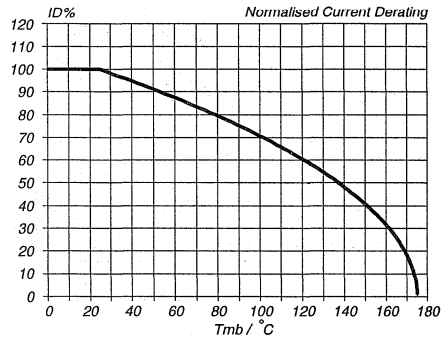


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

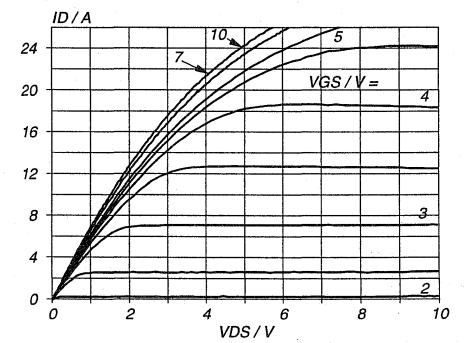


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

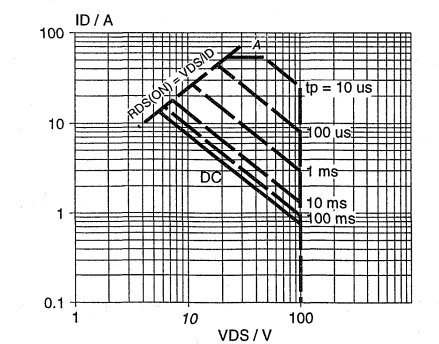


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

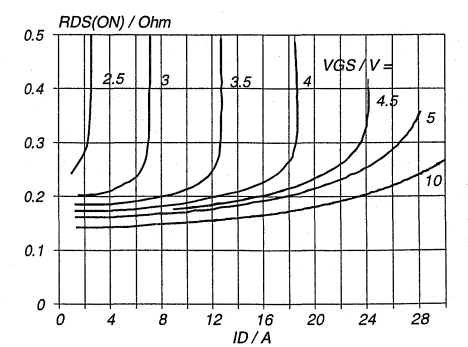


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

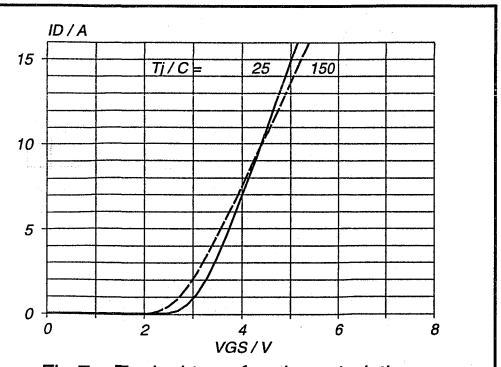


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

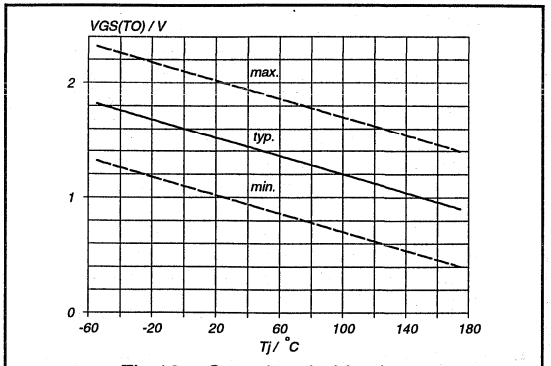


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

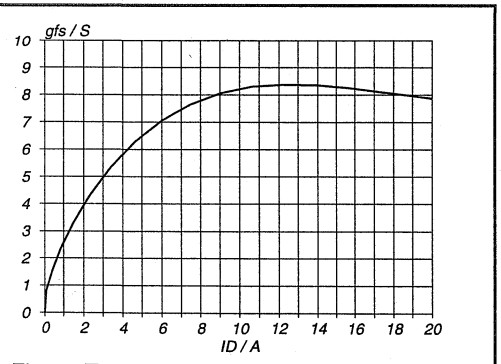


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

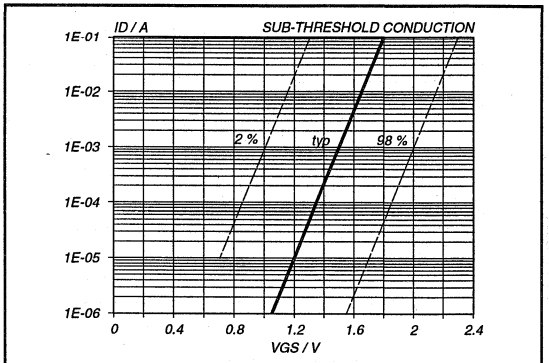


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

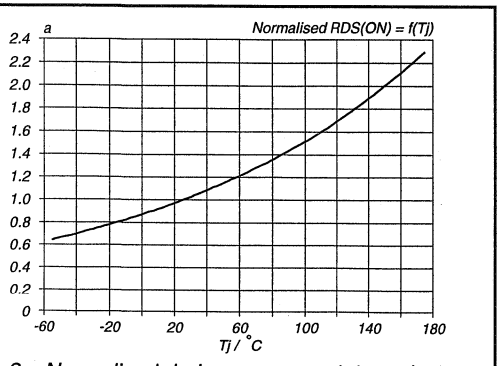


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 6.5$ A; $V_{GS} = 5$ V

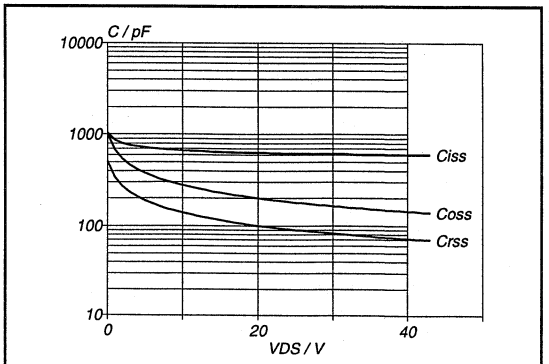


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

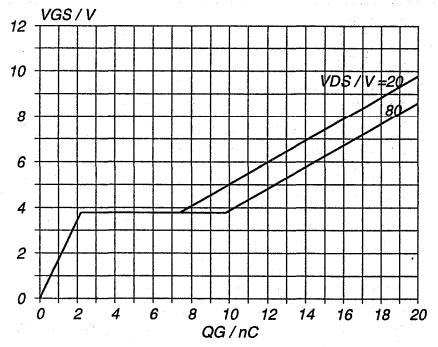


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 13$ A; parameter V_{DS}

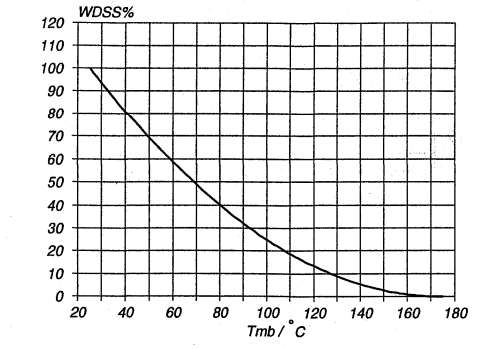


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 13$ A

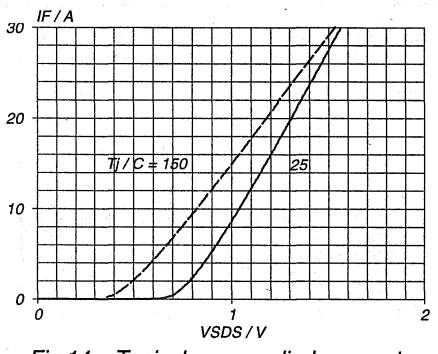


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

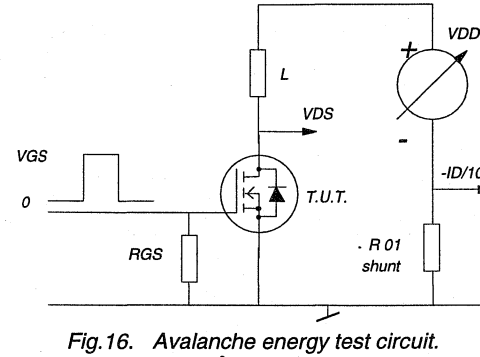


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK564-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

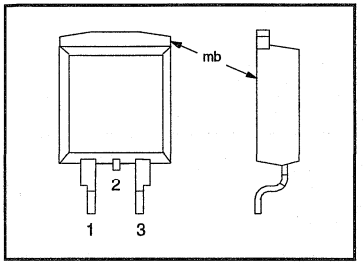
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	39	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	42	mΩ

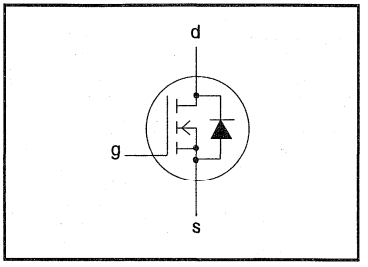
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	39	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	156	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	35	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	10	18	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	1750	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	110	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	150	220	ns
t_f	Turn-off fall time		-	100	145	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	39	A
I_{DRM}	Pulsed reverse drain current	-	-	-	156	A
V_{SD}	Diode forward voltage	I_F = 39 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 39 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 39 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

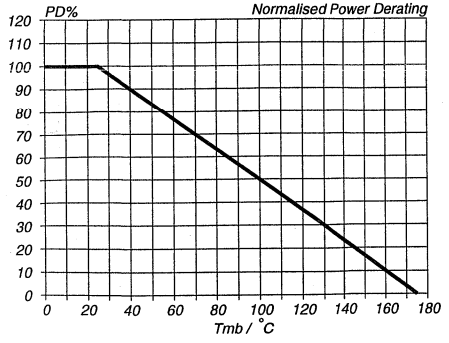


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

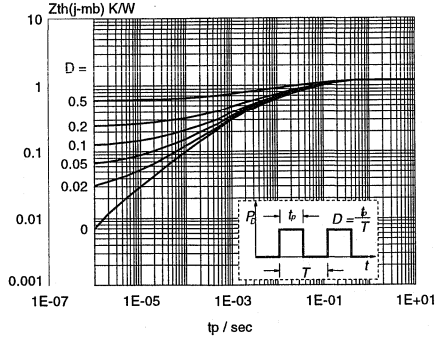


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

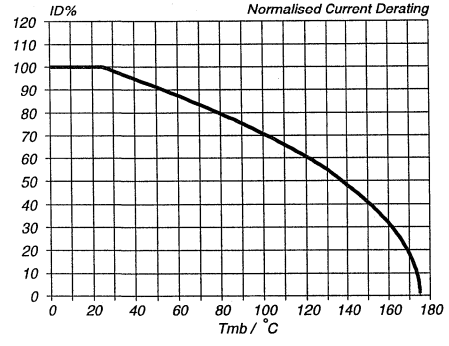


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

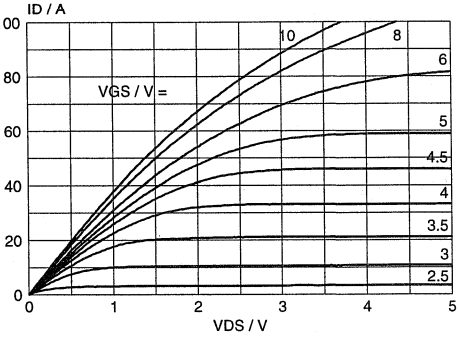


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

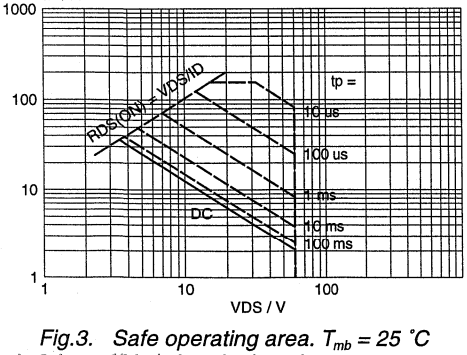


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

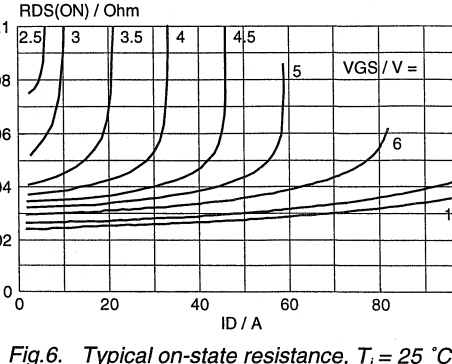


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

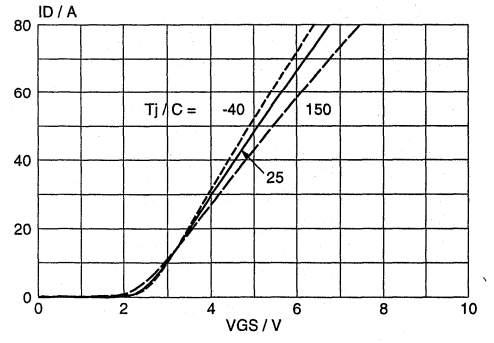


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

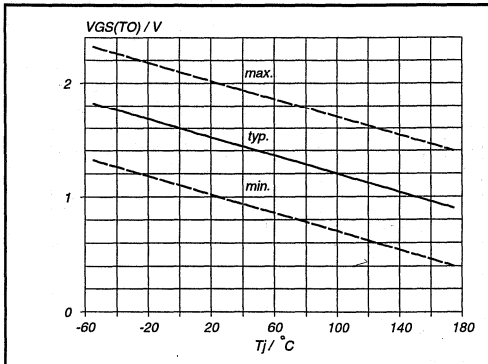


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

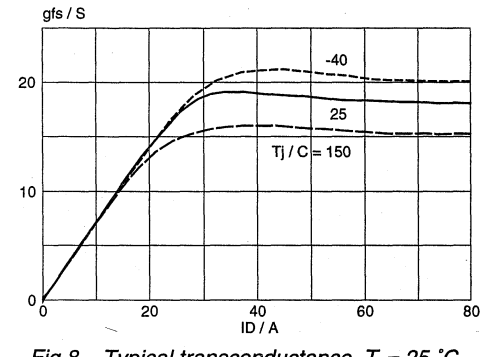


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

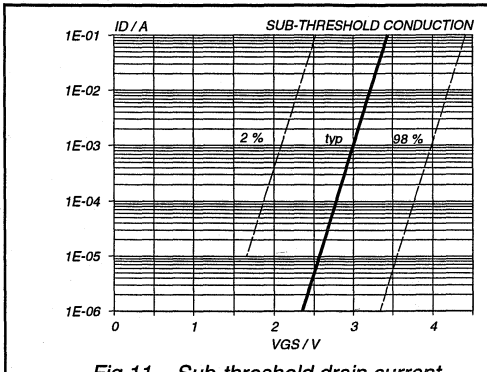


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

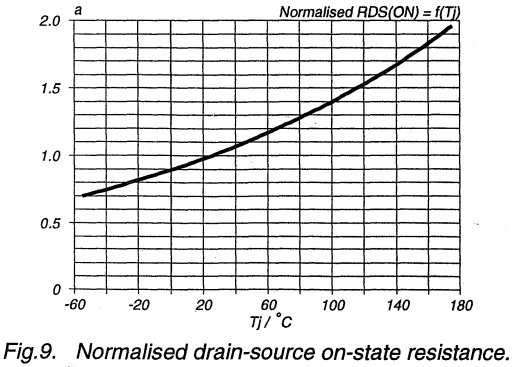


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 20$ A; $V_{GS} = 5$ V

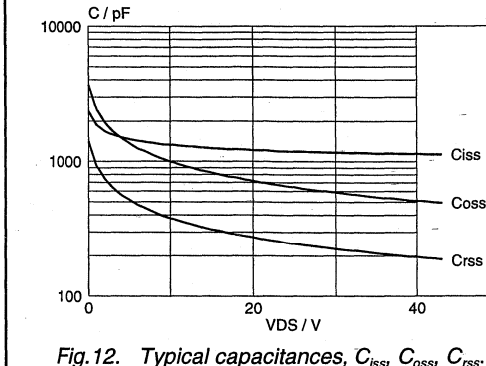


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

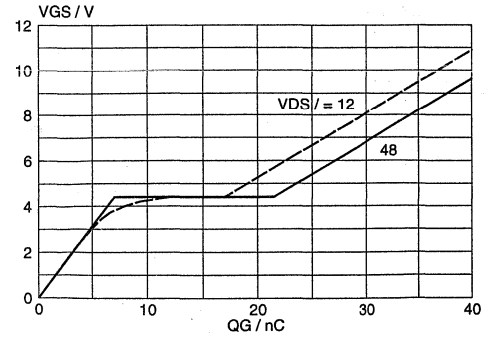


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 39$ A; parameter V_{DS}

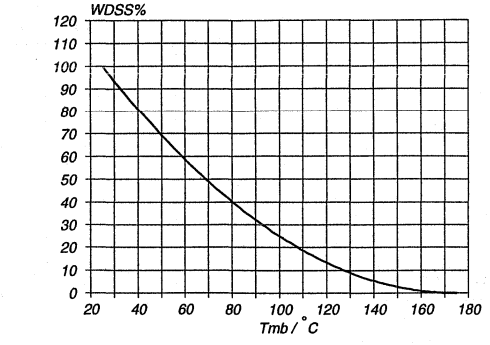


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 39$ A

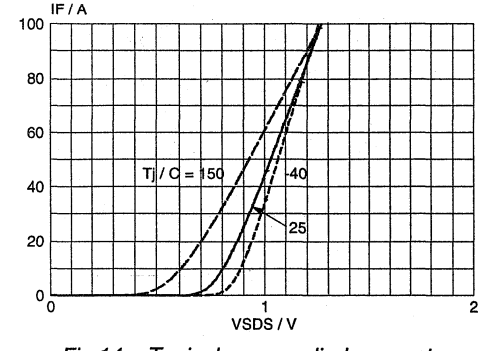


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

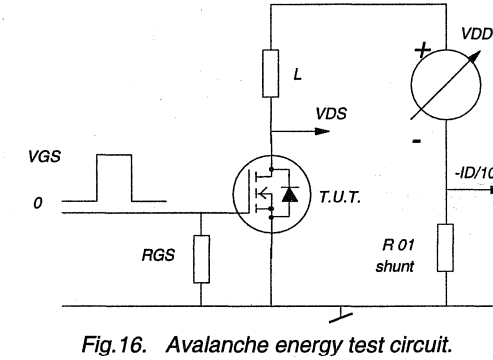


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK564-200A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

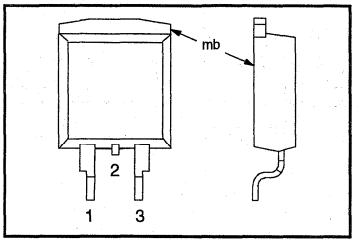
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.4	Ω

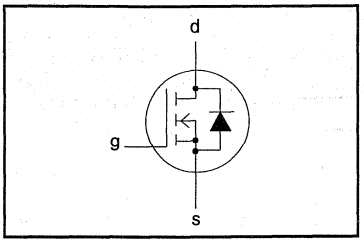
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 3.5 A	-	0.35	0.4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	6.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	800	1000	pF
C_{oss}	Output capacitance		-	120	160	pF
C_{rss}	Feedback capacitance		-	65	90	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	16	30	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	75	110	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	120	180	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	50	mJ

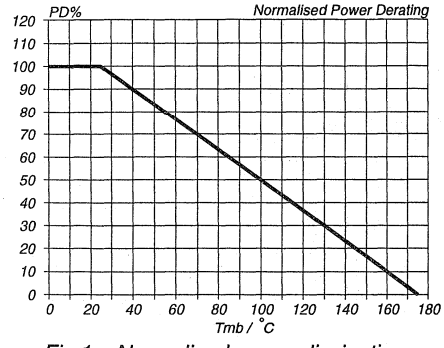


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

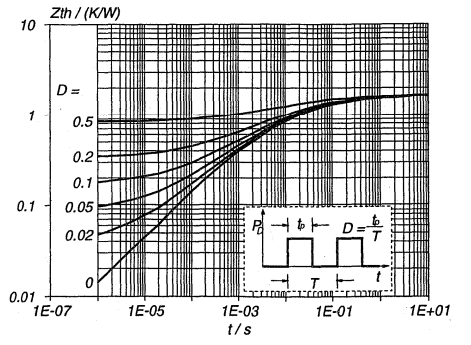


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

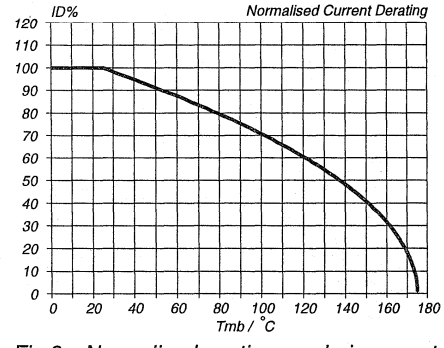


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

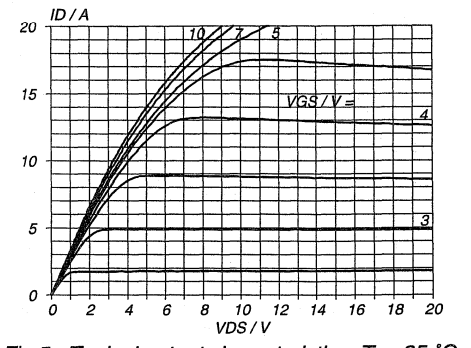


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

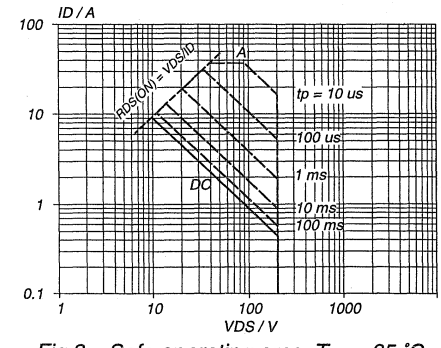


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

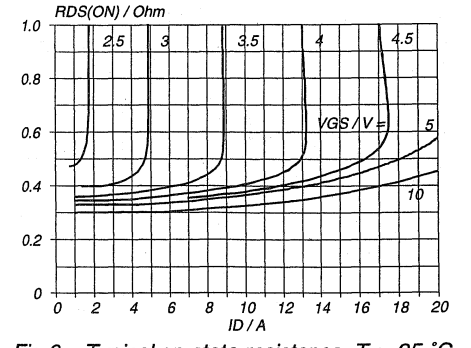


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

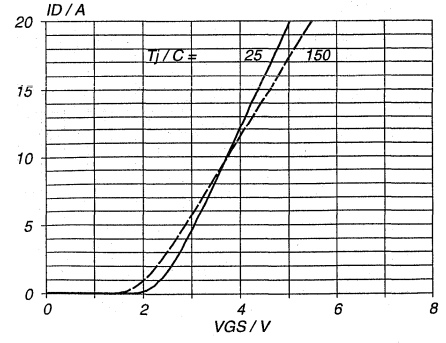


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

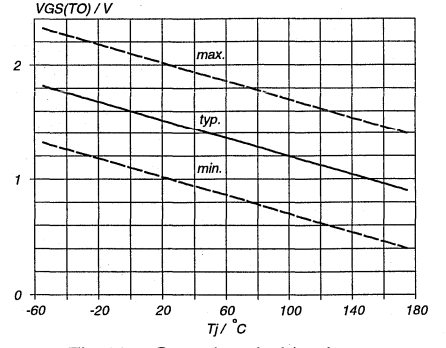


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

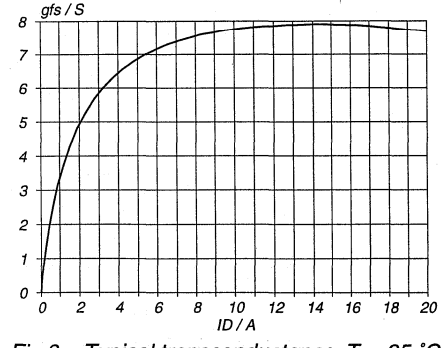


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

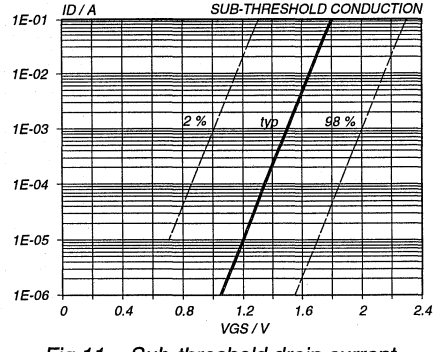


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

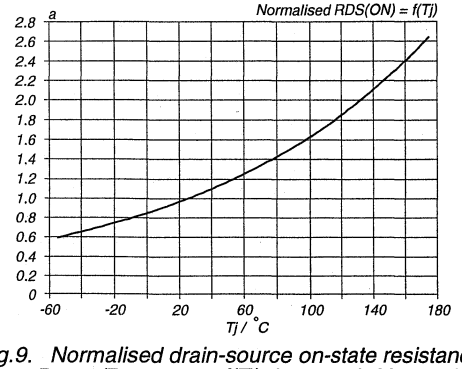


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 5 V

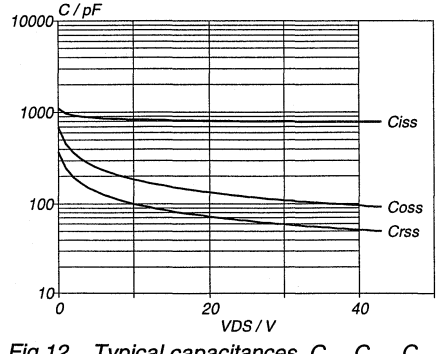


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

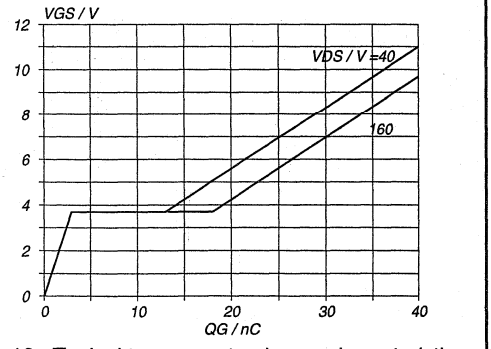


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 9.2$ A; parameter V_{DS}

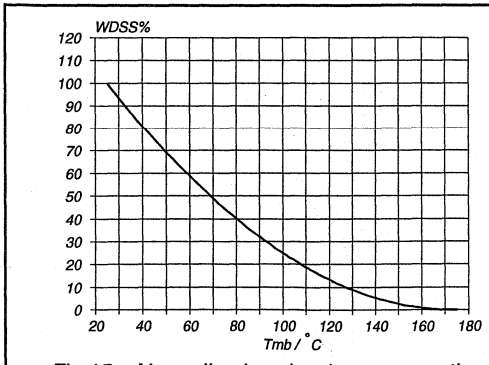


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

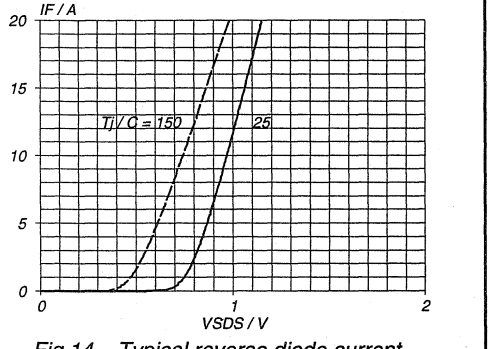


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

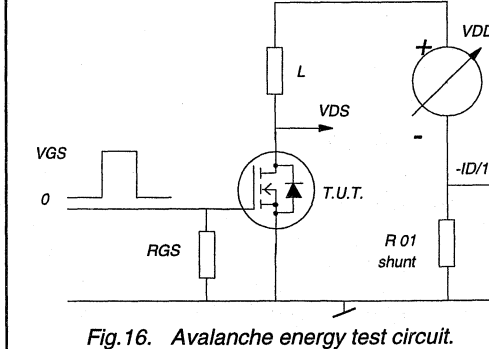


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK565-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

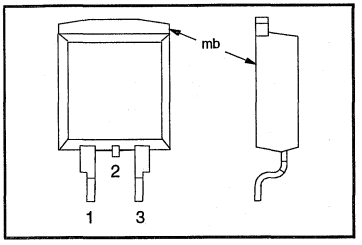
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	39	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.042	Ω

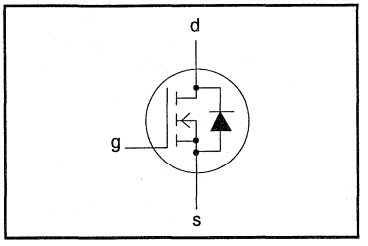
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	39	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	28	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	156	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	0.035	0.042	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	11	20	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	220	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	120	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	160	220	ns
t_f	Turn-off fall time		-	110	145	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	39	A
I_{DRM}	Pulsed reverse drain current	-	-	-	156	A
V_{SD}	Diode forward voltage	I_F = 39 A ; V_{GS} = 0 V	-	1.4	2.0	V
t_{rr}	Reverse recovery time	I_F = 39 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 39 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

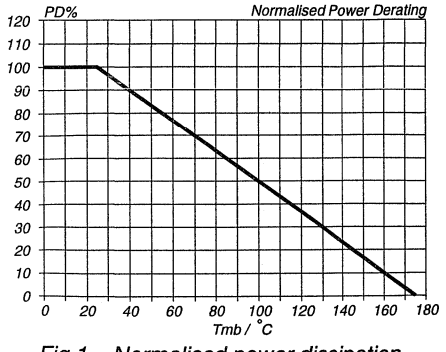


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

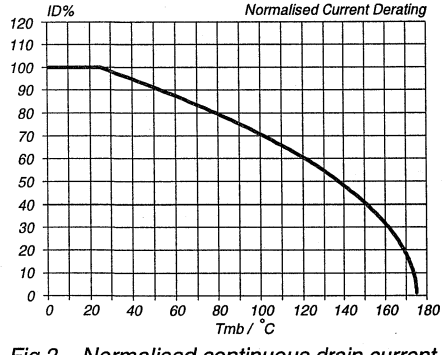


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

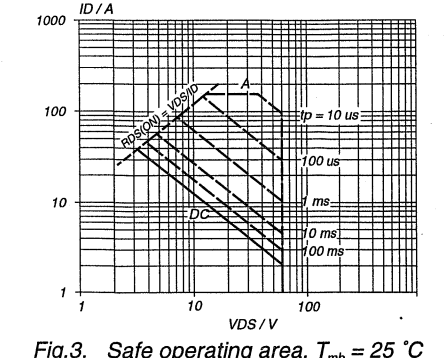


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

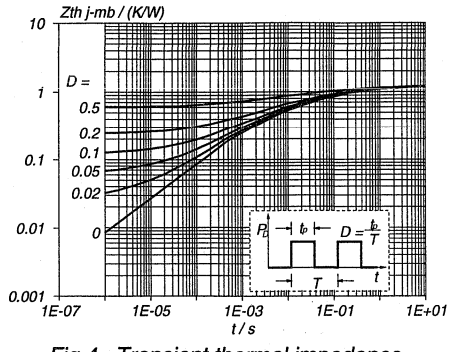


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

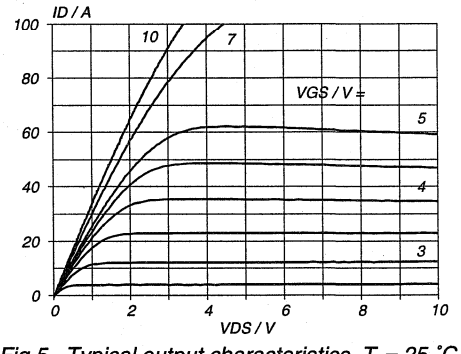


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

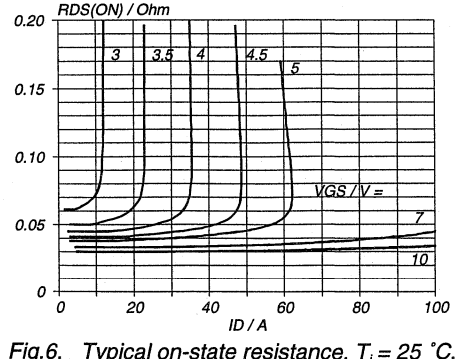


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

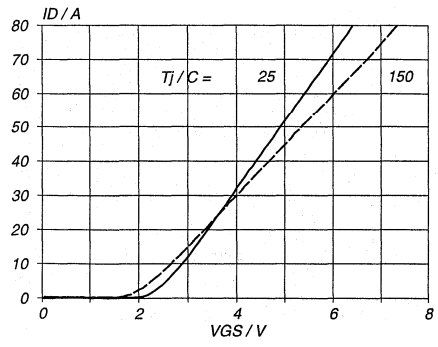


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

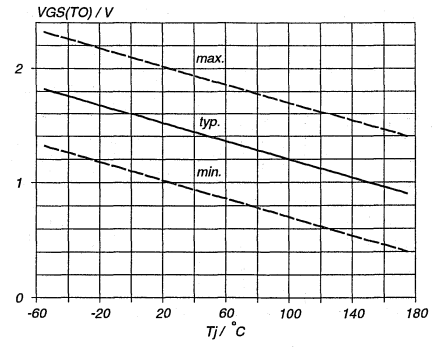


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

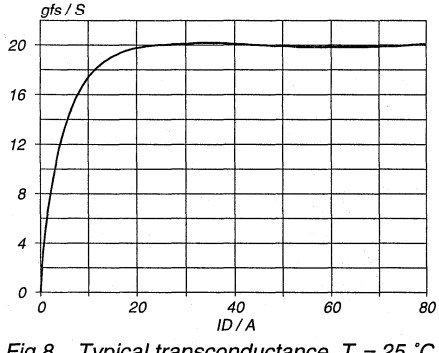


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

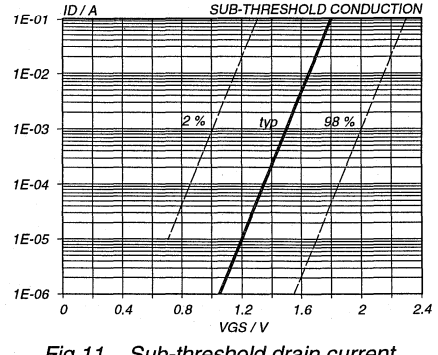


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

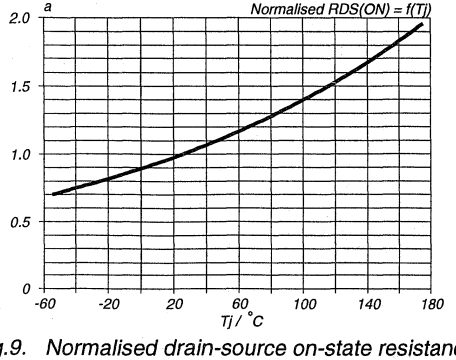


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

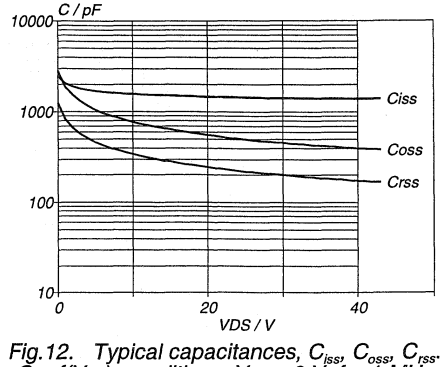


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

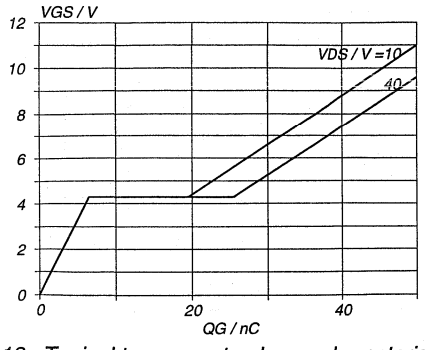


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 39$ A; parameter V_{DS}

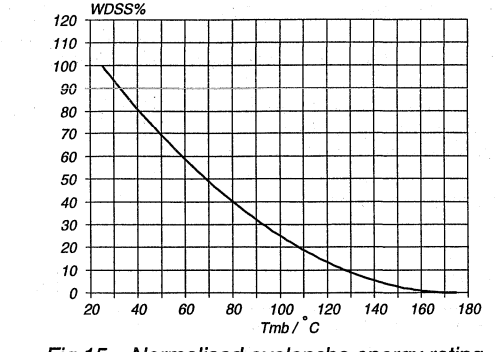


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 39$ A

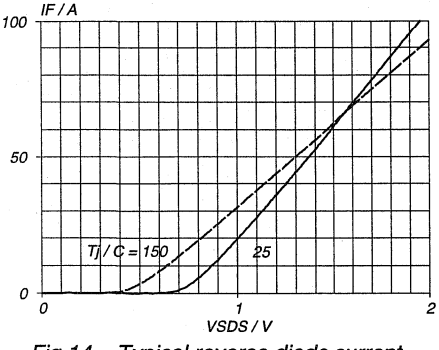


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

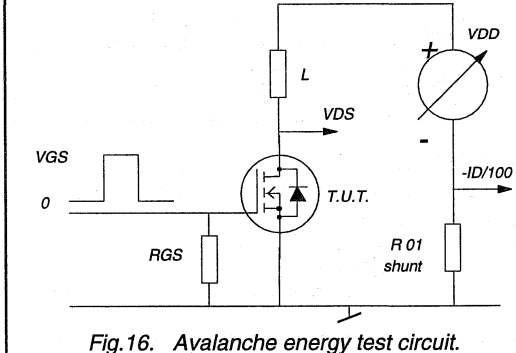


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK565-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

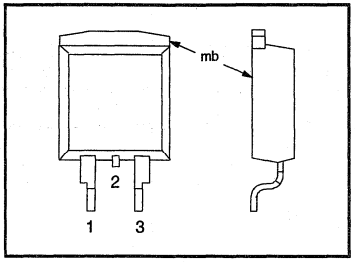
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	41	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	38	mΩ

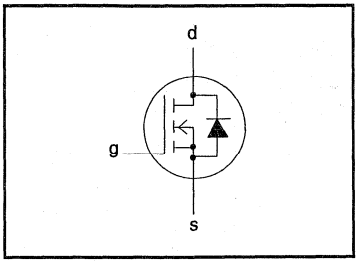
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18)	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	25	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	11	20	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1200	1750	pF
C_{oss}	Output capacitance		-	470	600	pF
C_{rss}	Feedback capacitance		-	180	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	120	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	160	220	ns
t_f	Turn-off fall time		-	110	145	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

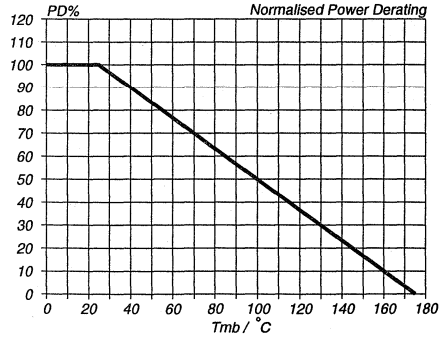


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

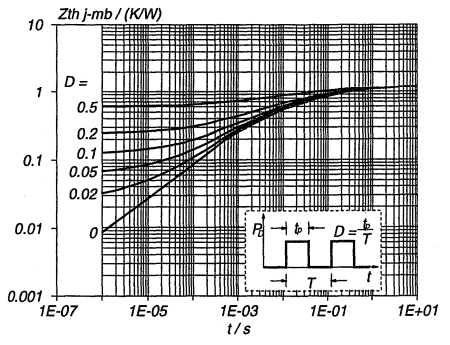


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

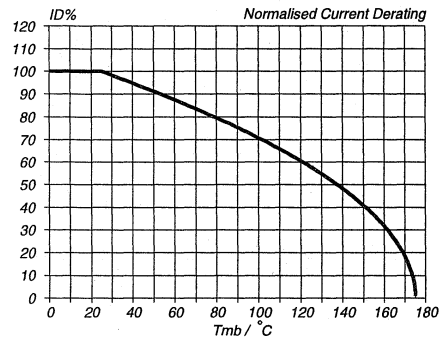


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

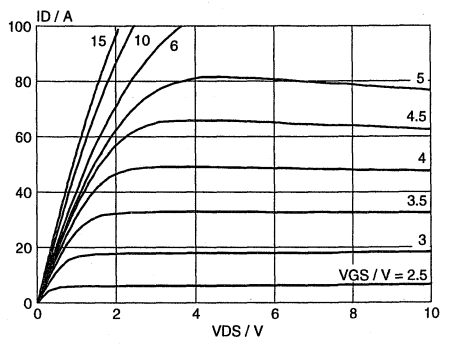


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

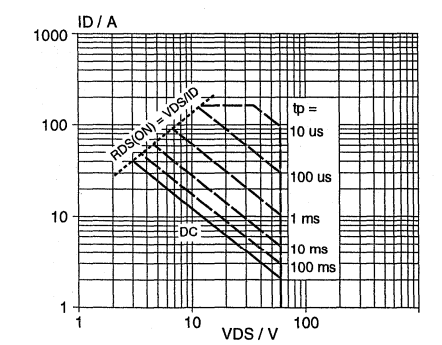


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

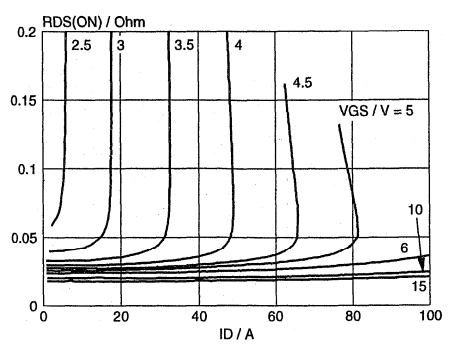


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

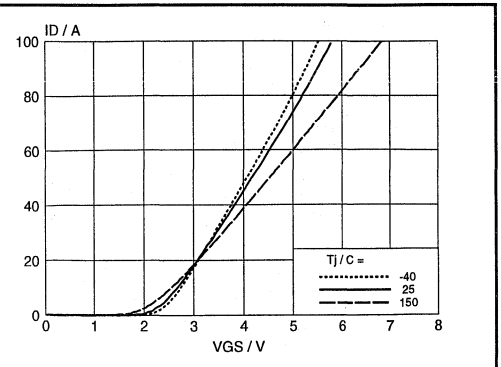


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

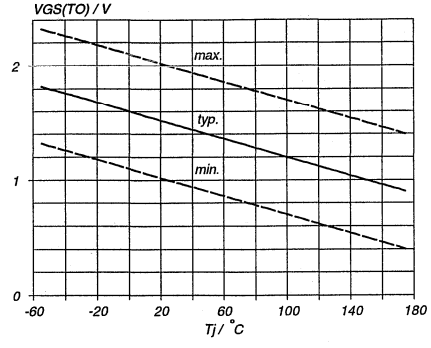


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

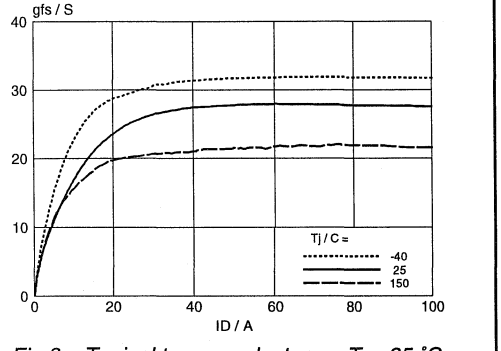


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V

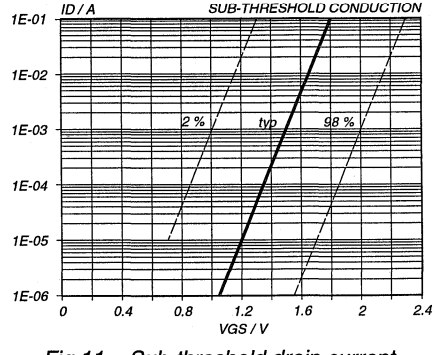


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

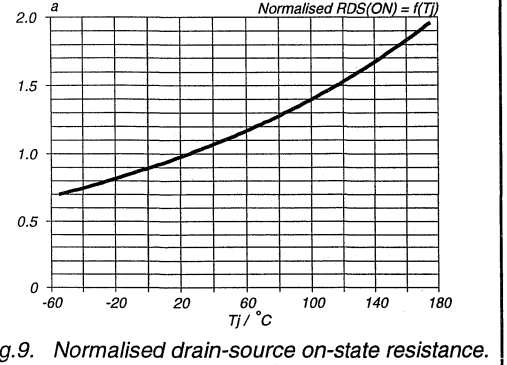


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 5 V

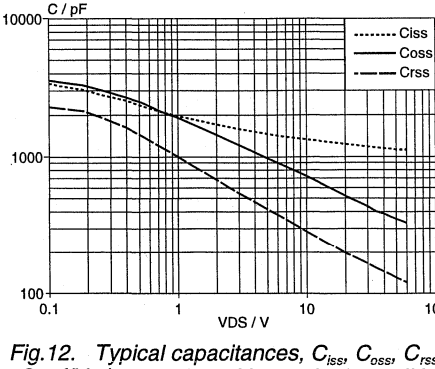


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

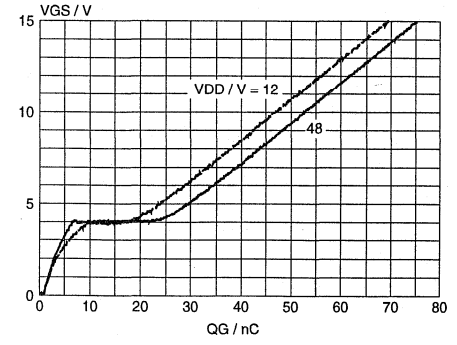


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

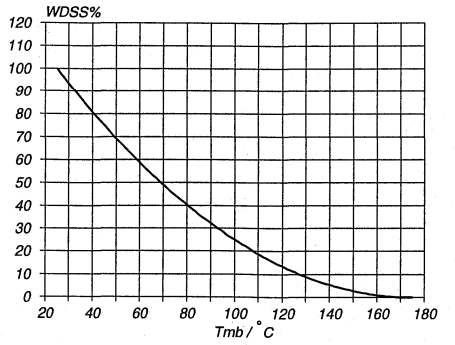


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

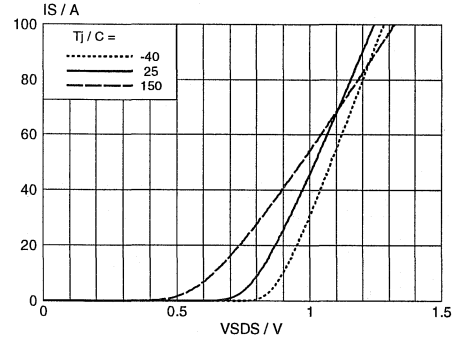


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

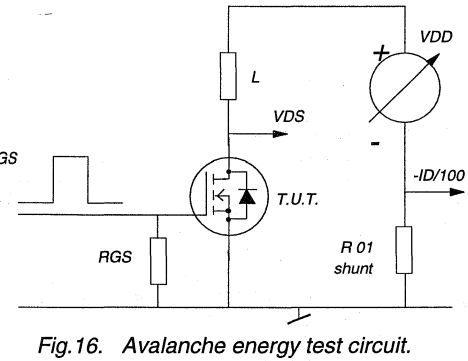


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK565-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

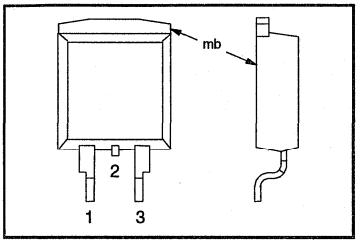
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	25	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5$ V	0.085	Ω

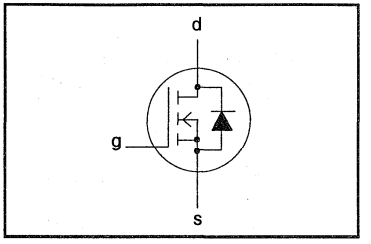
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	25	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	100	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 13 A	-	0.075	0.085	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	10	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C_{oss}	Output capacitance		-	280	350	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	65	85	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	135	180	ns
t_f	Turn-off fall time		-	80	110	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	25	A
I_{DRM}	Pulsed reverse drain current	-	-	-	100	A
V_{SD}	Diode forward voltage	I_F = 25 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 25 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; V_{DD} ≤ 50 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	140	mJ

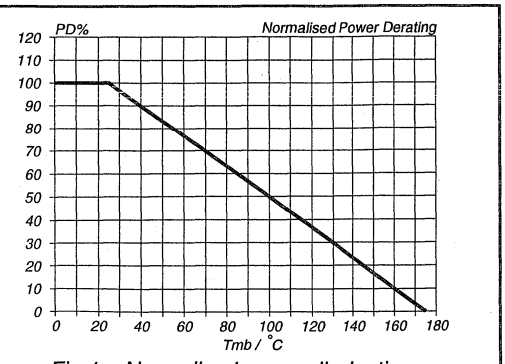


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

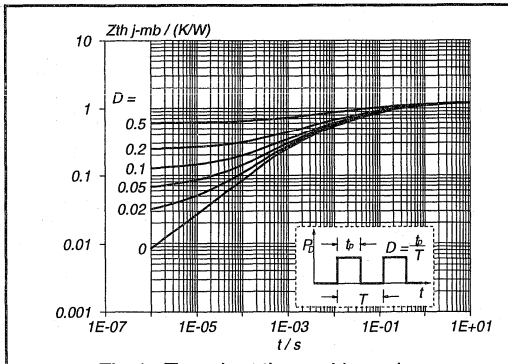


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

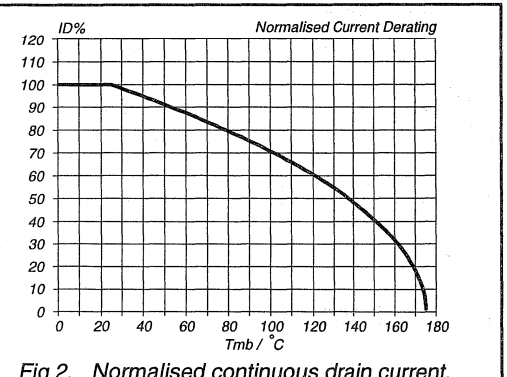


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

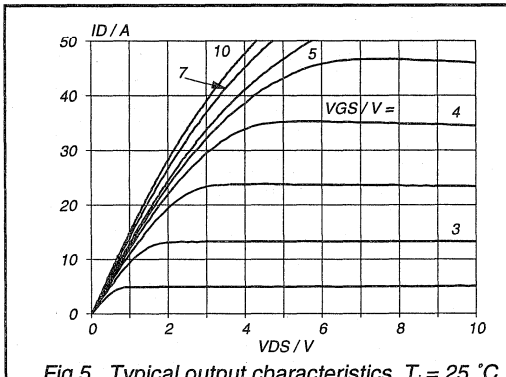


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

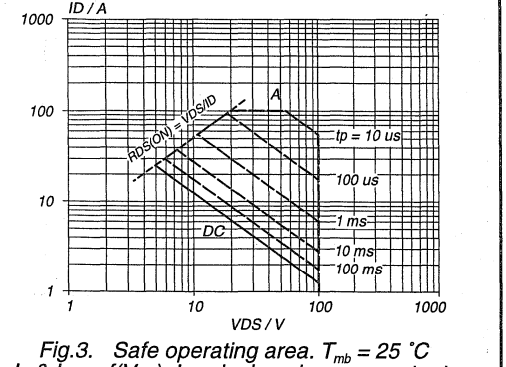


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

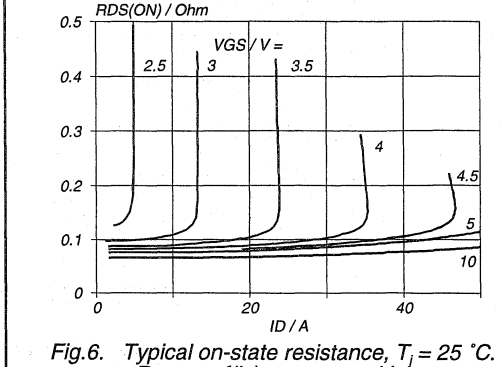


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

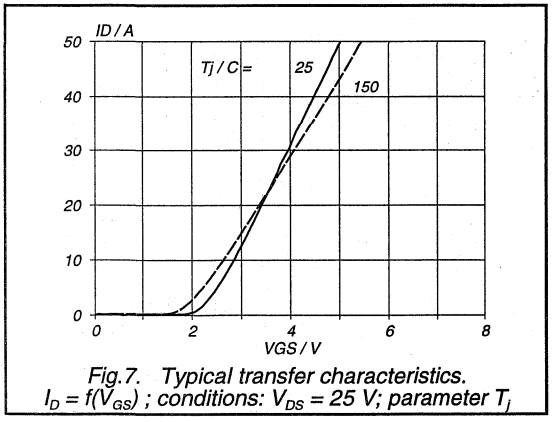


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

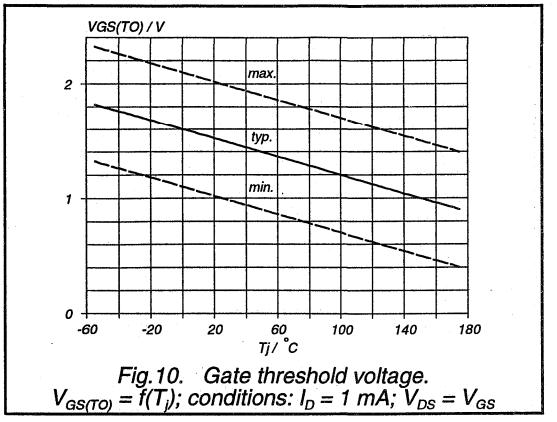


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

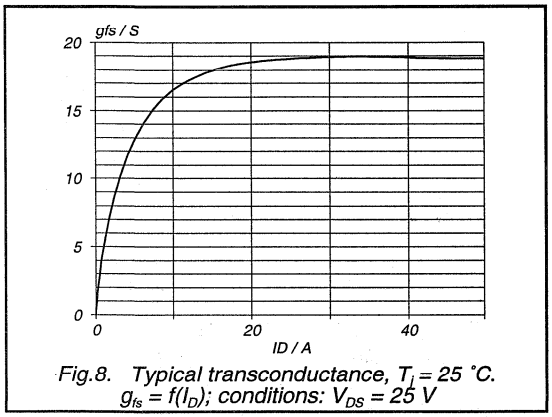


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

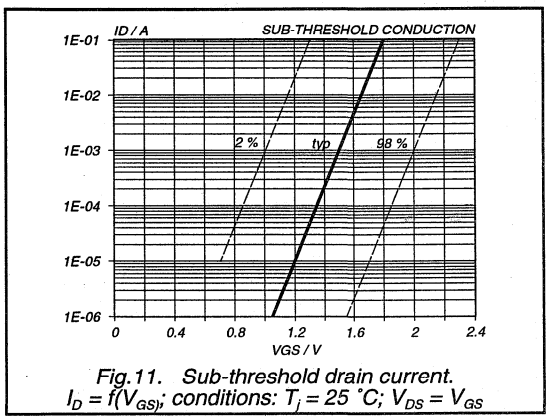


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

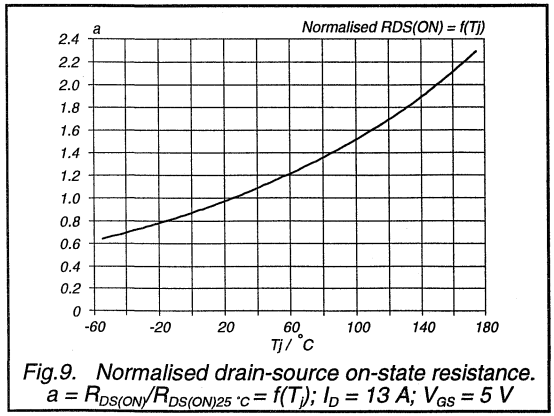


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 13$ A; $V_{GS} = 5$ V

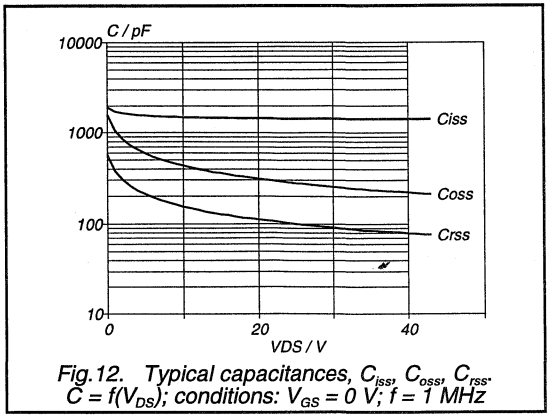


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

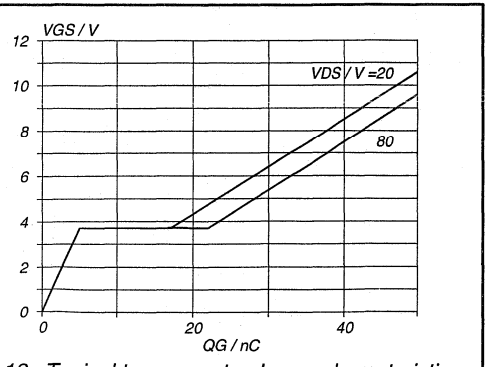


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 25$ A; parameter V_{DS}

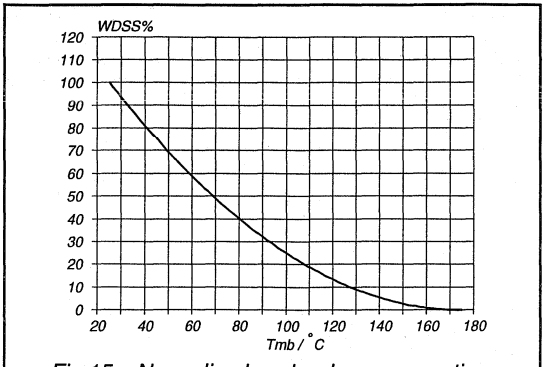


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 25$ A

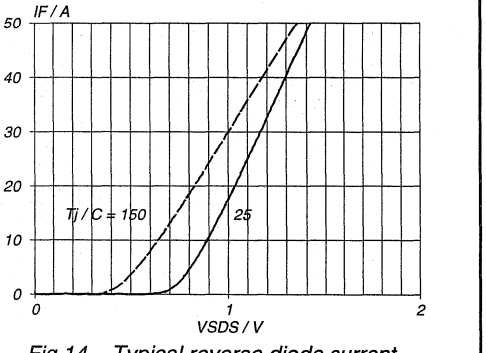


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

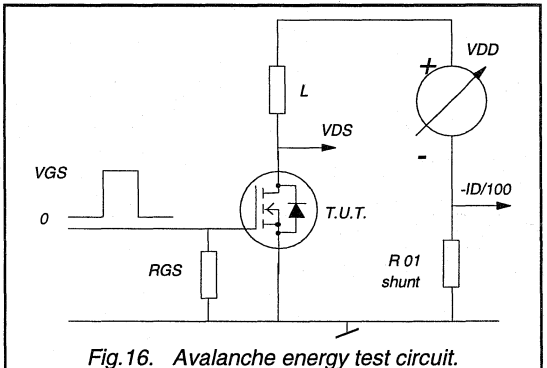


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK565-200A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

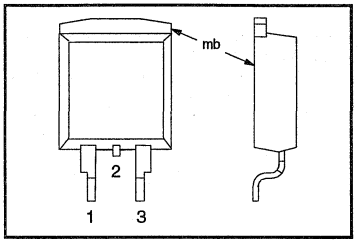
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.23	Ω

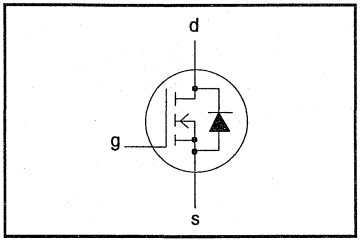
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 boards (see Fig. 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 7 A	-	0.2	0.23	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	8.0	15	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1600	2000	pF
C_{oss}	Output capacitance		-	180	250	pF
C_{rss}	Feedback capacitance		-	55	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	75	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	140	180	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.0	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	200	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 100 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	100	mJ

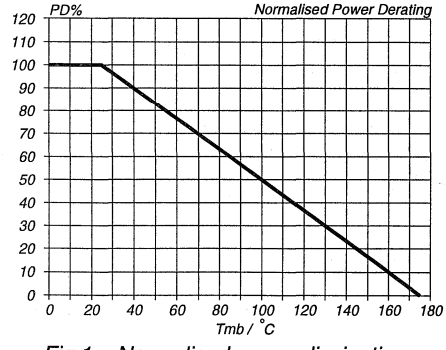


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

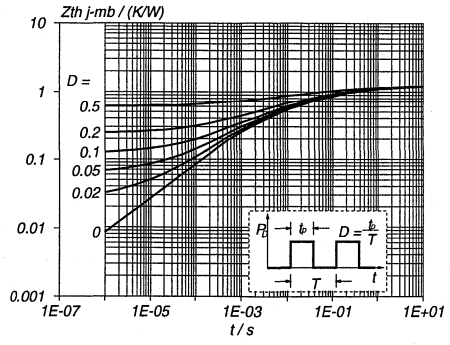


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

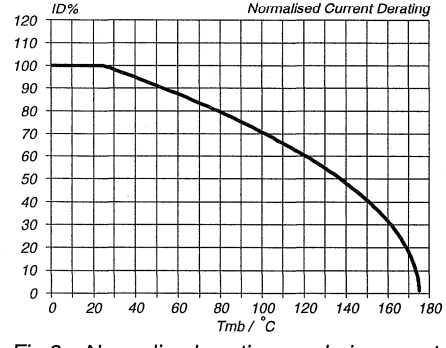


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

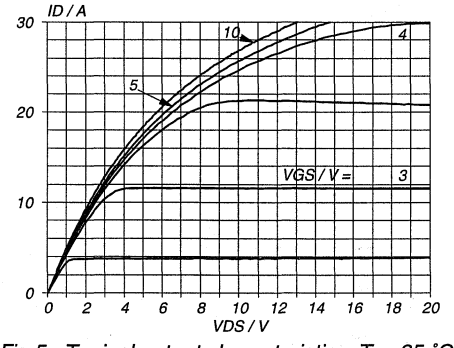


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

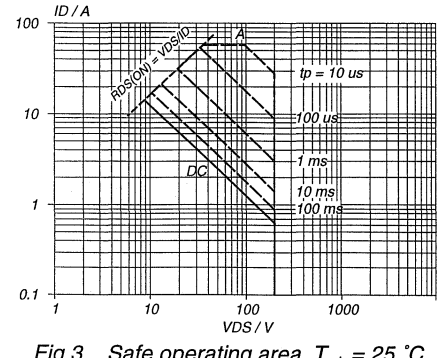


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

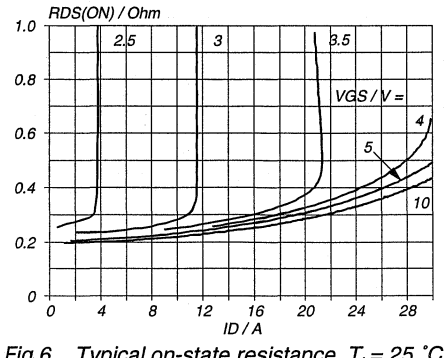


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

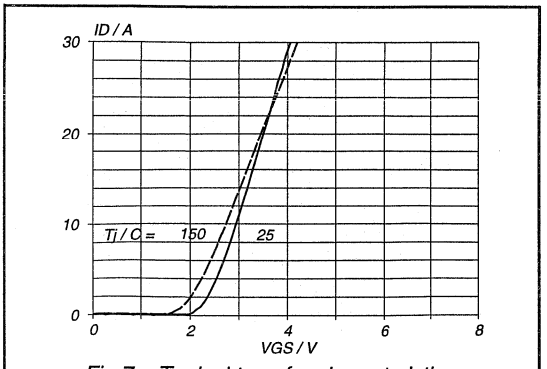


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

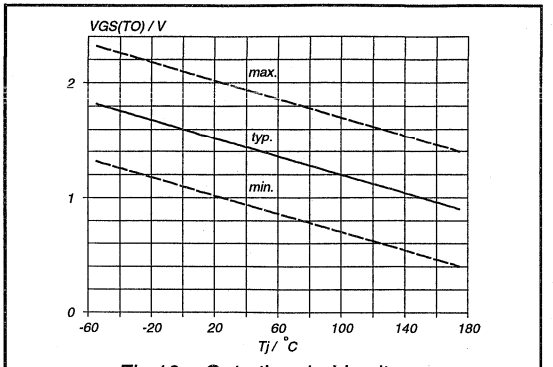


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

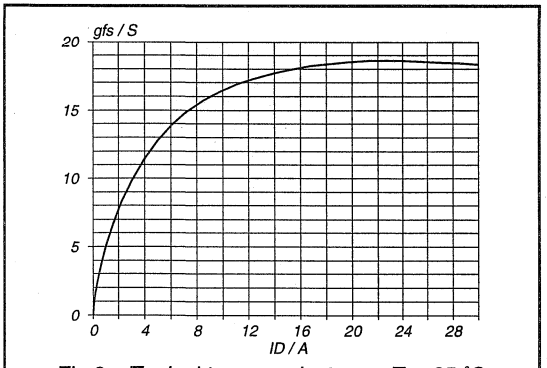


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

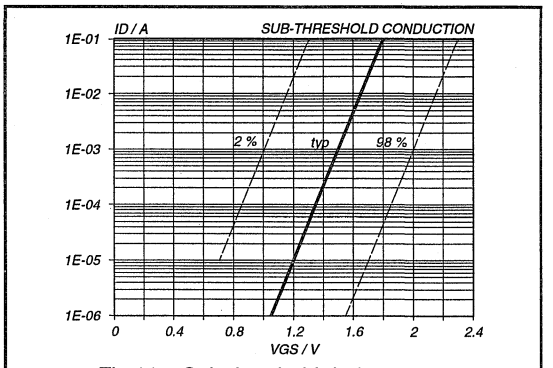


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

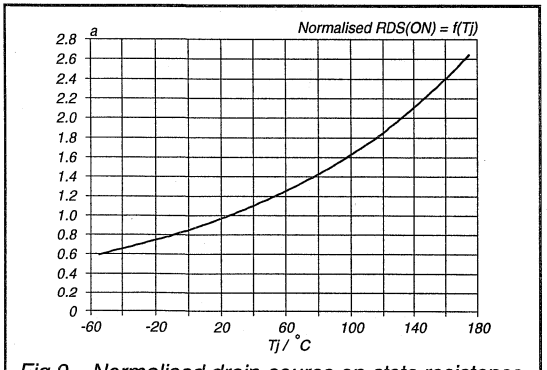


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 7 A; V_{GS} = 5 V

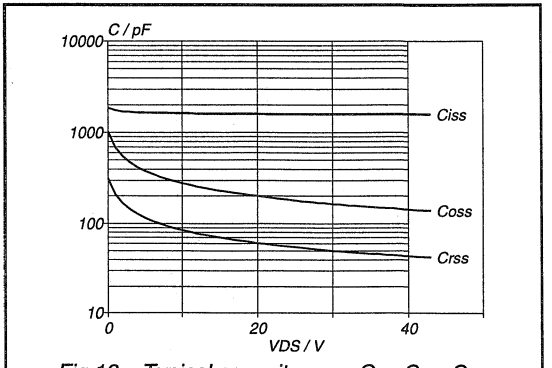


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

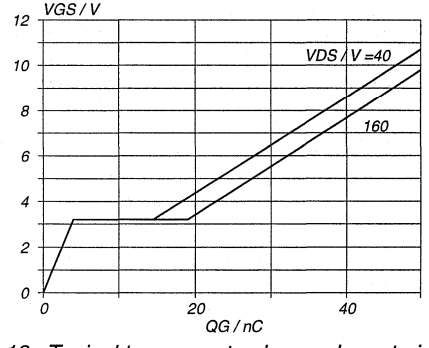


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

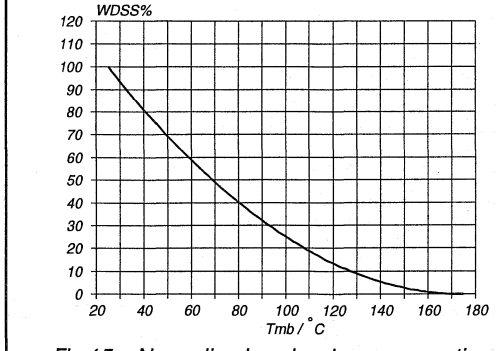


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

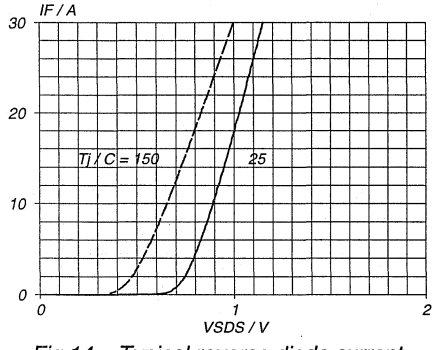


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

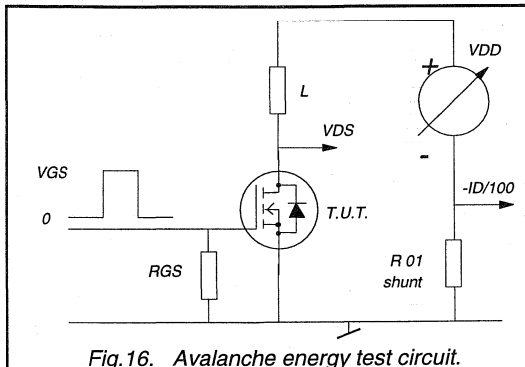


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK566-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

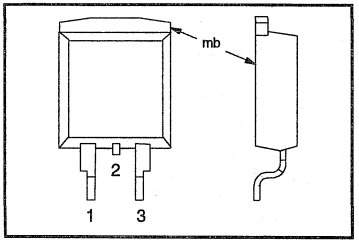
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	50	A
P_{tot}	Total power dissipation	150	W
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	26	mΩ

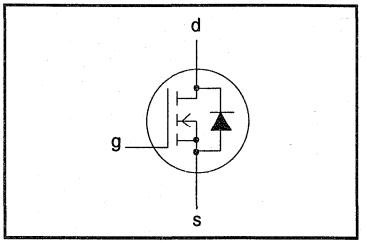
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	50	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	38	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	200	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 boards (see. Fig 18).	-	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	20	26	mΩ

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	17	30	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2800	pF
C_{oss}	Output capacitance		-	700	1000	pF
C_{rss}	Feedback capacitance		-	280	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	40	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V;	-	150	250	ns
$t_{d\,off}$	Turn-off delay time	R_{GS} = 50 Ω;	-	350	450	ns
t_f	Turn-off fall time	R_{gen} = 50 Ω	-	190	250	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	50	A
I_{DRM}	Pulsed reverse drain current	-	-	-	200	A
V_{SD}	Diode forward voltage	I_F = 50 A ; V_{GS} = 0 V	-	1.1	2.0	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A ; V_{DD} ≤ 25 V ; V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	150	mJ

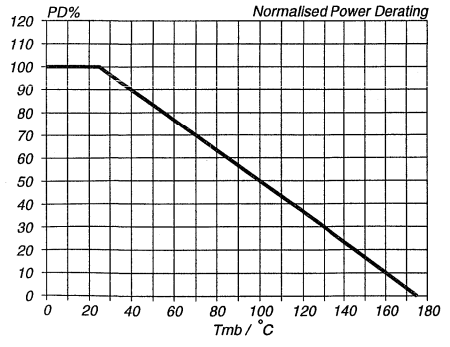


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

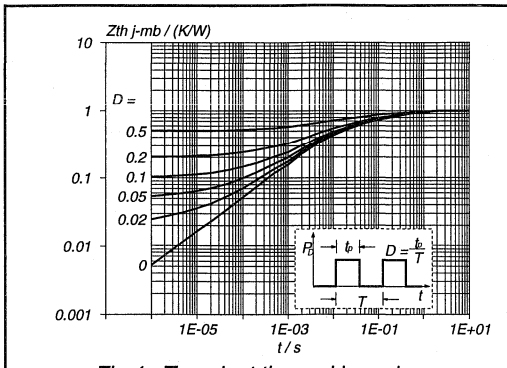


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

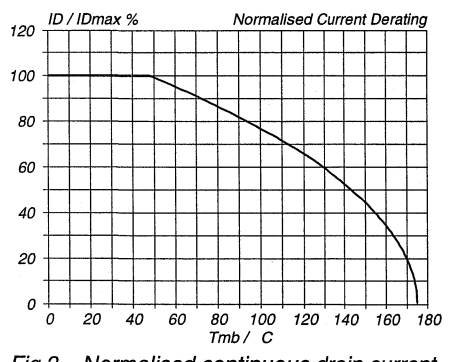


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

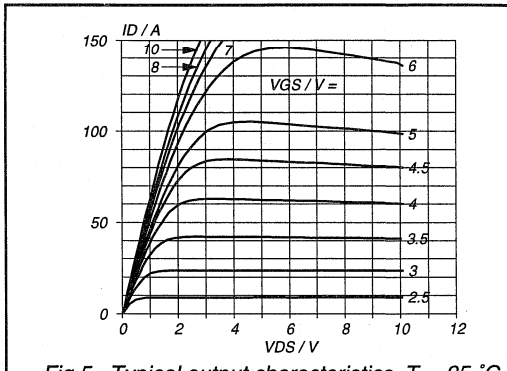


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

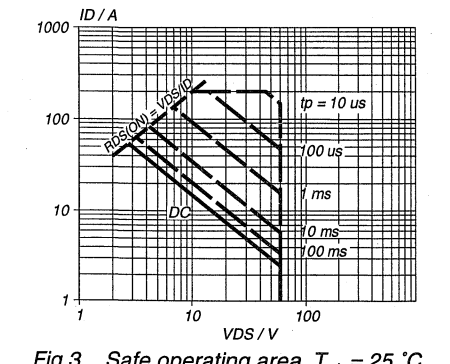


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

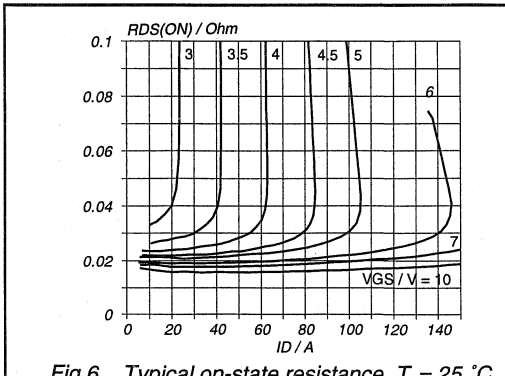


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

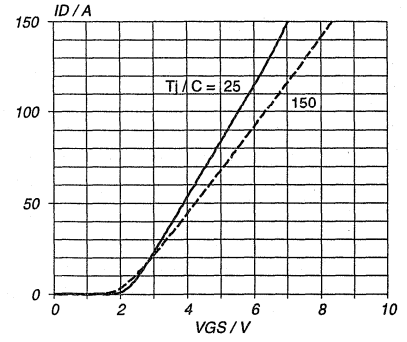


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

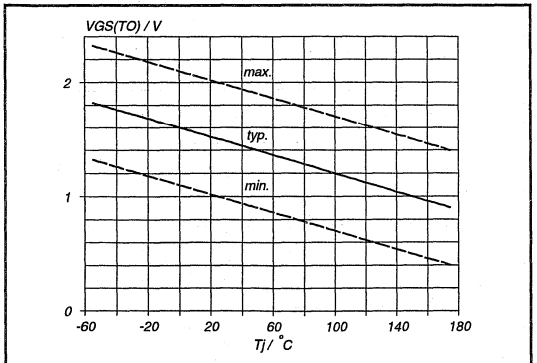


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

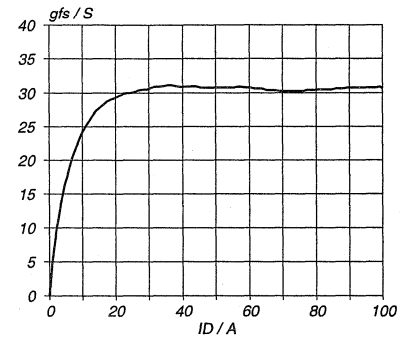


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 15$ V

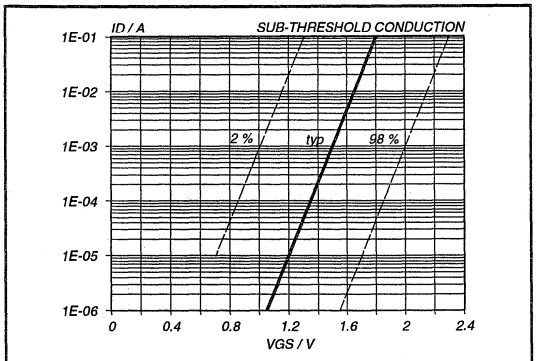


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

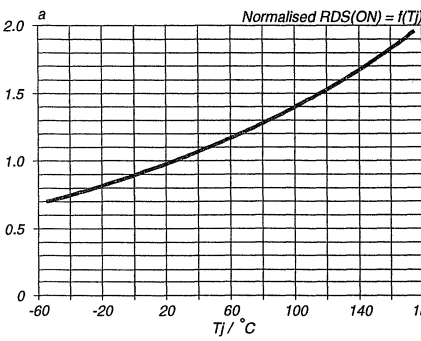


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 5$ V

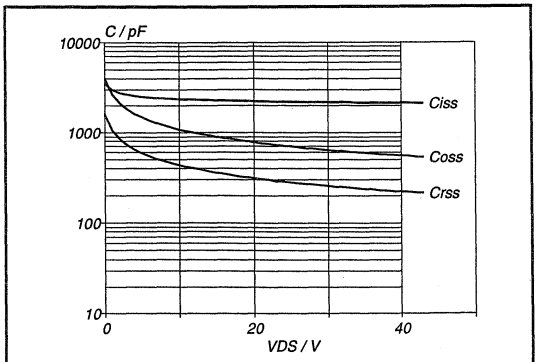


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

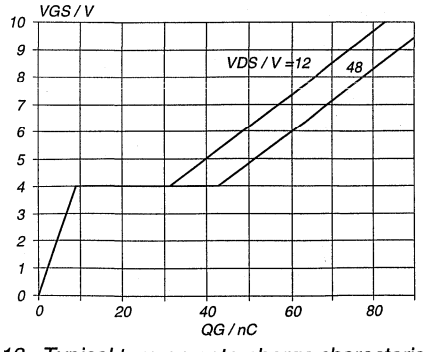


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

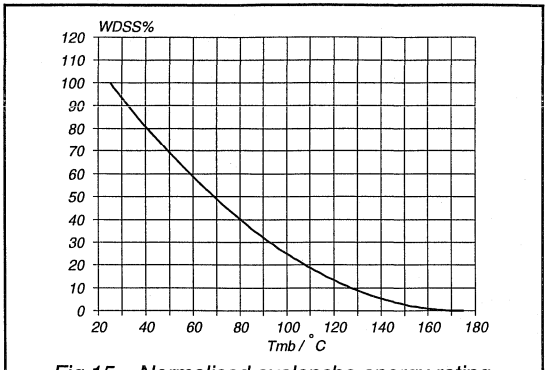


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 25$ A

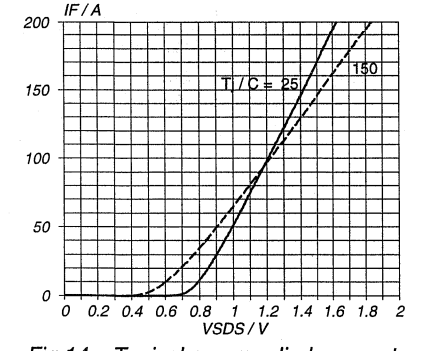


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

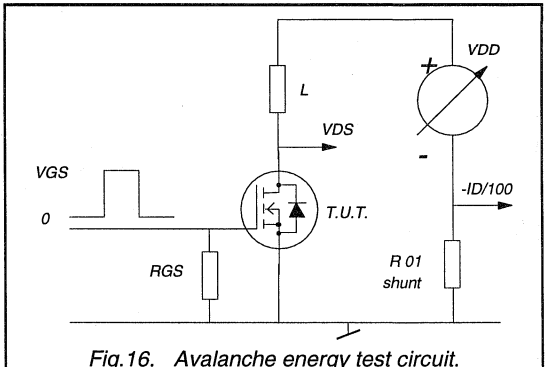


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK566-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

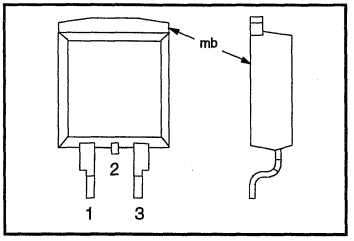
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	60	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	22	mΩ

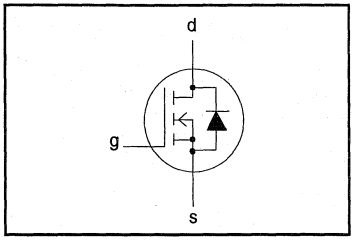
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	60	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	44	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb}= 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; i_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	18	22	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	17	30	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2800	pF
C_{oss}	Output capacitance		-	700	1000	pF
C_{rss}	Feedback capacitance		-	280	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	40	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	150	250	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	350	450	ns
t_f	Turn-off fall time		-	190	250	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	60	A
I_{DRM}	Pulsed reverse drain current	-	-	-	240	A
V_{SD}	Diode forward voltage	I_F = 50 A; V_{GS} = 0 V	-	1.1	2.0	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	150	mJ

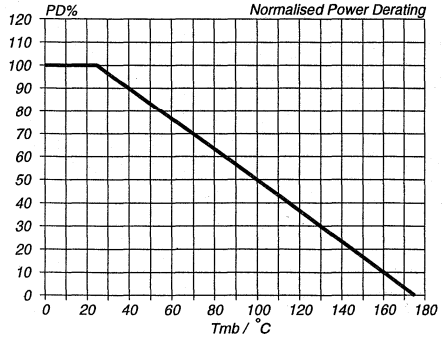


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

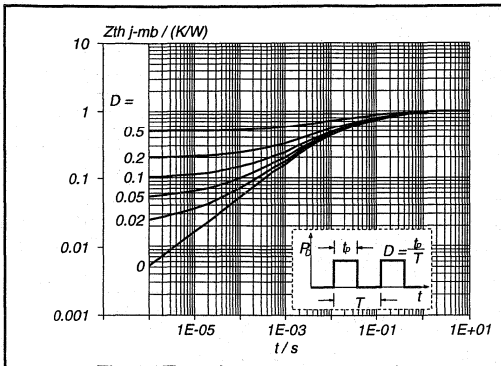


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

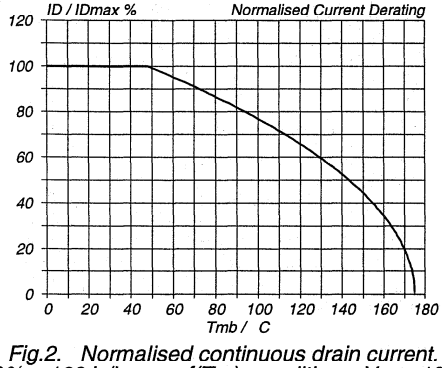


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

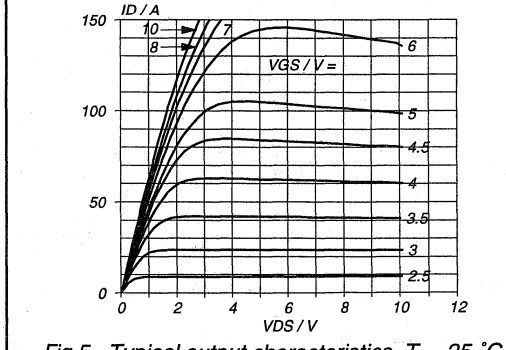


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

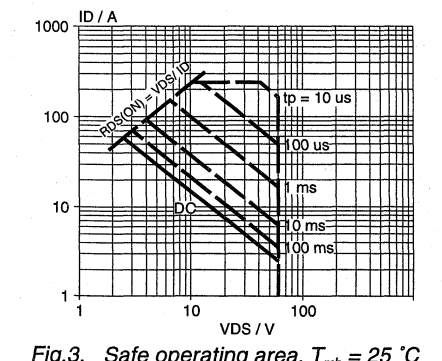


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

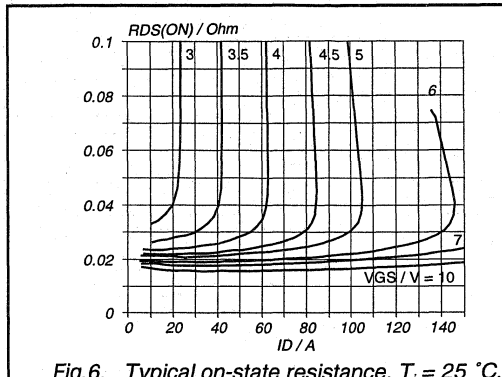


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

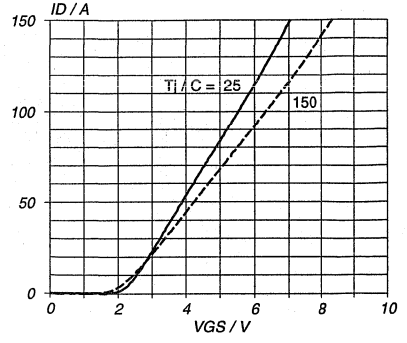


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

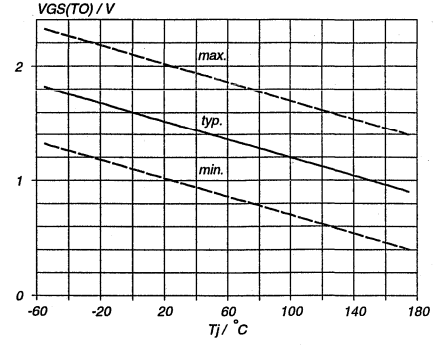


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

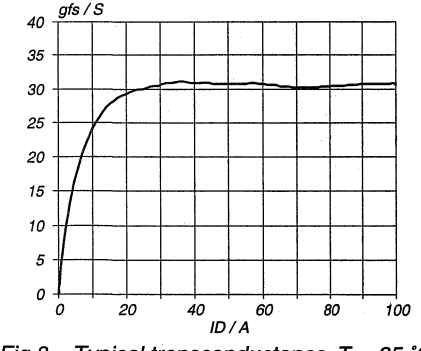


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

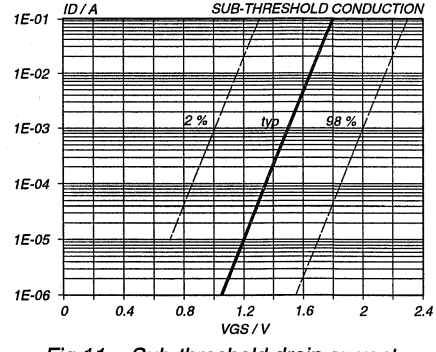


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

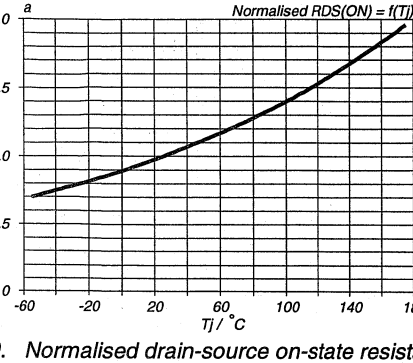


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

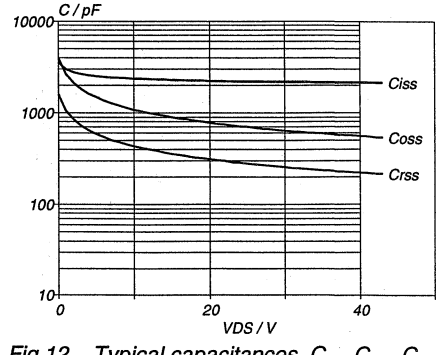


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

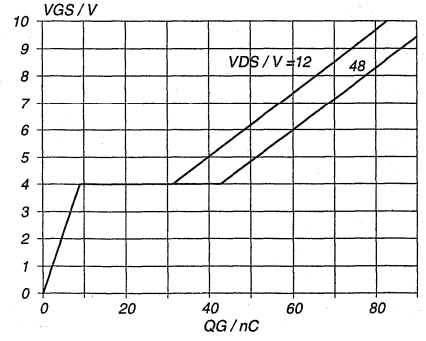


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

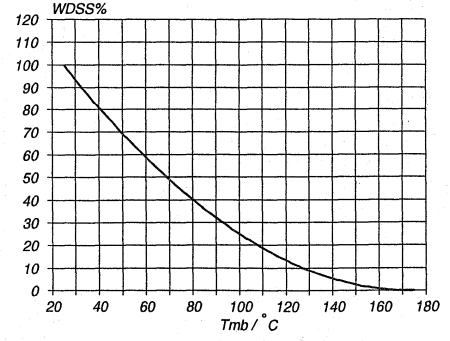


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 50$ A

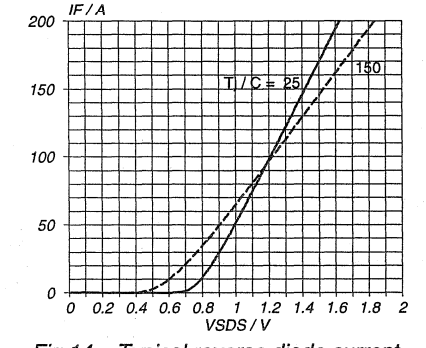


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

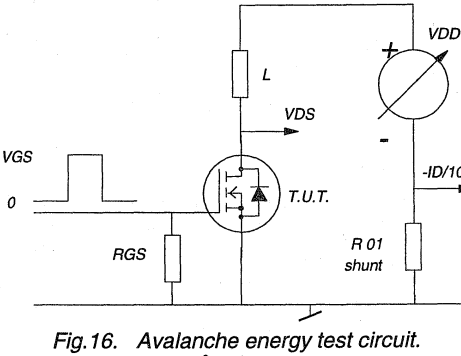


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Clamped logic level FET

BUK573-48C

GENERAL DESCRIPTION

Protected N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.

The device is intended for use in automotive applications. It has built-in zener diodes providing active drain voltage clamping.

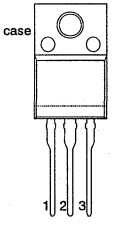
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamp voltage	40	48	58	V
I_D	Drain current (DC)			13	A
P_{tot}	Total power dissipation			25	W
W_{DSRR}	Repetitive clamped turn off energy; T_j = 150˚C			50	mJ
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V			85	mΩ

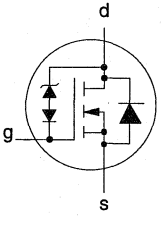
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	continuous	-	30	V
V_{DG}	Drain-gate voltage	continuous	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{hs} = 25 ˚C	-	13	A
I_D	Drain current (DC)	T_{hs} = 100 ˚C	-	8.2	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 ˚C	-	52	A
P_{tot}	Total power dissipation	T_{hs} = 25 ˚C	-	25	W
T_{stg}	Storage temperature	-	- 55	150	˚C
T_j	Junction Temperature	-	- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DG}$	Drain-gate zener voltage	$0.2 \leq -I_G \leq 0.4$ mA; $-55°C \leq T_j \leq 150°C$	38	45	54	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	1.0	1.5	2.0	V
$V_{GS(ON)}$	Gate voltage	V_{DS} = 10 V; I_D = 10 A; $-55°C \leq T_j \leq 150°C$	2.0	3.1	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V; T_j =150 °C	-	0.01	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V; T_j =150 °C	-	0.1	10	µA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A	-	65	85	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain source clamp voltage (peak value)	R_G = 10 kΩ; I_D = 10 A; $-55 \leq T_j \leq 150°C$; Inductive load.	40	48	58	V
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	7	12	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	550	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	100	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 12 V; I_D = 5 A;	-	3.5	-	µs
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 kΩ;	-	22	-	µs
$t_{d\,off}$	Turn-off delay time		-	16	-	µs
t_f	Turn-off fall time		-	18	-	µs
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{isol(rms)}$	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65 %; clean and dust free	-	-	2500	V_{RMS}
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.05	1.3	V

CLAMPED ENERGY LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSRS}	Drain-source non repetitive clamped inductive turn off energy	T_j = 25°C prior to clamping; I_D = 10 A; V_{GS} = 5 V; R_{GS} = 10 kΩ; inductive load (see Figs. 17,18)	-	200	mJ
W_{DSRR}	Drain-source repetitive clamped inductive turn off energy	T_j = 150°C prior to clamping; I_D = 10 A; V_{GS} = 5 V; R_{GS} = 10 kΩ; inductive load (see Figs. 17,18)	-	50	mJ

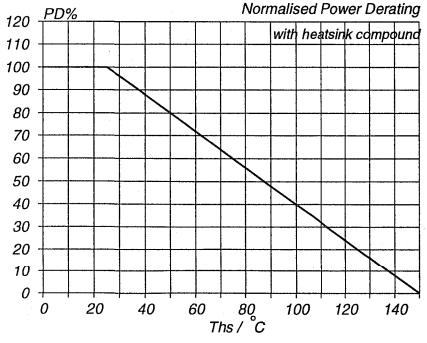


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{hs})

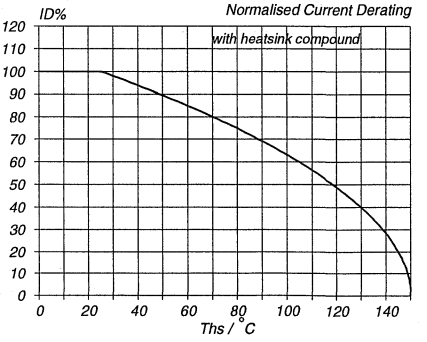


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{hs}); conditions: V_{GS} ≥ 5 V

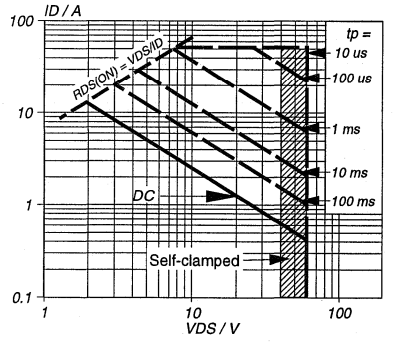


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

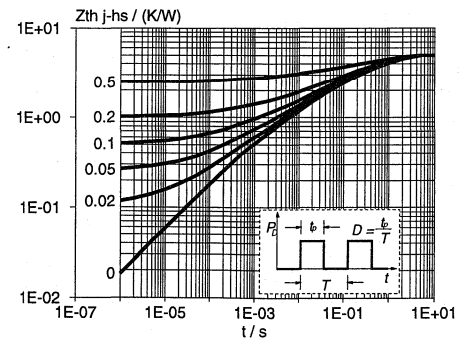


Fig.6. Transient thermal impedance.
$Z_{th\ j\text{-}hs}$ = f(t); parameter D = t_p/T

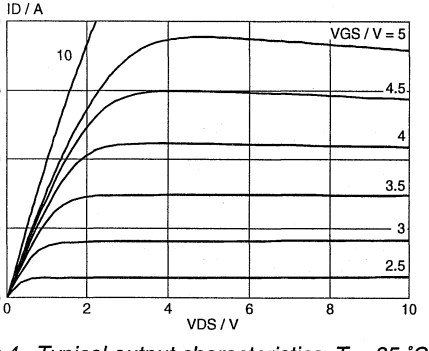


Fig.4. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

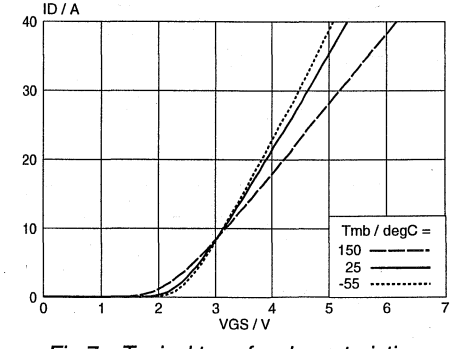


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V.

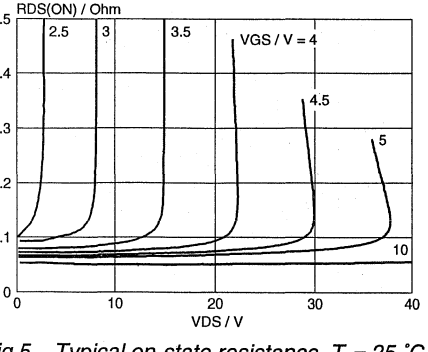


Fig.5. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

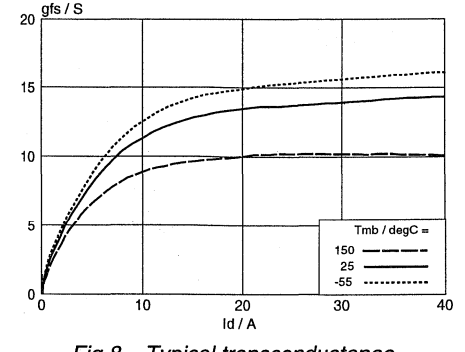


Fig.8. Typical transconductance.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

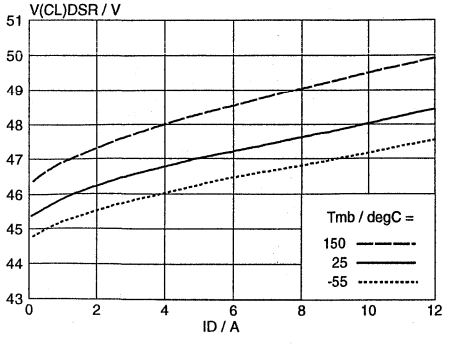


Fig.9. Typical clamping voltage
$V_{(CL)DSR} = f(I_D)$; *conditions:* $R_G = 10\ k\Omega$

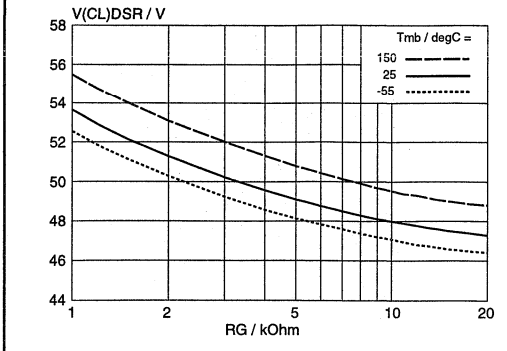


Fig.12. Typical clamping voltgage
$V_{(CL)DSR} = f(R_G)$; *conditions:* $I_D = 10$ *A.*

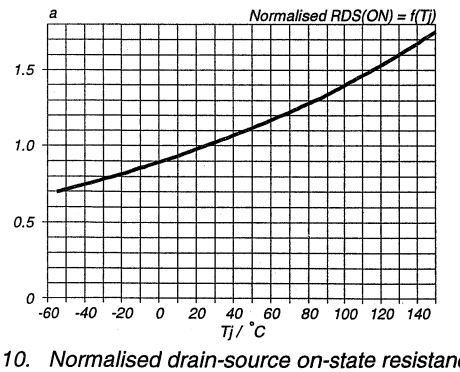


Fig.10. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 10$ *A;* $V_{GS} = 5$ *V*

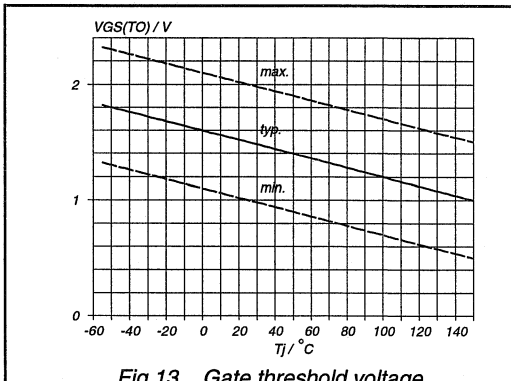


Fig.13. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; *conditions:* $I_D = 1$ *mA;* $V_{DS} = V_{GS}$

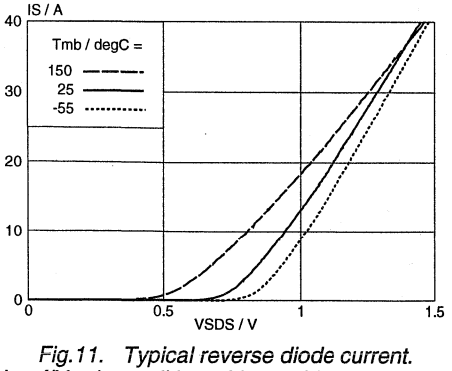


Fig.11. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ *V; parameter* T_j

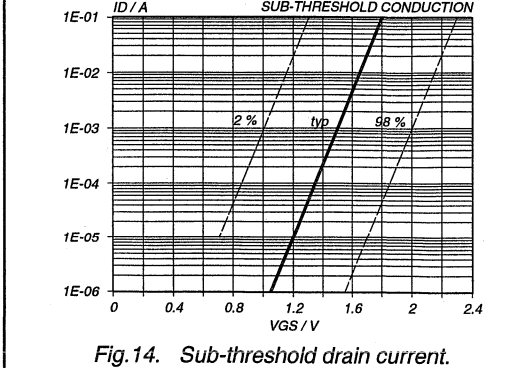


Fig.14. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ *°C;* $V_{DS} = V_{GS}$

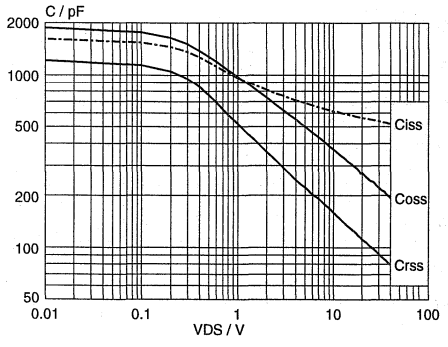


Fig.15. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

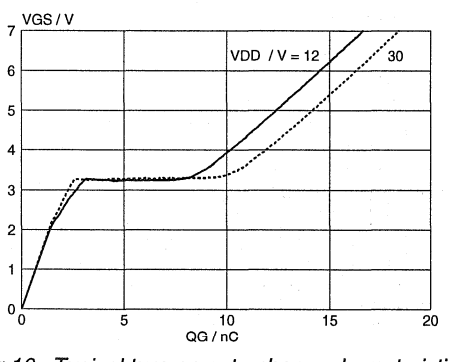


Fig.16. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 10$ A.

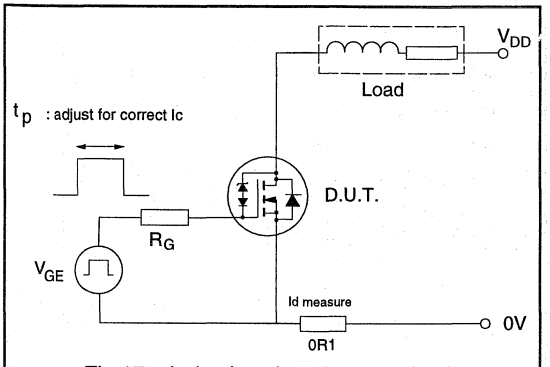


Fig.17. Inductive clamping test circuit.

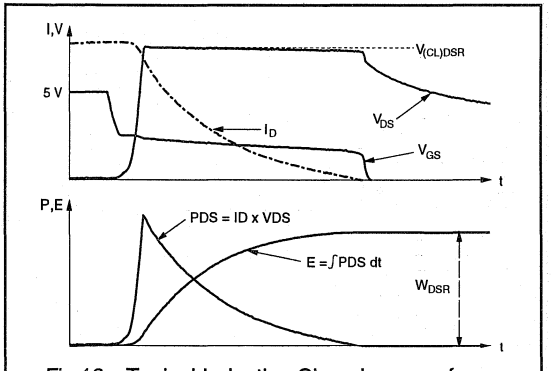


Fig.18. Typical Inductive Clamping waveforms

PowerMOS transistor
Logic level FET

BUK574-60H

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

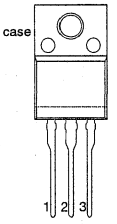
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	20	A
P_{tot}	Total power dissipation	30	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	42	mΩ

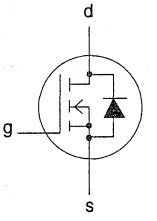
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	20	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	13.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	80	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	With heatsink compound	-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A	-	34	42	mΩ

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	10	18	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	1750	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	25	40	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	110	150	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	150	220	ns
t_f	Turn-off fall time		-	100	145	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	20	A
I_{DRM}	Pulsed reverse drain current	-	-	-	80	A
V_{SD}	Diode forward voltage	I_F = 20 A ; V_{GS} = 0 V	-	0.9	2.0	V
t_{rr}	Reverse recovery time	I_F = 20 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	i_D = 41 A ; $V_{DD} \leq$ 25 V ; T_{hs} = 25 °C V_{GS} = 5 V ; R_{GS} = 50 Ω	-	-	90	mJ

PowerMOS transistor Logic level FET

BUK581-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

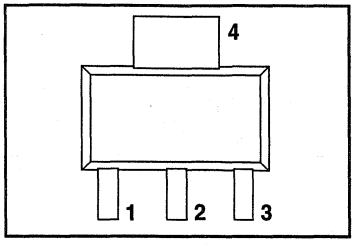
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	1.5	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.40	Ω

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



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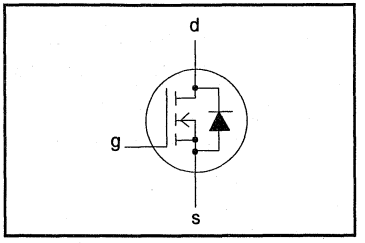


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1.5	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	6	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.5	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point[1]	Mounted on any PCB .	-	14	17	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	85	K/W

1 Temperature measured at solder joint on drain tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 1.5 A	-	0.28	0.40	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.5 A	1.0	2.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	170	300	pF
C_{oss}	Output capacitance		-	60	100	pF
C_{rss}	Feedback capacitance		-	25	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	7	10	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	15	25	ns
t_f	Turn-off fall time		-	25	35	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.5	A
I_{DRM}	Pulsed reverse drain current	-	-	-	6	A
V_{SD}	Diode forward voltage	I_F = 1.5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1.5 A; -dI_F/dt = 100 A/µs;	-	30	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	50	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non repetitive unclamped inductive turn-off energy	I_D = 1.5 A ; $V_{DD} \leq$ 25 V V_{GS} = 5 V ; R_{GS} = 50 Ω T_{amb} = 25 °C	-	-	10	mJ

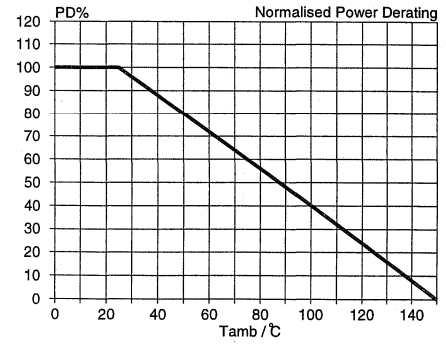


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

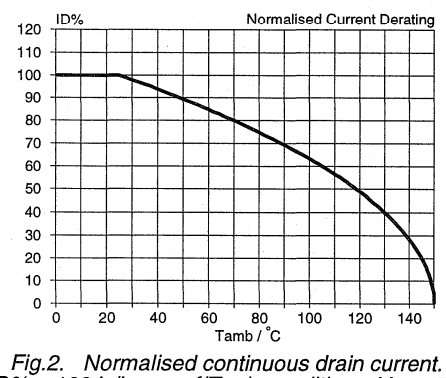


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 5 V

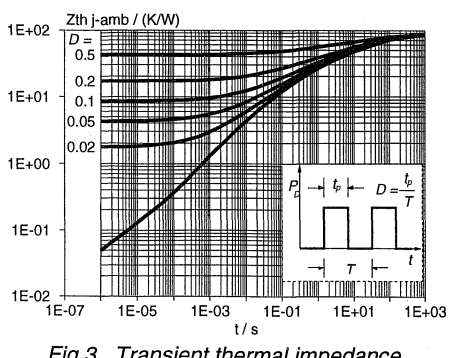


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

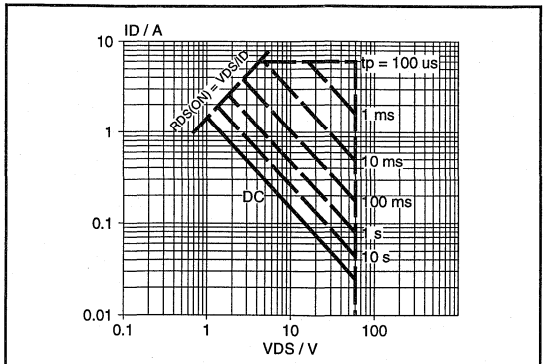


Fig.4. Safe operating area T_{amb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

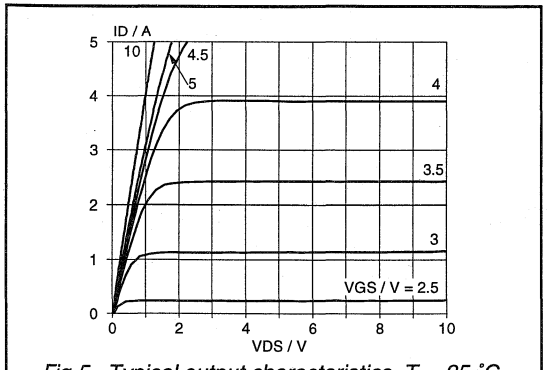


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

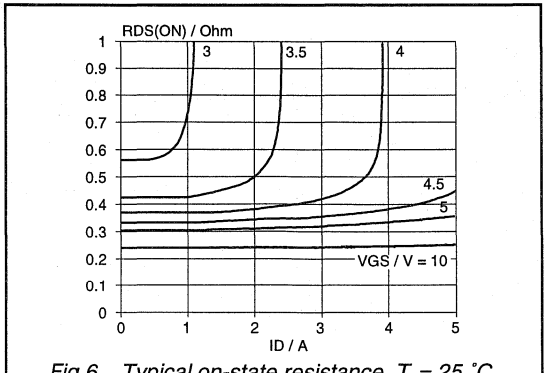


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

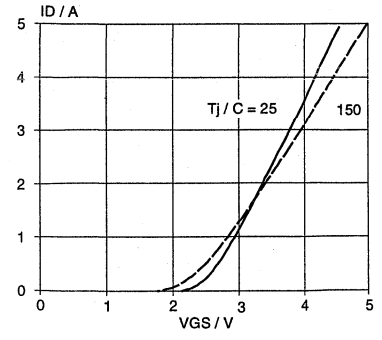


Fig.7. Typical transfer characteristics.
I_D = f(V_{GS}) ; conditions: V_{DS} = 25 V; parameter T_j

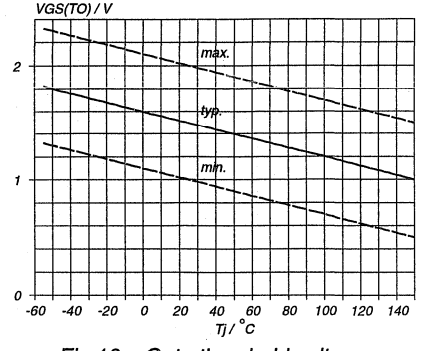


Fig.10. Gate threshold voltage.
$V_{GS(TO)}$ = f(T_j); conditions: I_D = 0.1 mA; V_{DS} = V_{GS}

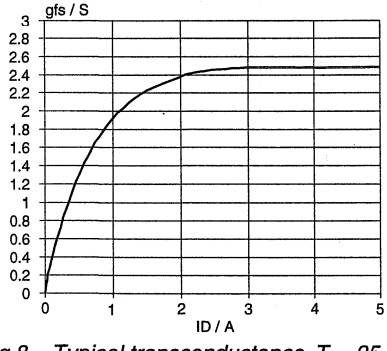


Fig.8. Typical transconductance, T_j = 25 °C.
g_{fs} = f(I_D); conditions: V_{DS} = 25 V

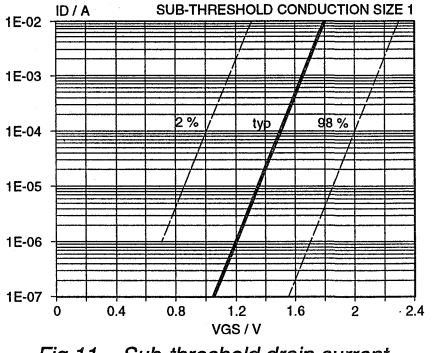


Fig.11. Sub-threshold drain current.
I_D = f(V_{GS}); conditions: T_j = 25 °C; V_{DS} = V_{GS}

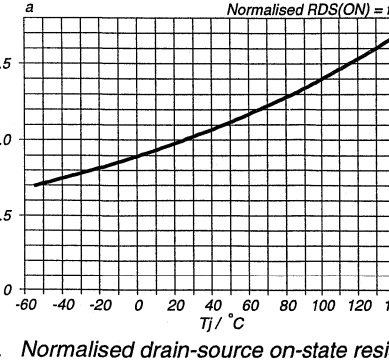


Fig.9. Normalised drain-source on-state resistance.
a = $R_{DS(ON)}$/$R_{DS(ON)25\,°C}$ = f(T_j); I_D = 1.5 A; V_{GS} = 5 V

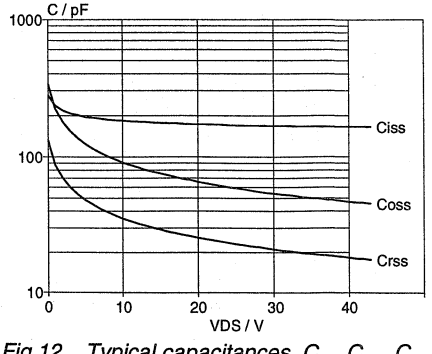


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

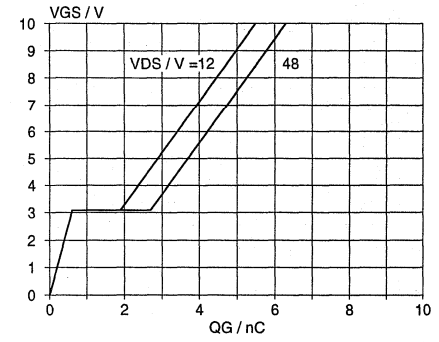


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 1.5$ A; parameter V_{DS}

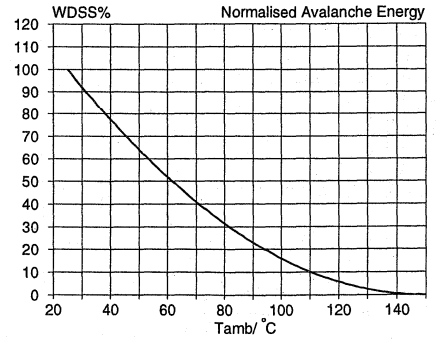


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1.5$ A

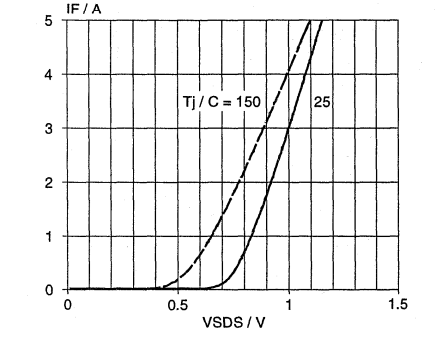


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

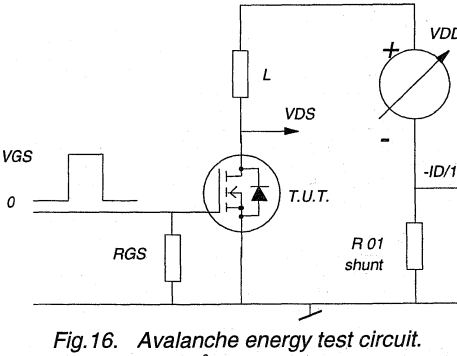


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor Logic level FET

BUK581-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

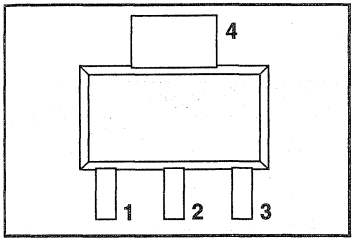
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	0.9	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.90	Ω

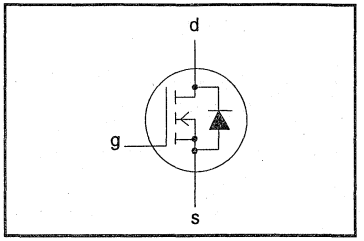
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	0.9	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	0.6	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	3.6	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.5	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB e.g. Fig.18	-	50	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	85	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 0.9 A	-	0.51	0.90	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 0.9 A	1	1.8	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	180	300	pF
C_{oss}	Output capacitance		-	45	60	pF
C_{rss}	Feedback capacitance		-	16	25	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	6	10	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	15	25	ns
t_f	Turn-off fall time		-	20	30	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	0.9	A
I_{DRM}	Pulsed reverse drain current	-	-	-	3.6	A
V_{SD}	Diode forward voltage	I_F = 0.9 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 0.9 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	100	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 0.9 A; V_{DD} ≤ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	10	mJ

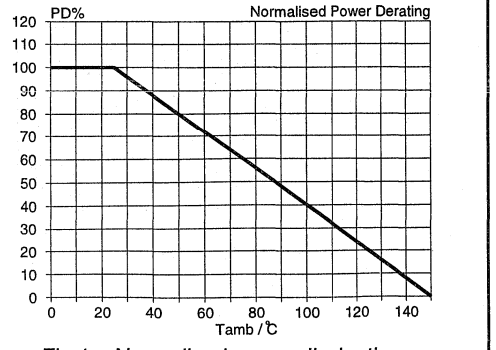


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

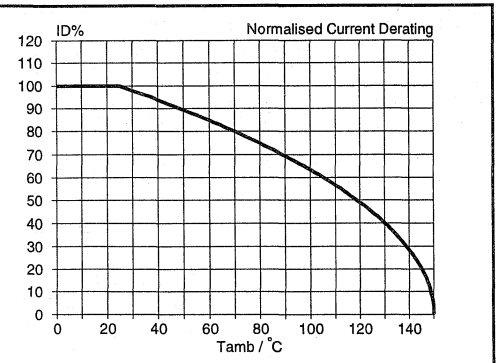


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 5 V

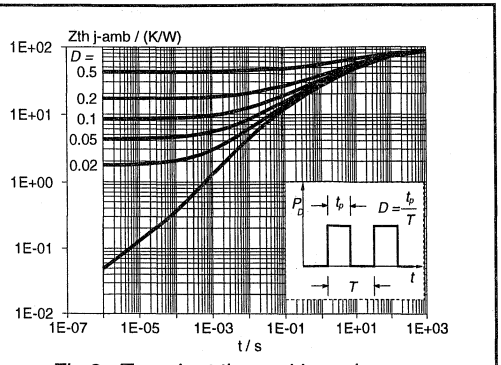


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

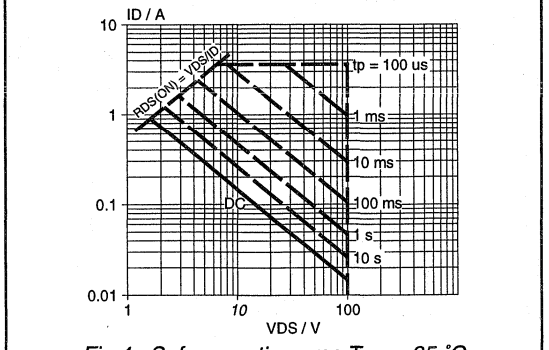


Fig.4. Safe operating area T_{amb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

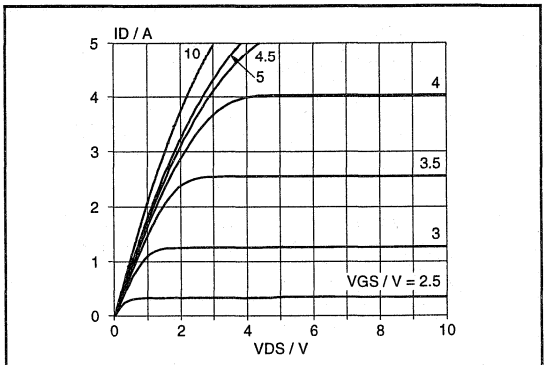


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

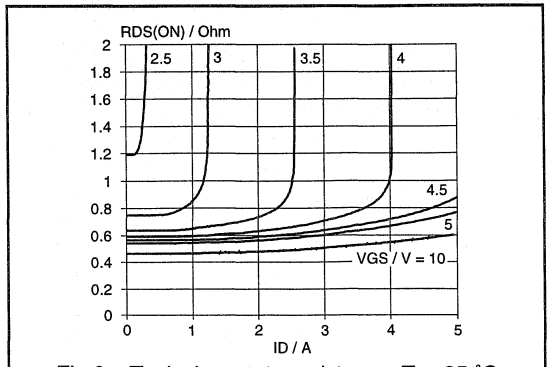


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

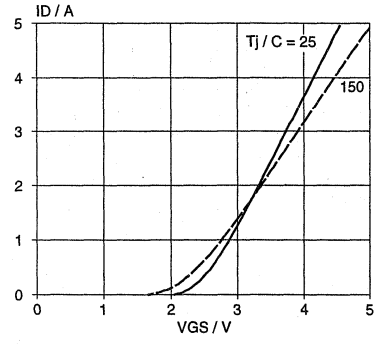


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

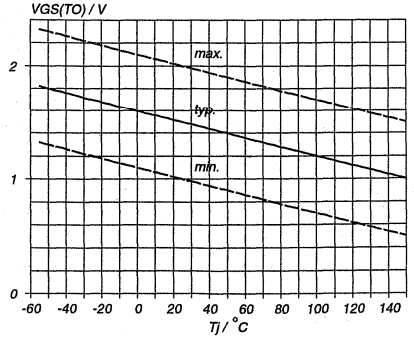


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.1$ mA; $V_{DS} = V_{GS}$

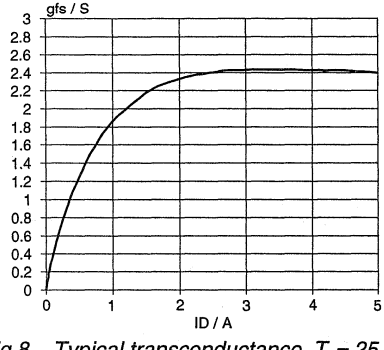


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

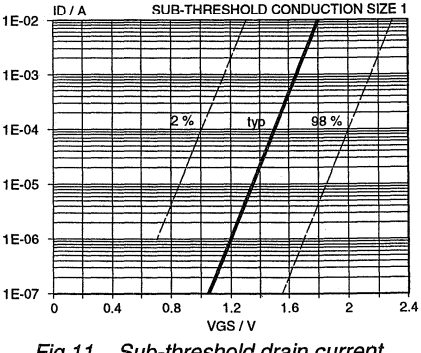


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

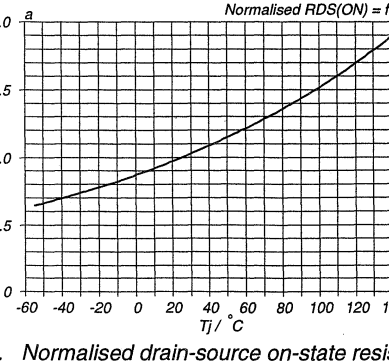


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 0.9$ A; $V_{GS} = 5$ V

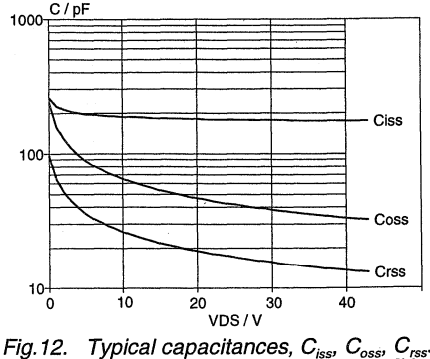


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

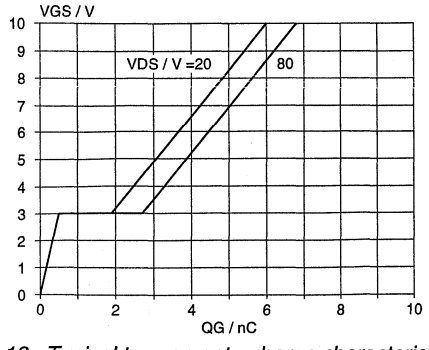


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 0.9$ A; parameter V_{DS}

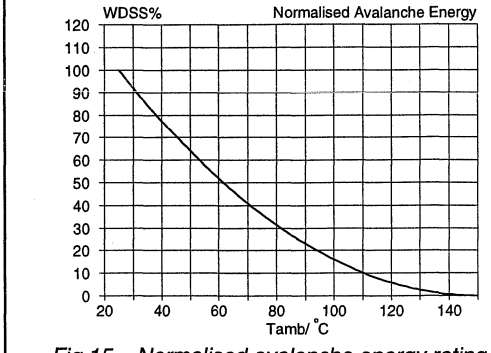


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 0.9$ A

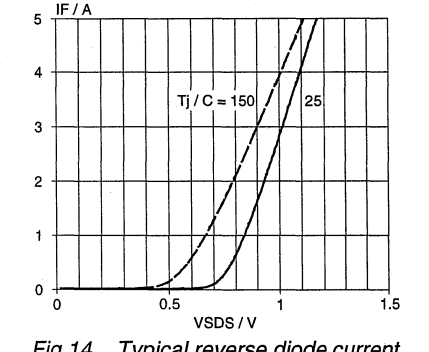


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

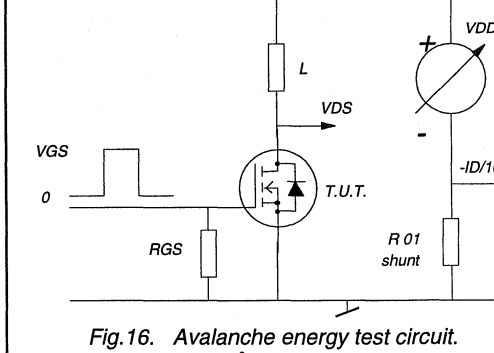


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Logic level FET

BUK582-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

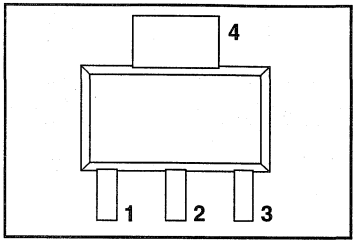
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	2.5	A
P_{tot}	Total power dissipation	1.7	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.15	Ω

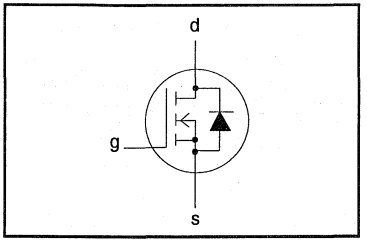
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	2.5	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1.5	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	10	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.7	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB e.g. Fig.18	-	40	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	75	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 2.5 A	-	0.12	0.15	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2.5 A	2	4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	350	600	pF
C_{oss}	Output capacitance		-	130	200	pF
C_{rss}	Feedback capacitance		-	50	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	50	80	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	40	70	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	2.5	A
I_{DRM}	Pulsed reverse drain current	-	-	-	10	A
V_{SD}	Diode forward voltage	I_F = 2.5 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 2.5 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	70	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.5 A; V_{DD} ≤ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	30	mJ

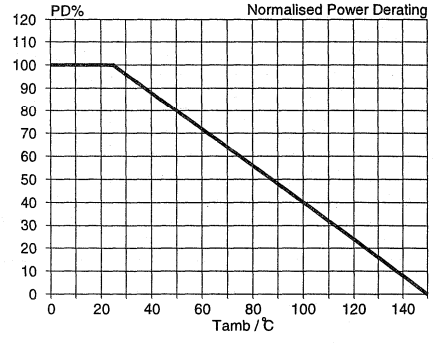


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

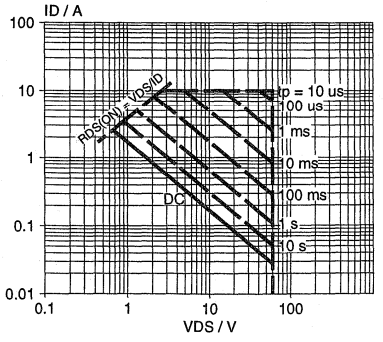


Fig.4. Safe operating area T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

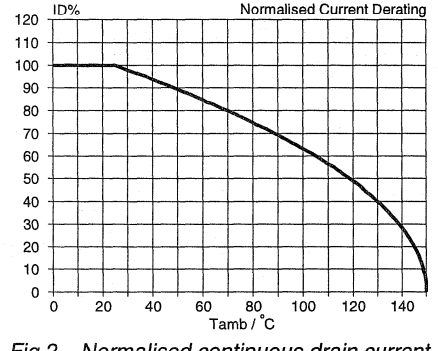


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 5 V

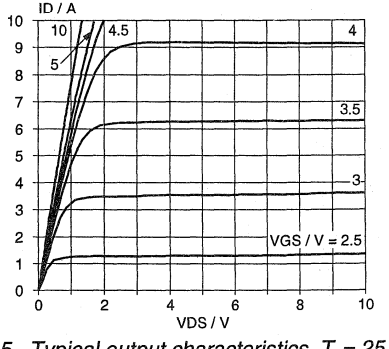


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

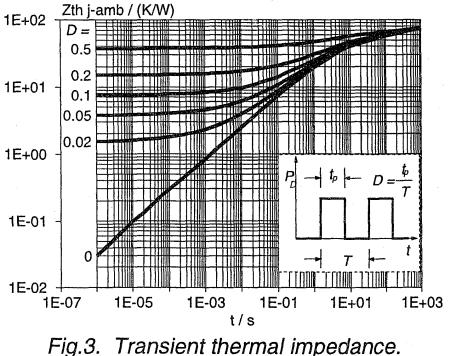


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

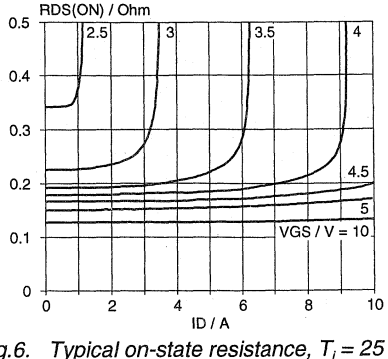


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

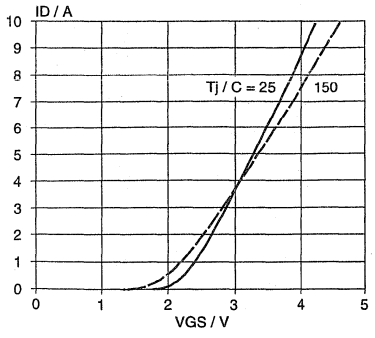


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

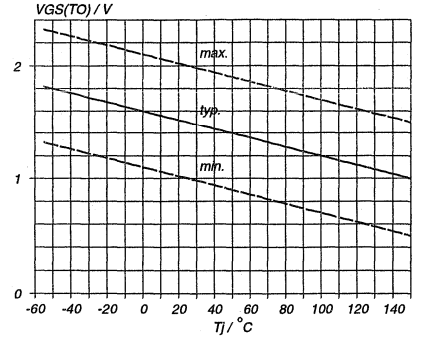


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

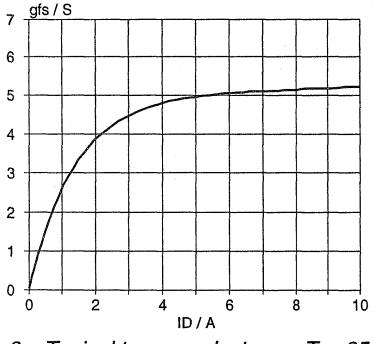


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

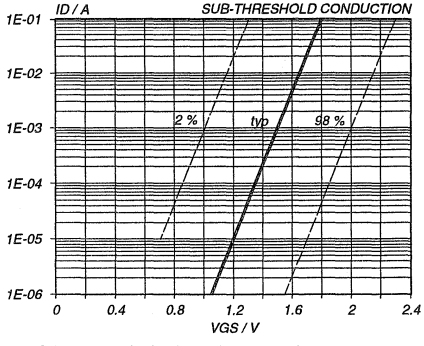


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

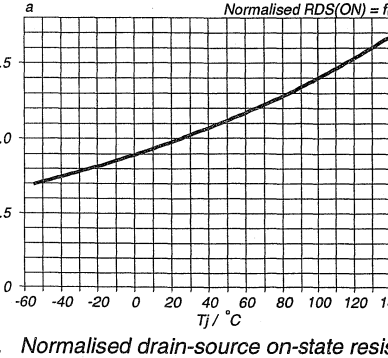


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 2.5 A; V_{GS} = 5 V

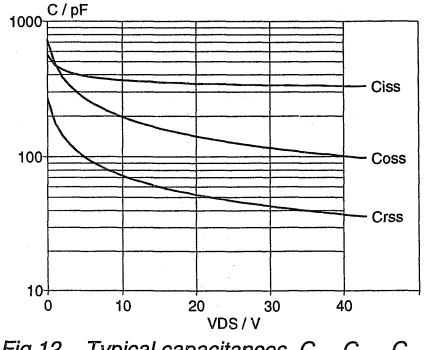


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

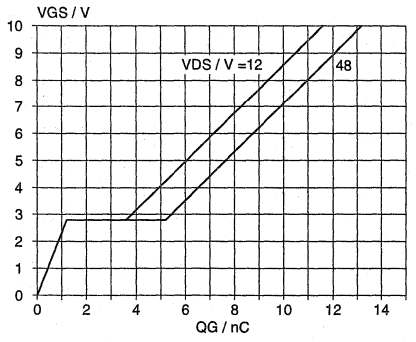


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 2.5$ A; parameter V_{DS}

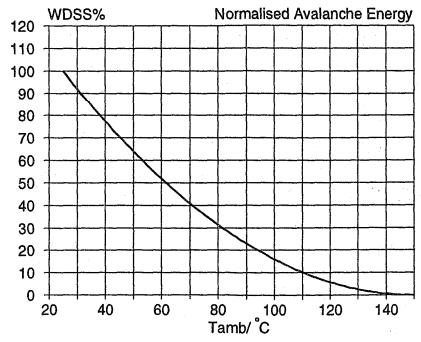


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 2.5$ A

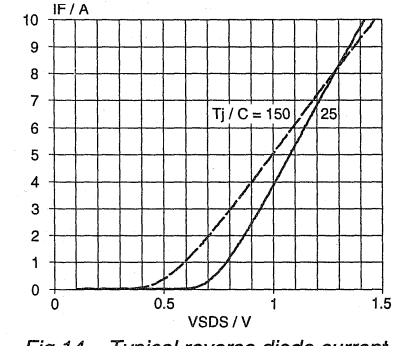


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

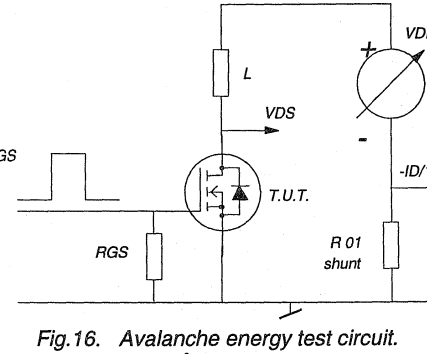


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK582-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

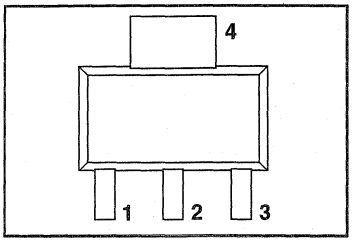
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	1.7	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.31	Ω

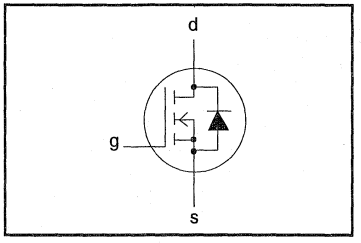
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	1.7	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	6.8	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.8	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}b}$	From junction to board[1]	Mounted on any PCB e.g. Fig.18	-	40	-	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	-	70	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 1.7 A	-	0.23	0.31	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.7 A	2	3	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	600	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	50	70	ns
t_f	Turn-off fall time		-	30	45	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.7	A
I_{DRM}	Pulsed reverse drain current	-	-	-	6.8	A
V_{SD}	Diode forward voltage	I_F = 1.7 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1.7 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.7 A; V_{DD} ≤ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	45	mJ

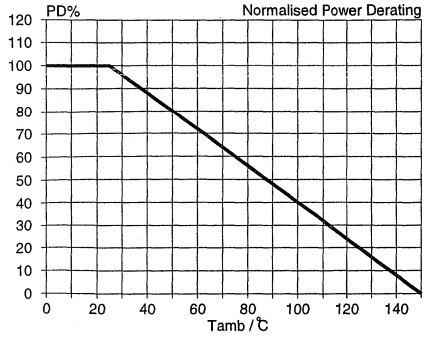


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{amb})

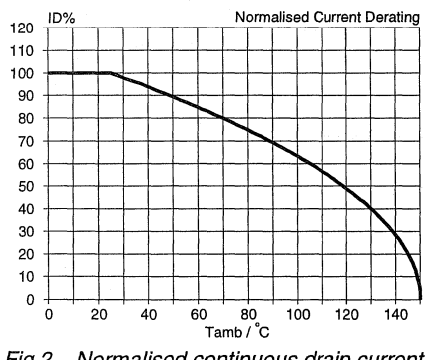


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{amb}); conditions: V_{GS} ≥ 5 V

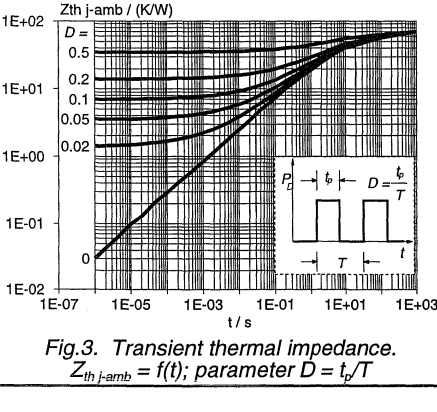


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

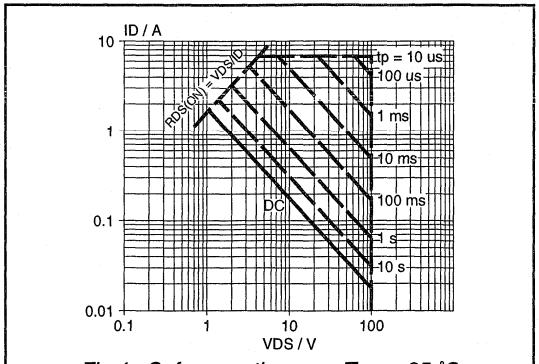


Fig.4. Safe operating area T_{amb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

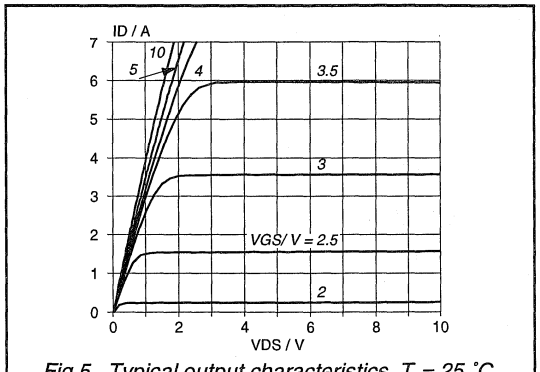


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

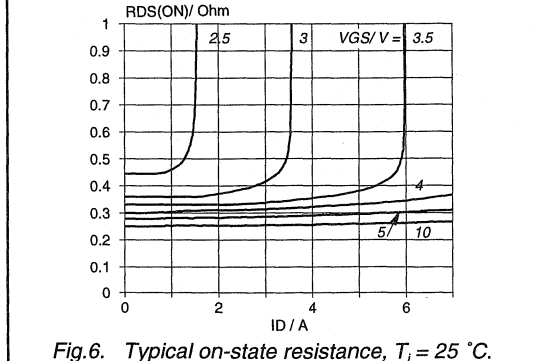


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

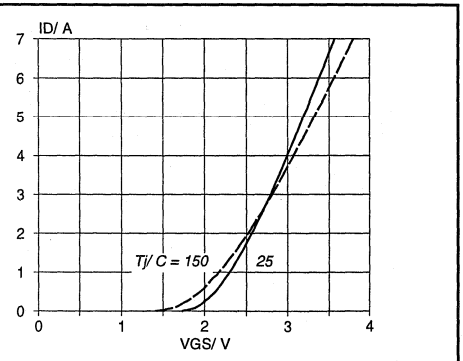


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

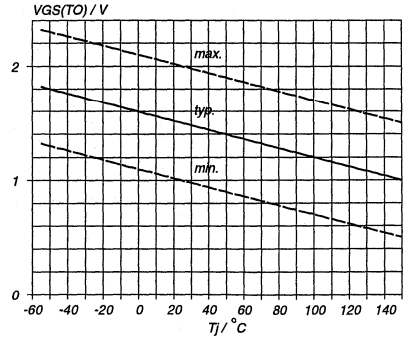


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

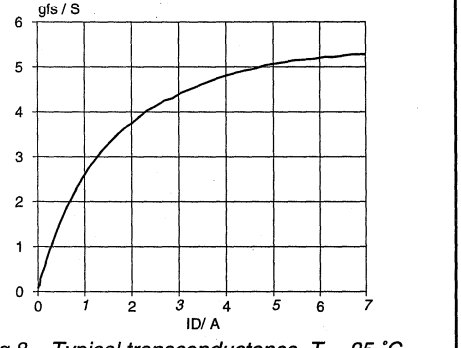


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

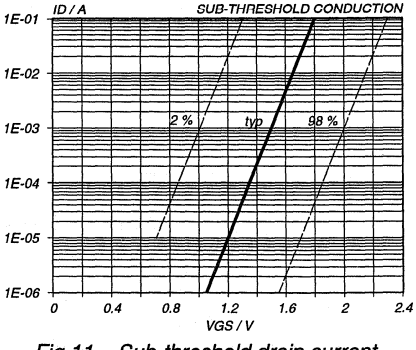


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

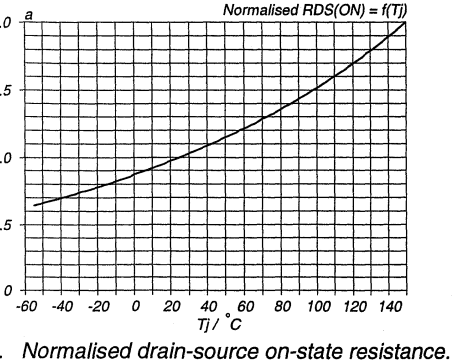


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.7 A; V_{GS} = 5 V

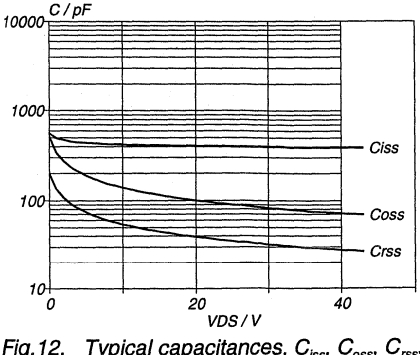


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

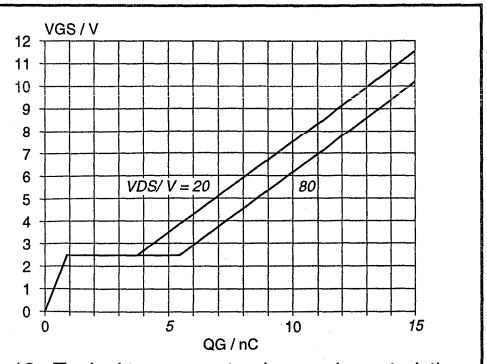


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 1.7$ A; parameter V_{DS}

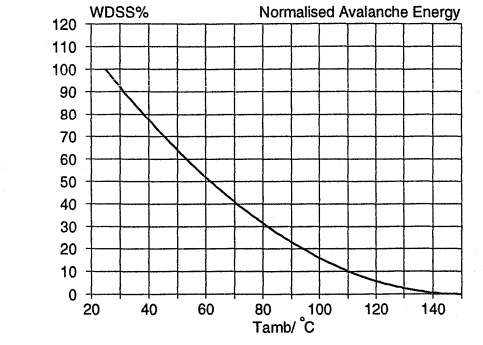


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 1.7$ A

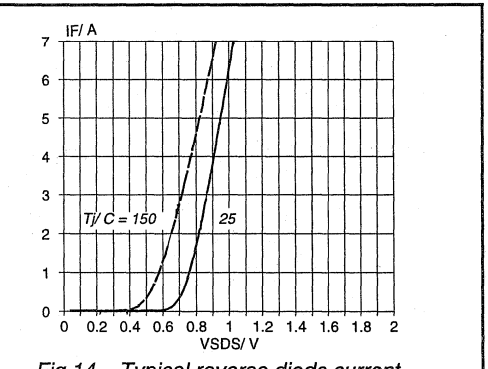


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

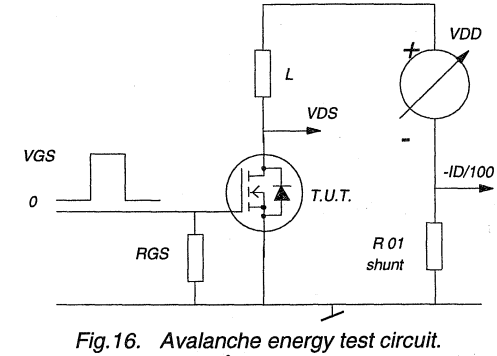


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor Logic level FET

BUK583-60A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

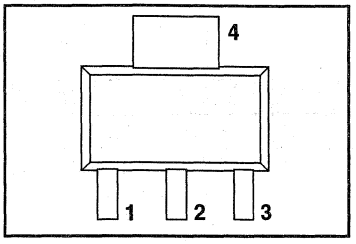
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	3.2	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.10	Ω

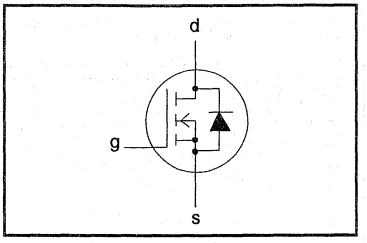
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	T_{amb} = 25 °C	-	3.2	A
I_D	Drain current (DC)	T_{amb} = 100 °C	-	2.0	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 °C	-	13	A
P_{tot}	Total power dissipation	T_{amb} = 25 °C	-	1.8	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	From junction to solder point[1]	Mounted on any PCB	-	12	15	K/W
$R_{th\ j\text{-}amb}$	From junction to ambient	Mounted on PCB of fig.18	-	-	70	K/W

1 Temperature measured at solder joint on drain tab.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	70	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 3.2 A	-	0.08	0.10	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.2 A	-	6.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	120	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_{GS} = 50 Ω;	-	35	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	55	80	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	3.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	13	A
V_{SD}	Diode forward voltage	I_F = 3.2 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 3.2 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.2 A; V_{DD} ≤ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{amb} = 25 °C	-	-	45	mJ

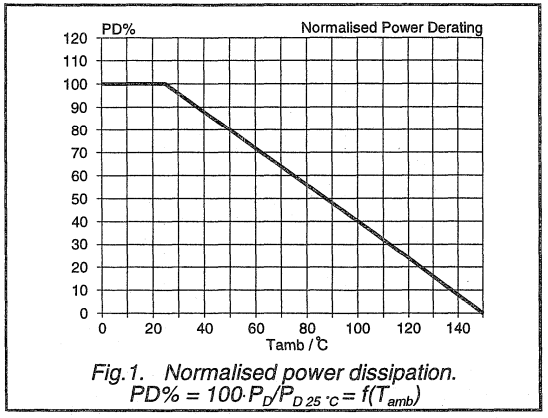


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{amb})

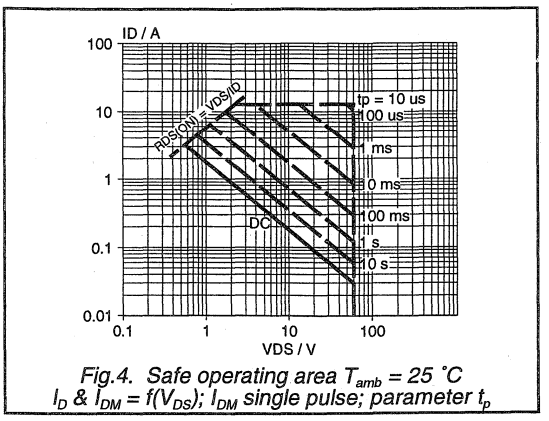


Fig.4. Safe operating area T_{amb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

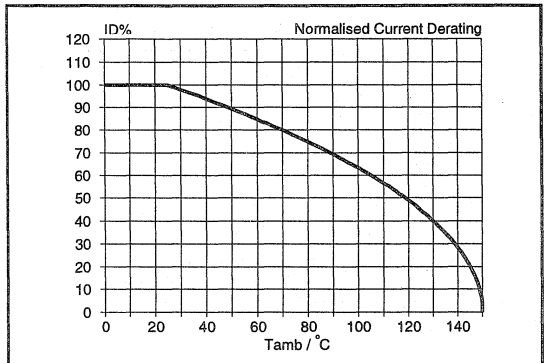


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{amb}); conditions: V_{GS} ≥ 5 V

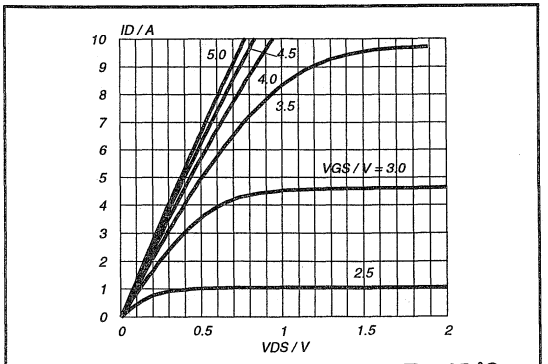


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

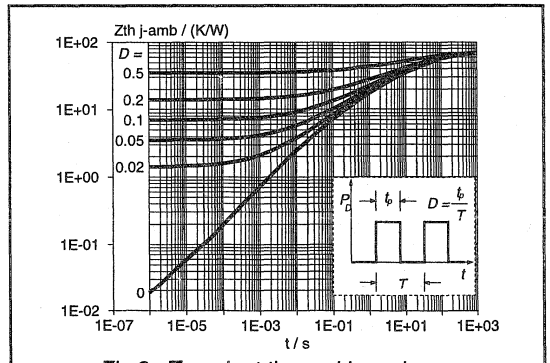


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb}$ = f(t); parameter D = t_p/T

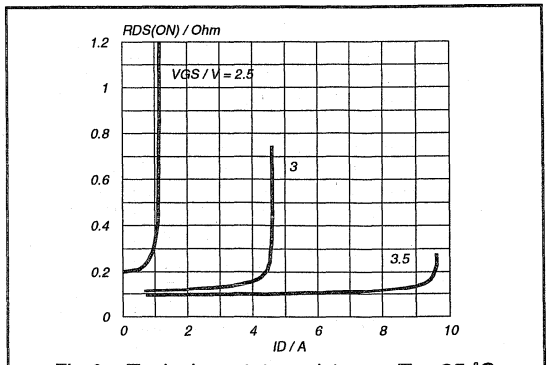


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

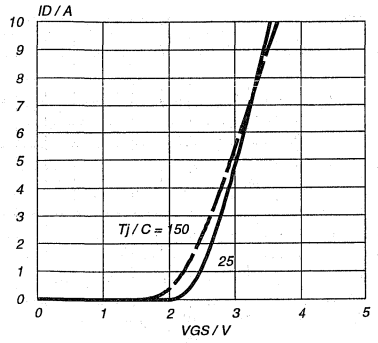


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

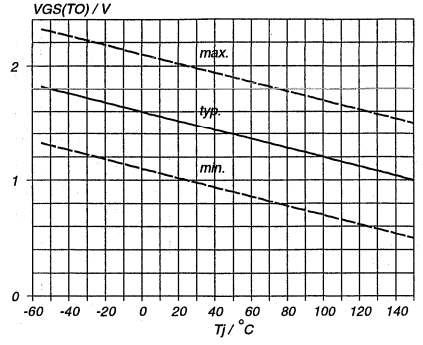


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

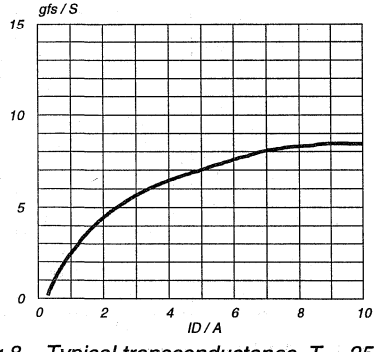


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

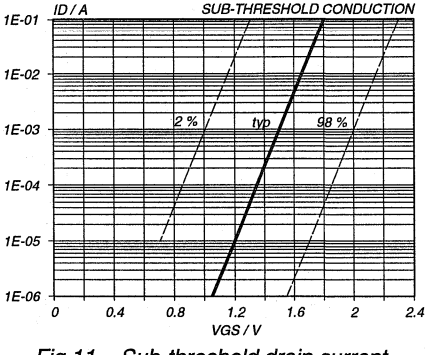


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

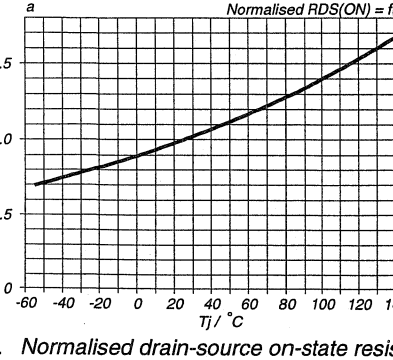


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.2 A; V_{GS} = 5 V

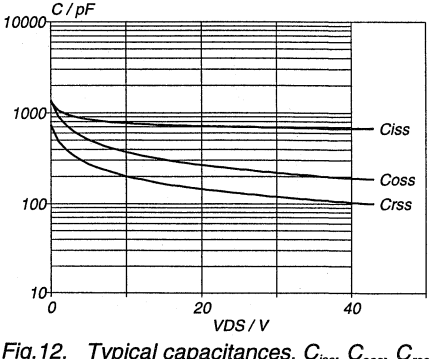


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

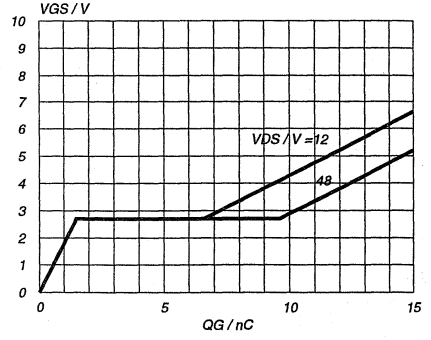


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 3.2$ A; parameter V_{DS}

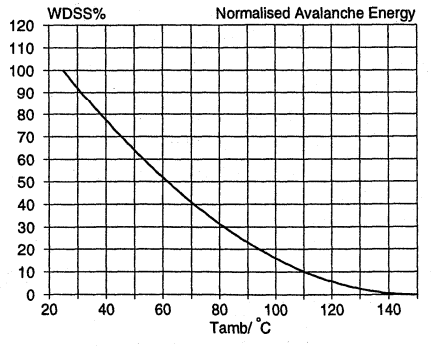


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 3.2$ A

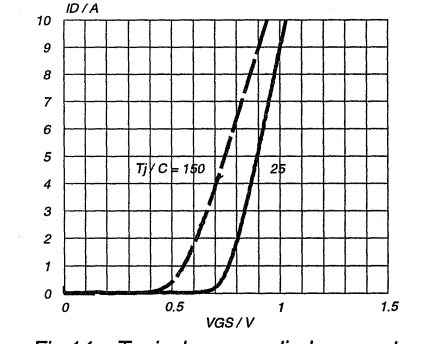


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

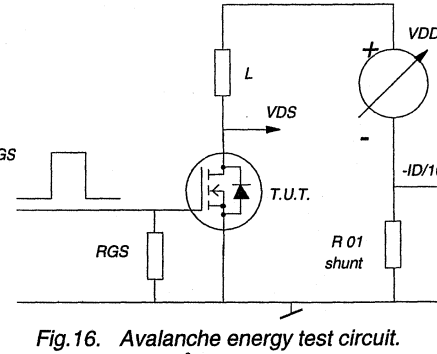


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

Insulated Gate Bipolar Transistor (IGBT) — BUK854-800A

GENERAL DESCRIPTION

Fast-switching N-channel insulated gate bipolar power transistor in a plastic envelope.
The device is intended for use in motor control, DC/DC and AC/DC converters, and in general purpose high frequency switching applications.

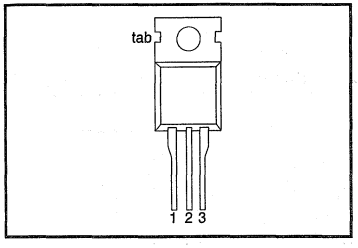
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CE}	Collector-emitter voltage	800	V
I_C	Collector current (DC)	12	A
P_{tot}	Total power dissipation	85	W
V_{CEsat}	Collector-emitter on-state voltage	3.5	V
E_{off}	Turn-off Energy Loss	0.5	mJ

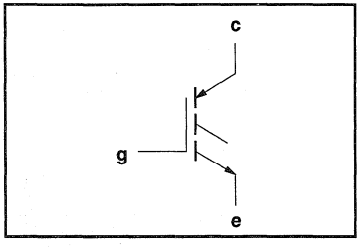
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collector-emitter voltage	-	-5	800	V
V_{CGR}	Collector-gate voltage	R_{GE} = 20 kΩ	-	800	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	30	V
I_C	Collector current (DC)	T_{mb} = 25 °C	-	12	A
I_C	Collector current (DC)	T_{mb} = 100 °C	-	6	A
I_{CLM}	Collector Current (Clamped Inductive Load)	$T_j \leq T_{jmax.}$ $V_{CL} \leq 500$ V	-	20	A
I_{CM}	Collector current (pulsed peak value, on-state)	$T_j \leq T_{jmax.}$	-	30	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	85	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.47	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V; I_C = 0.25 mA	800	-	-	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	3	4	5.5	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j = 25 °C	-	10	100	µA
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j =125 °C	-	0.1	1	mA
I_{ECS}	Reverse collector current	V_{CE} = -5 V; V_{GE} = 0 V	-	0.1	5	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±30 V; V_{CE} = 0 V	-	10	100	nA
V_{CEsat}	Collector-emitter saturation voltage	V_{GE} = 15 V; I_C = 6 A	-	2.4	3.5	V
		V_{GE} = 15 V; I_C = 12 A	-	3.1	-	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 3 A	1.5	4	-	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	400	750	pF
C_{oes}	Output capacitance		-	45	80	pF
C_{res}	Feedback capacitance		-	15	40	pF
$t_{d\,on}$	Turn-on delay time	I_C = 6 A; V_{CC} = 500 V;	-	20	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	30	-	ns
E_{on}	Turn-on Energy Loss	T_j = 25°C;	-	0.25	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	170	270	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	200	400	ns
E_{off}	Turn-off Energy Loss	losses	-	0.25	0.5	mJ
$t_{d\,on}$	Turn-on delay time	I_C = 6 A; V_{CC} = 500 V;	-	20	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	30	-	ns
E_{on}	Turn-on Energy Loss	T_j = 125°C;	-	0.25	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	200	350	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	400	800	ns
E_{off}	Turn-off Energy Loss	losses	-	0.5	1	mJ

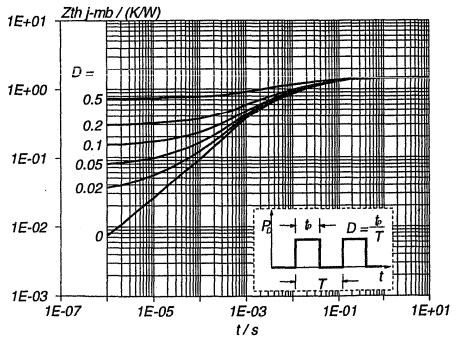


Fig.1. Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

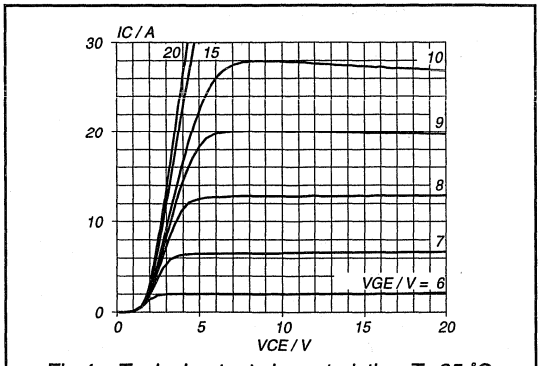


Fig.4. Typical output characteristics, T_j=25 °C. $I_C=f(V_{CE})$; parameter V_{GE}

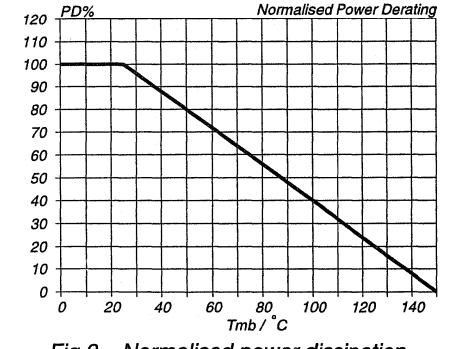


Fig.2. Normalised power dissipation. PD% = 100.$P_D/P_{D\ 25°C}$ = f(T_{mb})

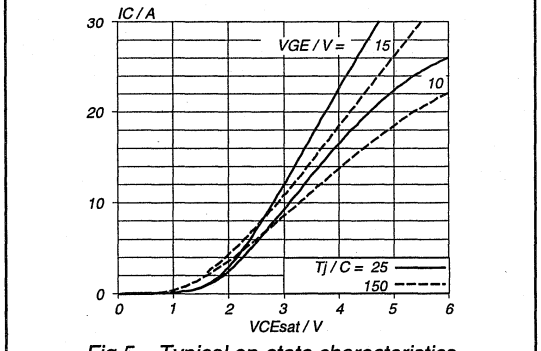


Fig.5. Typical on-state characteristics $I_C=f(V_{CE})$; parameters T_j, V_{GE}

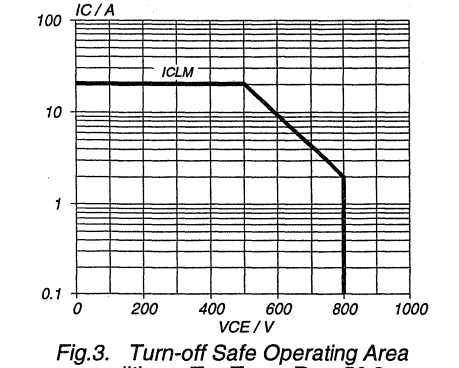


Fig.3. Turn-off Safe Operating Area conditions: $T_j \leq T_{jmax.}$; $R_G = 50\ \Omega$

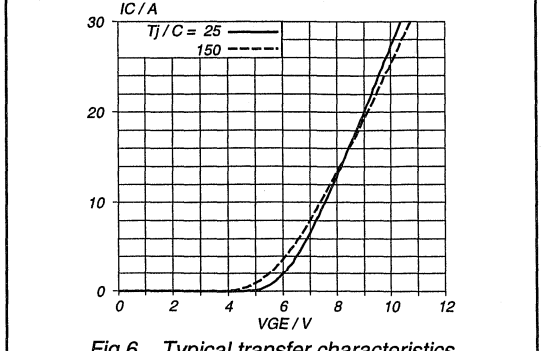


Fig.6. Typical transfer characteristics $I_C=f(V_{GE})$; conditions: V_{CE}=15 V; parameter T_j

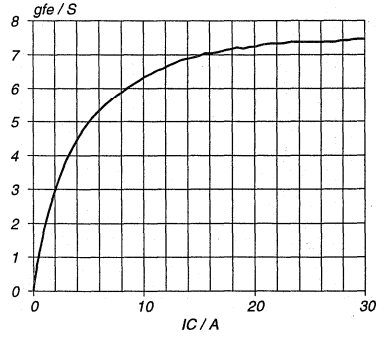


Fig.7. Typical transconductance, T_j = 25 °C. $g_{fe} = f(I_C)$; conditions: V_{CE} = 15 V

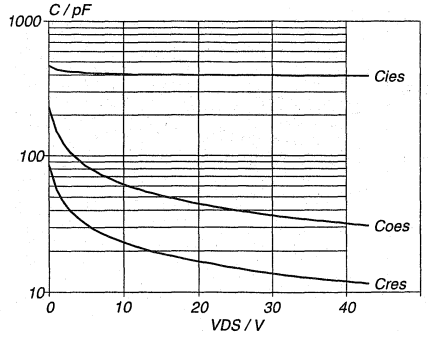


Fig.10. Typical capacitances, C_{ies}, C_{oes}, C_{res}. $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1MHz.

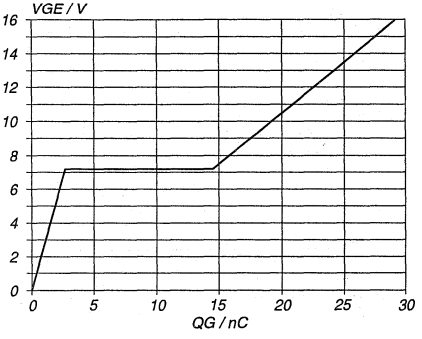


Fig.8. Typical turn-on gate-charge characteristics. $V_{GE} = f(Q_G)$; conditions: I_C = 6 A; V_{CE} = 500 V

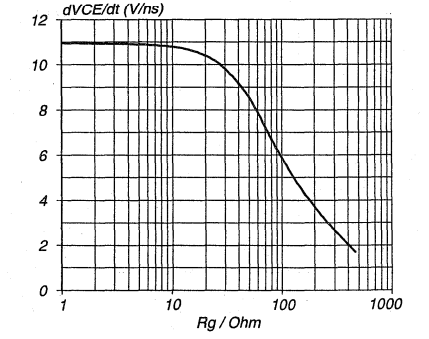


Fig.11. Typical turn-off dV_{CE}/dt vs. R_G conditions: I_C = 6 A; V_{CL} = 500 V; T_j = 125 °C

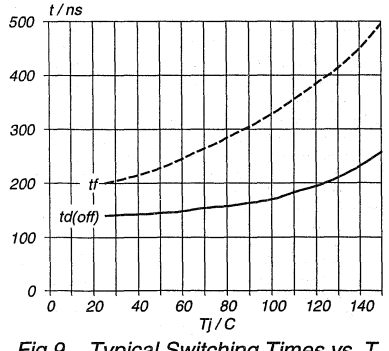


Fig.9. Typical Switching Times vs. T_j conditions: I_C = 6 A; V_{CL} = 500 V; R_G = 25 Ω

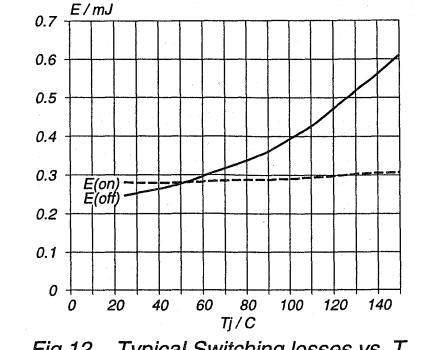


Fig.12. Typical Switching losses vs. T_j conditions: I_C = 6 A; V_{CL} = 500 V; R_G = 25 Ω

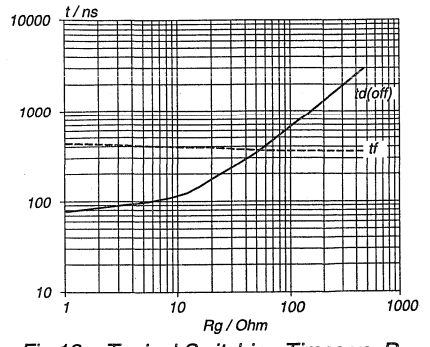


Fig.13. Typical Switching Times vs. R_G conditions: I_C = 6 A; V_{CL} = 500 V; T_j = 125 °C

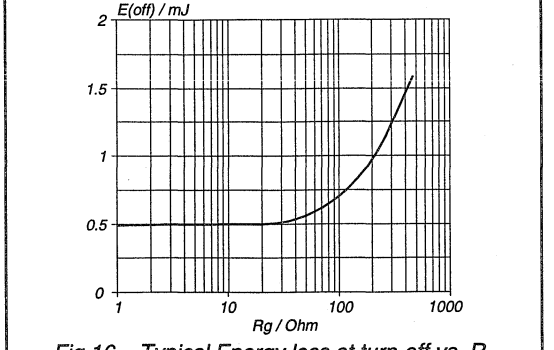


Fig.16. Typical Energy loss at turn-off vs. R_G conditions: I_C = 6 A; V_{CL} = 500 V; T_j = 125 °C

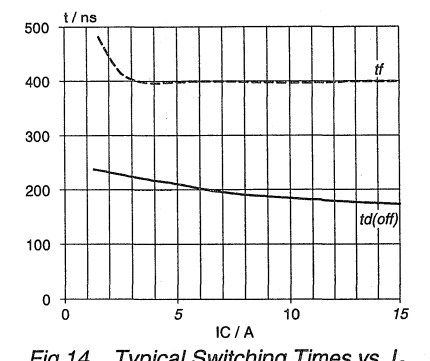


Fig.14. Typical Switching Times vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C

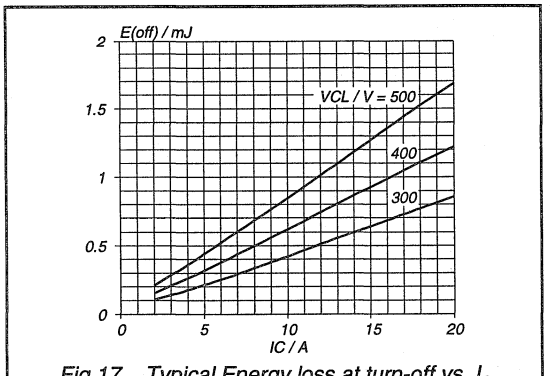


Fig.17. Typical Energy loss at turn-off vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C; parameter V_{CL}

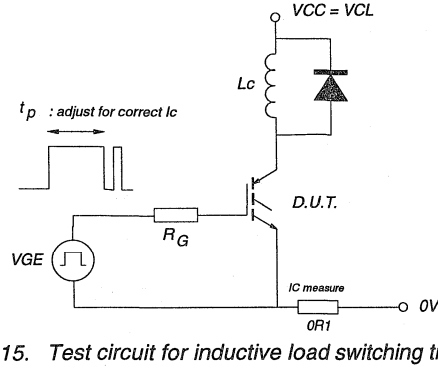


Fig.15. Test circuit for inductive load switching times.

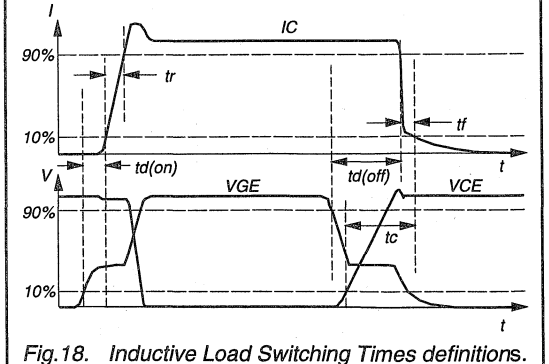


Fig.18. Inductive Load Switching Times definitions.

Insulated Gate Bipolar Transistor Protected Logic-Level IGBT

BUK856-400 IZ

GENERAL DESCRIPTION

Protected N-channel logic-level insulated gate bipolar power transistor in a plastic envelope, intended for automotive ignition applications. The device has built-in zener diodes providing active collector voltage clamping and ESD protection up to 2 kV.

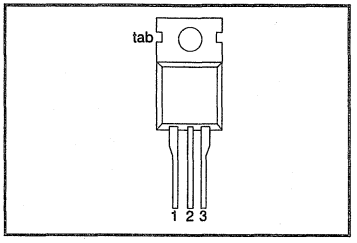
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage	350	400	500	V
V_{CEsat}	Collector-emitter on-state voltage			2.2	V
I_C	Collector current (DC)			20	A
P_{tot}	Total power dissipation			100	W
E_{CERS}	Clamped energy dissipation			300	mJ

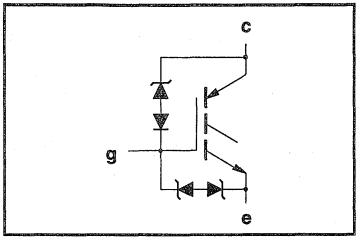
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collecter-emitter voltage	$t_p \leq 500\ \mu s$	-	500	V
V_{CE}	Collector-emitter voltage	Continuous	-20	50	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	12	V
I_C	Collector current (DC)	$T_{mb} = 100\ ^\circ C$	-	10	A
I_C	Collector current (DC)	$T_{mb} = 25\ ^\circ C$	-	20	A
I_{CM}	Collector current (pulsed peak value, on-state)	$T_{mb} = 25\ ^\circ C$; $t_p \leq 10$ ms; $V_{CE} \leq 15$ V	-	25	A
I_{CLM}	Collector current (clamped inductive load)	$1\ k\Omega \leq R_G \leq 10\ k\Omega$	-	10	A
E_{CERS}	Clamped turn-off energy (non-repetitive)	$T_{mb} = 25\ ^\circ C$; $I_C = 10$ A; $R_G = 1\ k\Omega$; see Figs. 23,24	-	300	mJ
E_{CERR} [1]	Clamped turn-off energy (repetitive)	$T_{mb} = 100\ ^\circ C$; $I_C = 8$ A; $R_G = 1\ k\Omega$; f = 50 Hz	-	125	mJ
E_{ECR} [1]	Reverse avalanche energy (repetitive)	$I_E = 1$ A; f = 50 Hz	-	5	mJ
P_{tot}	Total power dissipation	$T_{mb} = 25\ ^\circ C$	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Operating Junction Temperature	-	-40	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

1 This applies to short-term operation in ignition circuits with open-secondary ignition coil.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base		-	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CG}$	Collector-gate zener breakdown voltage	2 mA ≤ -I_G ≤ 5 mA; -40 ≤ T_j ≤150°C	350	400	500	V
$V_{(BR)EC}$	Reverse collector-emitter breakdown voltage	I_E = 10 mA	20	30	50	V
$\pm V_{(BR)GES}$	Gate-emitter breakdown voltage	I_G = ± 1 mA	12	16	20	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	1	1.5	2	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA; -40 ≤ T_j ≤150°C	0.6	-	2.4	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 50 V; V_{GE} = 0 V; T_j = 25 °C	-	0.01	10	µA
I_{CES}	Zero gate voltage collector current	T_j = 125 °C	-	0.01	1	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V	-	0.2	5	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V; T_j = 125°C	-	2	20	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±6 V	-	0.1	1	µA
		T_j = 150°C	-	5	100	µA
V_{CEsat}	Collector-emitter on-state voltage	V_{GE} = 4.5 V; I_C = 8 A	-	1.2	2.2	V
		V_{GE} = 3.5 V; I_C = 6 A; -40 ≤ T_j ≤150°C	-	1.2	2.2	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage (peak value)	R_G = 1 kΩ; I_C = 10 A; -40 ≤ T_j ≤150°C; Inductive load; see Figs. 23,24	350	400	500	V
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 4 A	5.5	15	20	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	940	1200	pF
C_{oes}	Output capacitance		-	95	130	pF
C_{res}	Feedback capacitance		-	30	50	pF
$t_{d\ off}$	Turn-off delay time	I_C = 8 A; V_{CL} = 300 V; R_G = 1 kΩ;	-	13	18	µs
t_f	Fall time	V_{GE} = 5 V; T_j = 125°C;	-	6	10	µs
t_c	Crossover Time	Inductive load; see Figs. 20,21	-	12	-	µs
E_{off}	Turn-off Energy loss		-	13	-	mJ

Insulated Gate Bipolar Transistor Protected Logic-Level IGBT

BUK856-400 IZ

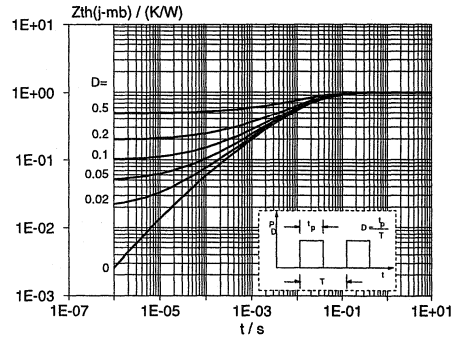


Fig.1. Transient thermal impedance
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

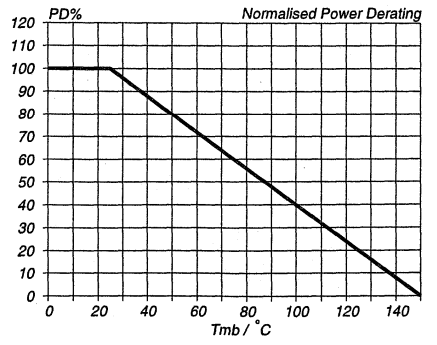


Fig.4. Normalised power dissipation.
$PD\% = 100.P_D/P_{D\ 25°C} = f(T_{mb})$

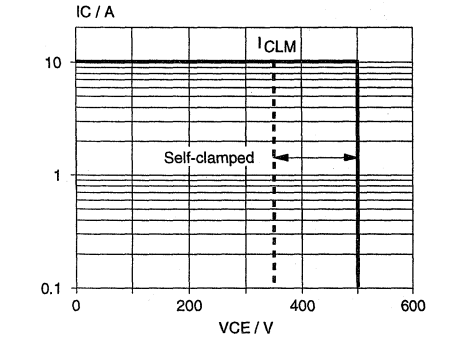


Fig.2. Turn-off Safe Operating Area
conditions: $T_j \leq T_{jmax.}$; $R_G \geq 1\ k\Omega$

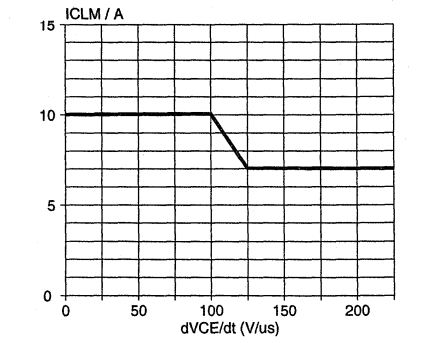


Fig.5. Derating of I_{CLM} with turn-off dV_{CE}/dt
conditions: $V_{CE} \leq 500\ V$; $T_j \leq T_{jmax.}$

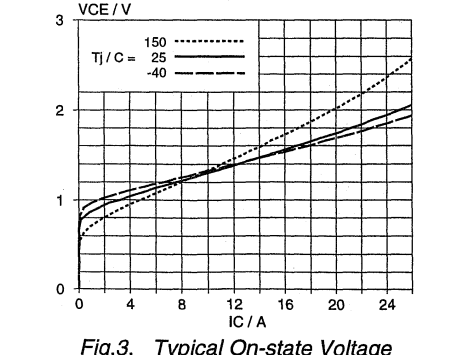


Fig.3. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; parameter T_j; conditions: $V_{GE} = 3.5\ V$

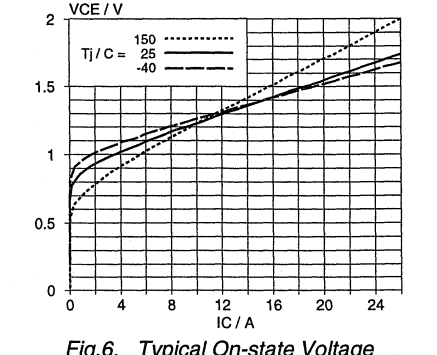


Fig.6. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; parameter T_j; conditions: $V_{GE} = 5\ V$

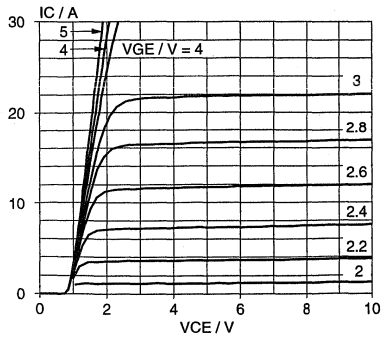


Fig.7. Typical Output Characteristics
$I_C = f(V_{CE})$; parameter V_{GE}; conditions: $T_j = 25°C$

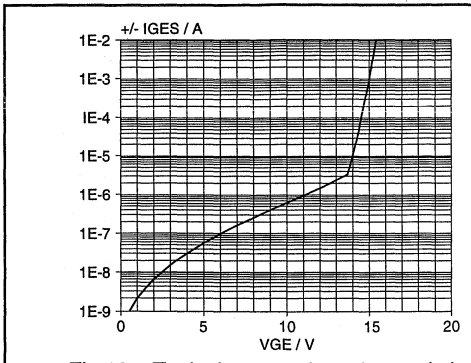


Fig.10. Typical gate-emitter charcteristics
$I_{GES} = f(V_{GE})$; conditions: $V_{CE} = 0$ V; $T_j = 25°C$

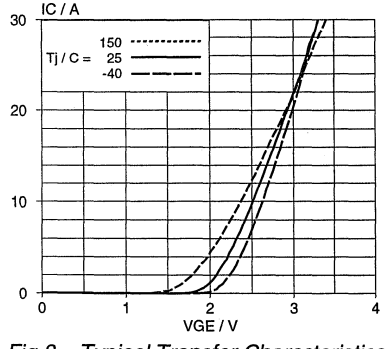


Fig.8. Typical Transfer Characteristics
$I_C = f(V_{GE})$, parameter T_j; conditions: $V_{CE} = 10$ V

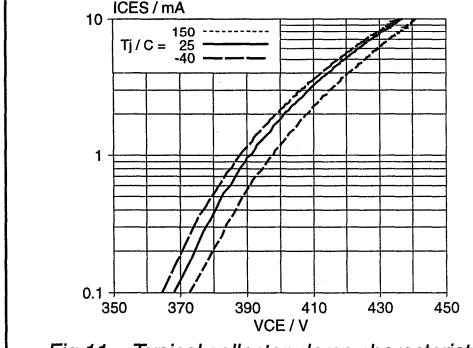


Fig.11. Typical collector clamp characteristics
$I_{CES} = f(V_{CE})$; parameter T_j; conditions: $V_{GE} = 0$ V

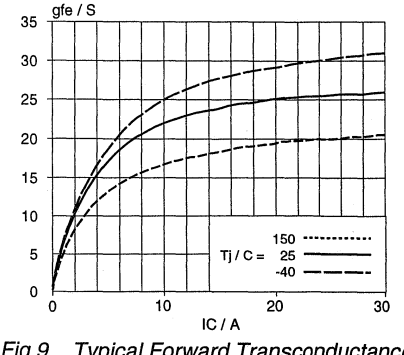


Fig.9. Typical Forward Transconductance
$g_{fe} = f(I_C)$; parameter T_j; conditions: $V_{CE} = 10$ V

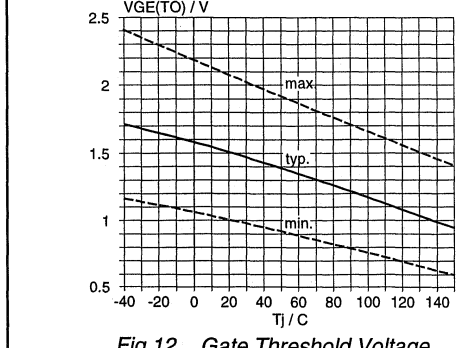


Fig.12. Gate Threshold Voltage
$V_{GE(TO)} = f(T_j)$; conditions: $I_C = 1$ mA; $V_{CE} = V_{GE}$

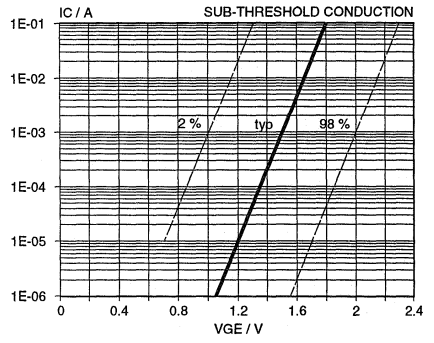


Fig.13. Sub-threshold collector current $I_C = f(V_{GE})$; $T_j = 25°C$; $V_{CE} = V_{GE}$

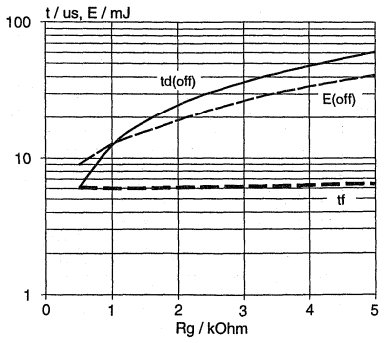


Fig.16. Typical Switching Characteristics vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

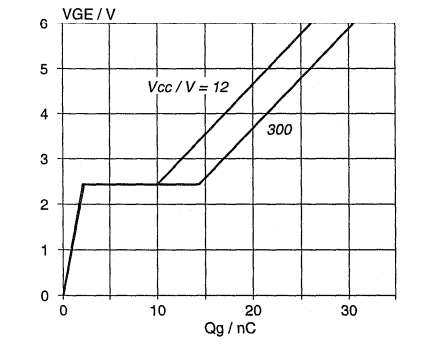


Fig.14. Typical Turn-on Gate Charge Characteristics $V_{GE} = f(Q_G)$; conditions: I_C = 8 A.

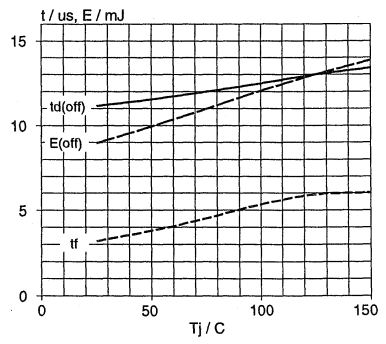


Fig.17. Typical Switching Characteristics vs. T_j conditions: I_C=8 A; V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

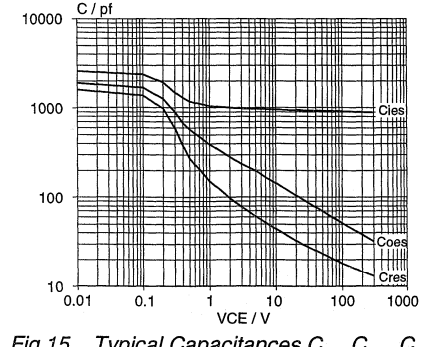


Fig.15. Typical Capacitances C_{ies}, C_{oes}, C_{res} $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1 MHz

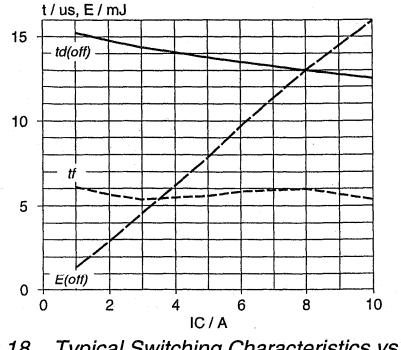


Fig.18. Typical Switching Characteristics vs. I_C conditions: T_j=125 °C V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

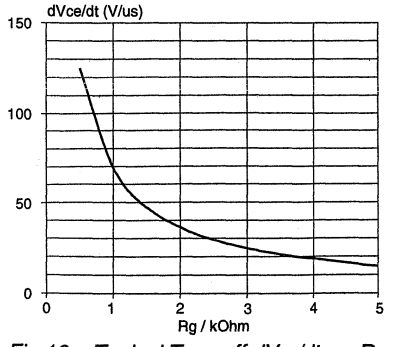


Fig.19. Typical Turn-off dV_{CE}/dt vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

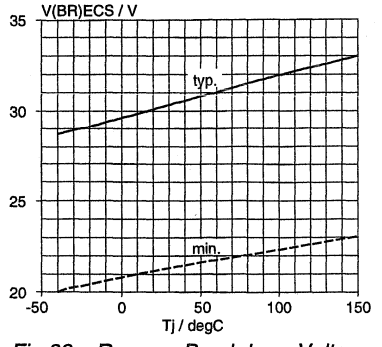


Fig.22. Reverse Breakdown Voltage $V_{(BR)ECS} = f(T_j)$; conditions: I_{EC} = 50 mA

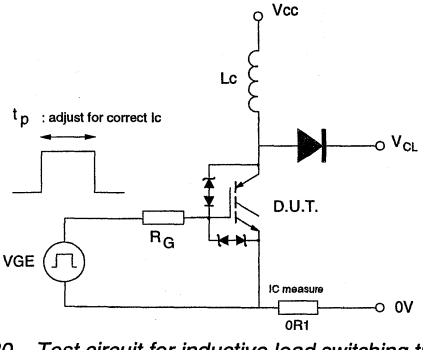


Fig.20. Test circuit for inductive load switching times.

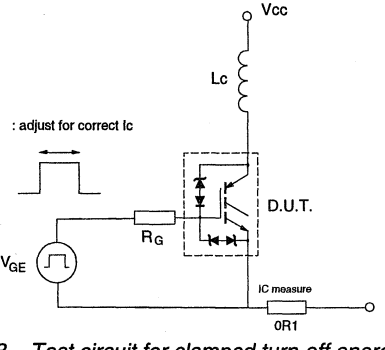


Fig.23. Test circuit for clamped turn-off energy test

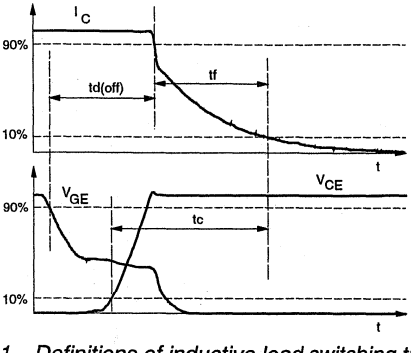


Fig.21. Definitions of inductive load switching times.

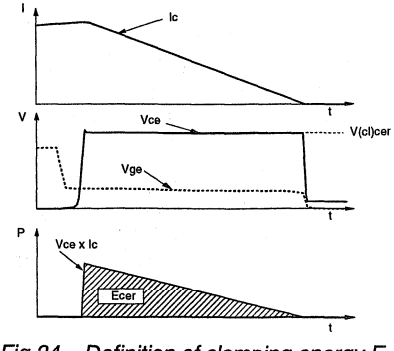


Fig.24. Definition of clamping energy E_{CER}

Insulated Gate Bipolar Transistor (IGBT) — BUK856-800A

GENERAL DESCRIPTION

Fast-switching N-channel insulated gate bipolar power transistor in a plastic envelope.
The device is intended for use in motor control, DC/DC and AC/DC converters, and in general purpose high frequency switching applications.

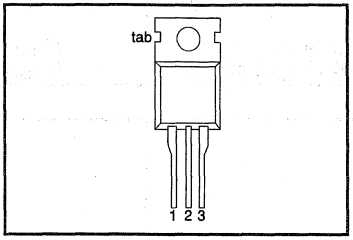
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CE}	Collector-emitter voltage	800	V
I_C	Collector current (DC)	24	A
P_{tot}	Total power dissipation	125	W
V_{CEsat}	Collector-emitter on-state voltage	3.5	V
E_{off}	Turn-off energy Loss	1.0	mJ

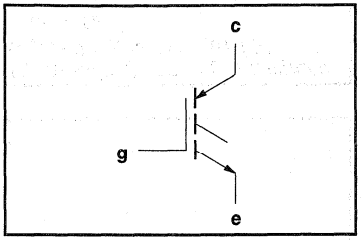
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collector-emitter voltage	-	-5	800	V
V_{CGR}	Collector-gate voltage	R_{GE} = 20 kΩ	-	800	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	30	V
I_C	Collector current (DC)	T_{mb} = 25 °C	-	24	A
I_C	Collector current (DC)	T_{mb} = 100 °C	-	12	A
I_{CLM}	Collector Current (Clamped Inductive Load)	$T_j \leq T_{jmax.}$ $V_{CL} \leq 500$ V	-	40	A
I_{CM}	Collector current (pulsed peak value, on-state)	$T_j \leq T_{jmax.}$	-	50	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Junction to mounting base	-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	In free air	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V; I_C = 0.25 mA	800	-	-	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	3	4	5.5	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j = 25 °C	-	10	200	µA
I_{CES}	Zero gate voltage collector current	V_{CE} = 800 V; V_{GE} = 0 V; T_j =125 °C	-	0.2	1	mA
I_{ECS}	Reverse collector current	V_{CE} = -5 V; V_{GE} = 0 V	-	0.1	5	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±30 V; V_{CE} = 0 V	-	10	100	nA
V_{CEsat}	Collector-emitter saturation voltage	V_{GE} = 15 V; I_C = 12 A	-	2.4	3.5	V
		V_{GE} = 15 V; I_C = 24 A	-	3.1	-	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 6 A	3	7	-	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	900	1250	pF
C_{oes}	Output capacitance		-	85	120	pF
C_{res}	Feedback capacitance		-	30	50	pF
$t_{d\,on}$	Turn-on delay time	I_C = 12 A; V_{CC} = 500 V;	-	25	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	45	-	ns
E_{on}	Turn-on Energy Loss	T_j = 25°C;	-	0.6	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	230	350	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	200	400	ns
E_{off}	Turn-off Energy Loss	losses	-	0.5	1	mJ
$t_{d\,on}$	Turn-on delay time	I_C = 12 A; V_{CC} = 500 V;	-	25	-	ns
t_r	Turn-on rise time	V_{GE} = 15 V; R_G = 25Ω;	-	45	-	ns
E_{on}	Turn-on Energy Loss	T_j = 125°C;	-	0.6	-	mJ
$t_{d\,off}$	Turn-off delay time	Inductive Load	-	300	450	ns
t_f	Turn-off fall time	Energy Losses include all 'tail'	-	400	800	ns
E_{off}	Turn-off Energy Loss	losses	-	1	2	mJ

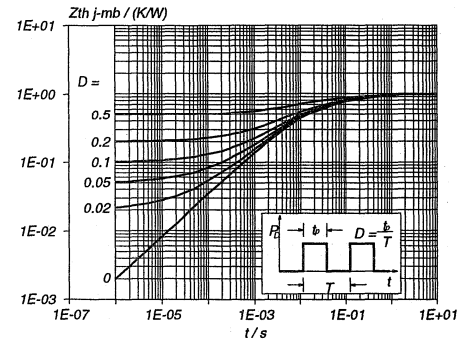


Fig.1. Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

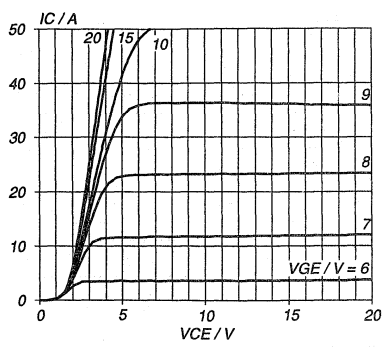


Fig.4. Typical output characteristics, T_j=25 ˚C. $I_C=f(V_{CE})$; parameter V_{GE}

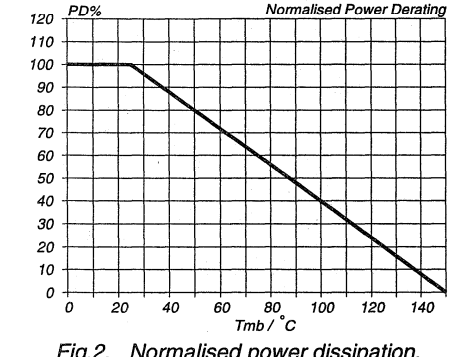


Fig.2. Normalised power dissipation. $PD\% = 100.P_D/P_{D\ 25^\circ C} = f(T_{mb})$

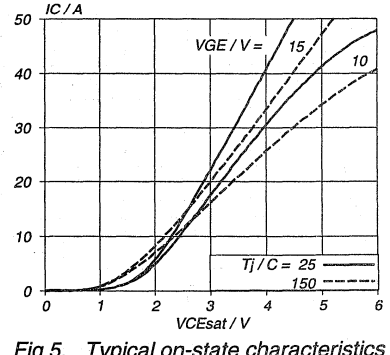


Fig.5. Typical on-state characteristics $I_C=f(V_{CE})$; parameters T_j V_{GE}

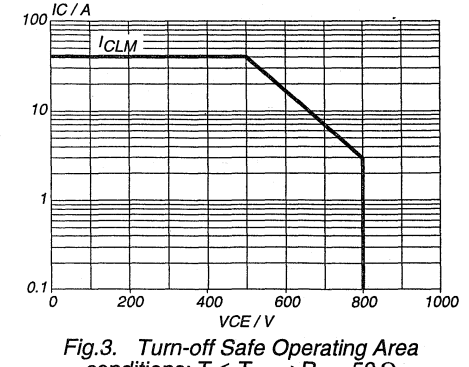


Fig.3. Turn-off Safe Operating Area conditions: $T_j \leq T_{jmax.}$; $R_G = 50\ \Omega$

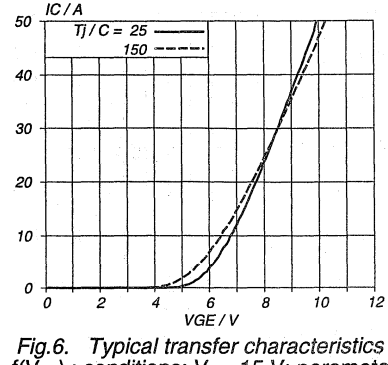


Fig.6. Typical transfer characteristics $I_C=f(V_{GE})$; conditions: V_{CE}=15 V; parameter T_j

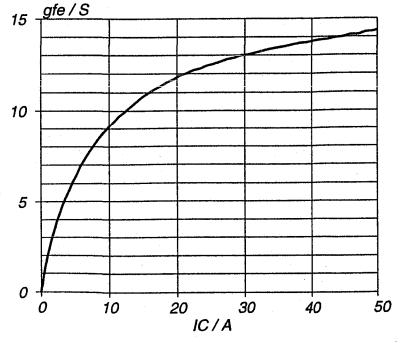


Fig.7. Typical transconductance, T_j = 25 °C. $g_{fe} = f(I_C)$; conditions: V_{CE} = 15 V

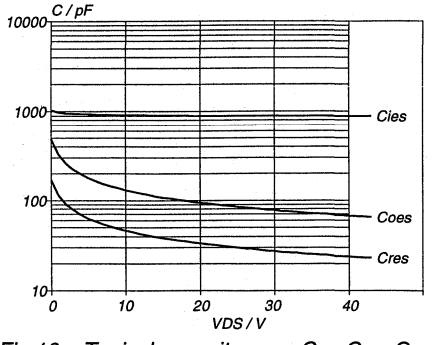


Fig.10. Typical capacitances, C_{ies}, C_{oes}, C_{res}. $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1MHz.

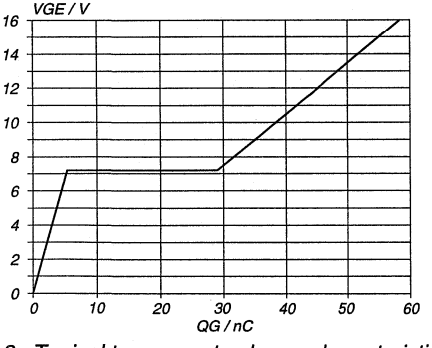


Fig.8. Typical turn-on gate-charge characteristics. $V_{GE} = f(Q_G)$; conditions: I_C = 12 A; parameter V_{CE}

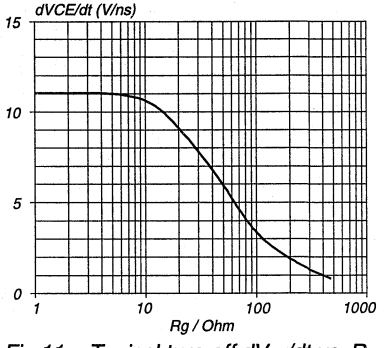


Fig.11. Typical turn-off dV_{CE}/dt vs. R_G conditions: I_C = 12 A; V_{CL} = 500 V; T_j = 125 °C

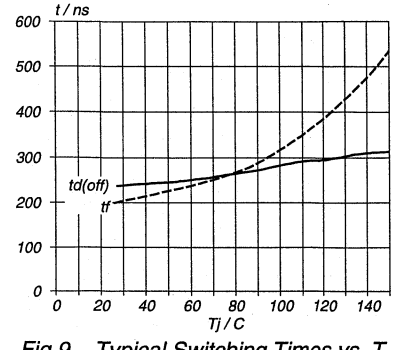


Fig.9. Typical Switching Times vs. T_j conditions: I_C = 12 A; V_{CL} = 500 V; R_G = 25 Ω

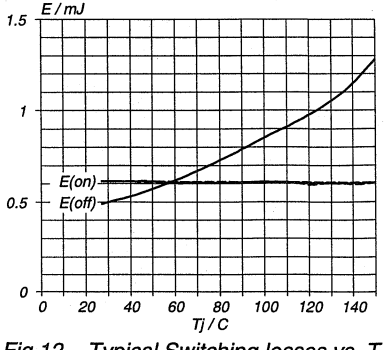


Fig.12. Typical Switching losses vs. T_j conditions: I_C = 12 A; V_{CL} = 500 V; R_G = 25 Ω

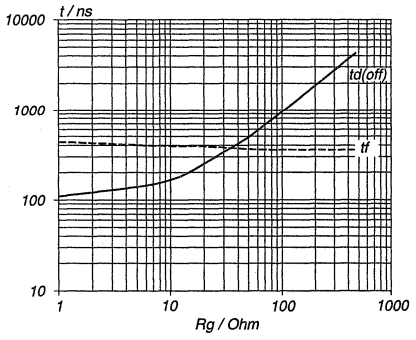


Fig.13. Typical Switching Times vs. R_G conditions: I_C = 12 A; V_{CL} = 500 V; T_j = 125 °C

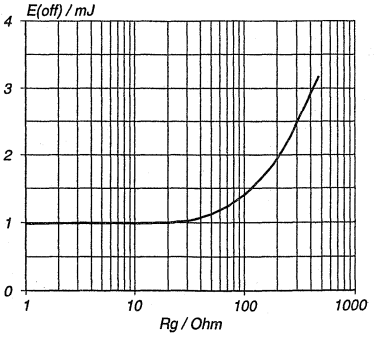


Fig.16. Typical Energy loss at turn-off vs. R_G conditions: I_C = 12 A; V_{CL} = 500 V; T_j = 125 °C

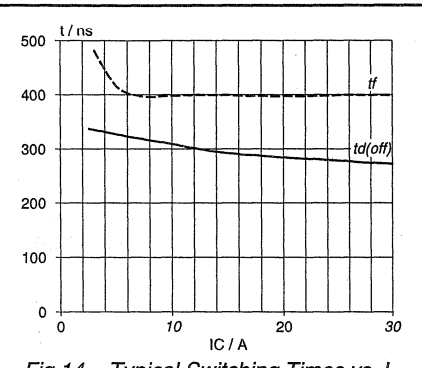


Fig.14. Typical Switching Times vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C

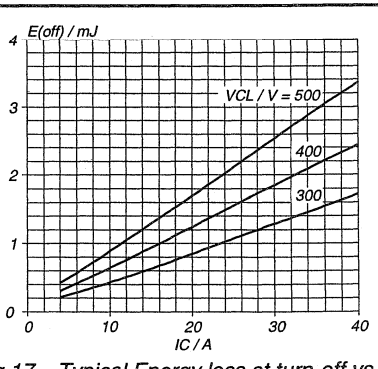


Fig.17. Typical Energy loss at turn-off vs. I_C conditions: V_{CL} = 500 V; R_G = 25 Ω; T_j = 125°C; parameter V_{CL}

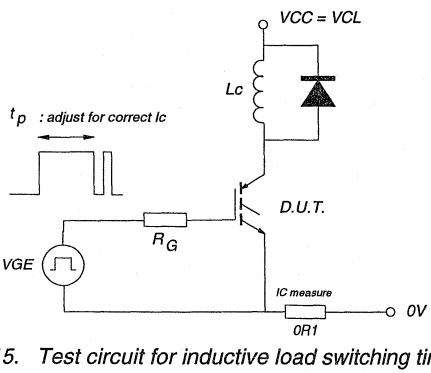


Fig.15. Test circuit for inductive load switching times.

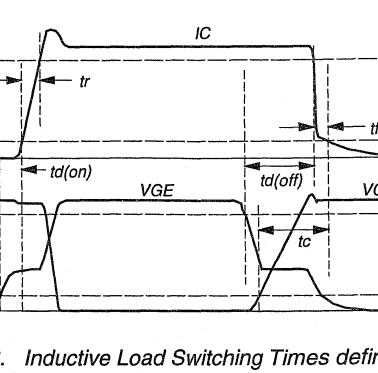


Fig.18. Inductive Load Switching Times definitions.

Insulated Gate Bipolar Transistor
Protected Logic-Level IGBT

BUK866-400 IZ

GENERAL DESCRIPTION

Protected N-channel logic-level insulated gate bipolar power transistor in a plastic envelope suitable for surface mount applications. It is intended for automotive ignition applications, and has integral zener diodes providing active collector voltage clamping and ESD protection up to 2 kV.

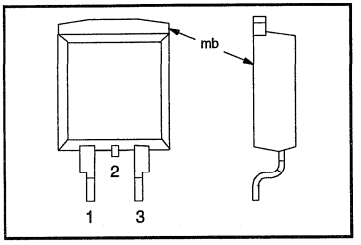
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage	350	400	500	V
V_{CEsat}	Collector-emitter on-state voltage			2.2	V
I_C	Collector current (DC)			20	A
P_{tot}	Total power dissipation			100	W
E_{CERS}	Clamped energy dissipation			300	mJ

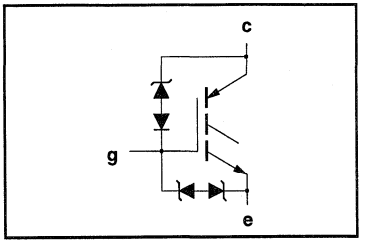
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	collector
3	emitter
tab	collector

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CE}	Collecter-emitter voltage	$t_p \leq 500$ µs	-	500	V
V_{CE}	Collector-emitter voltage	Continuous	-20	50	V
$\pm V_{GE}$	Gate-emitter voltage	-	-	12	V
I_C	Collector current (DC)	T_{mb} = 100 °C	-	10	A
I_C	Collector current (DC)	T_{mb} = 25 °C	-	20	A
I_{CM}	Collector current (pulsed peak value, on-state)	T_{mb} = 25 °C; $t_p \leq 10$ ms; $V_{CE} \leq 15$ V	-	25	A
I_{CLM}	Collector current (clamped inductive load)	1 kΩ ≤ R_G ≤ 10 kΩ	-	10	A
E_{CERS}	Clamped turn-off energy (non-repetitive)	T_{mb} = 25 °C; I_C = 10 A; R_G = 1 kΩ; see Figs. 23,24	-	300	mJ
E_{CERR}	Clamped turn-off energy (repetitive)	T_{mb} = 125 °C; I_C = 8 A; R_G = 1 kΩ; f = 50 Hz; t = 60 min.	-	125	mJ
E_{ECR}	Reverse avalanche energy (repetitive)	I_E = 1 A; f = 50 Hz	-	5	mJ
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Operating Junction Temperature	-	-40	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 26).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CG}$	Collector-gate zener breakdown voltage	2 mA ≤ $-I_G$ ≤ 5 mA; -40 ≤ T_j ≤150°C	350	400	500	V
$V_{(BR)EC}$	Reverse collector-emitter breakdown voltage	I_E = 10 mA	20	30	50	V
$\pm V_{(BR)GES}$	Gate-emitter breakdown voltage	I_G = ± 1 mA	12	16	20	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA	1	1.5	2	V
$V_{GE(TO)}$	Gate threshold voltage	V_{CE} = V_{GE}; I_C = 1 mA; -40 ≤ T_j ≤150°C	0.6	-	2.4	V
I_{CES}	Zero gate voltage collector current	V_{CE} = 50 V; V_{GE} = 0 V; T_j = 25 °C	-	0.01	10	µA
I_{CES}	Zero gate voltage collector current	T_j = 125 °C	-	0.01	1	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V	-	0.2	5	mA
I_{EC}	Reverse collector current	V_{CE} = -20 V; T_j = 125°C	-	2	20	mA
I_{GES}	Gate emitter leakage current	V_{GE} = ±6 V	-	0.1	1	µA
		T_j = 150°C	-	5	100	µA
V_{CEsat}	Collector-emitter on-state voltage	V_{GE} = 4.5 V; I_C = 8 A	-	1.2	2.2	V
		V_{GE} = 3.5 V; I_C = 6 A; -40 ≤ T_j ≤150°C	-	1.2	2.2	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)CER}$	Collector-emitter clamp voltage (peak value)	R_G = 1 kΩ; I_C = 10 A; -40 ≤ T_j ≤150°C; Inductive load; see Figs. 23,24	350	400	500	V
g_{fe}	Forward transconductance	V_{CE} = 15 V; I_C = 4 A	5.5	15	20	S
C_{ies}	Input capacitance	V_{GE} = 0 V; V_{CE} = 25 V; f = 1 MHz	-	940	1200	pF
C_{oes}	Output capacitance		-	95	130	pF
C_{res}	Feedback capacitance		-	30	50	pF
$t_{d\ off}$	Turn-off delay time	I_C = 8 A; V_{CL} = 300 V; R_G = 1 kΩ;	-	13	18	µs
t_f	Fall time	V_{GE} = 5 V; T_j = 125°C;	-	6	10	µs
t_c	Crossover Time	Inductive load; see Figs. 20,21	-	12	-	µs
E_{off}	Turn-off Energy loss		-	13	-	mJ

Insulated Gate Bipolar Transistor
Protected Logic-Level IGBT

BUK866-400 IZ

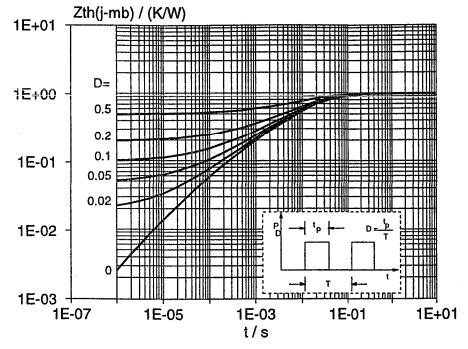


Fig.1. Transient thermal impedance
$Z_{th\ j\text{-}mb} = f(t)$; *parameter* $D = t_p/T$

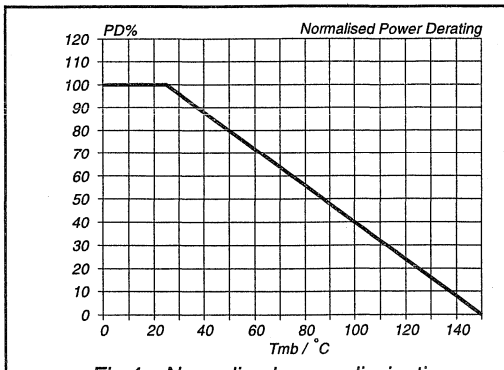


Fig.4. Normalised power dissipation.
$PD\% = 100.P_D/P_{D\ 25°C} = f(T_{mb})$

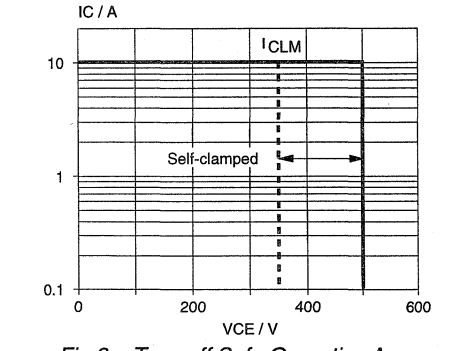


Fig.2. Turn-off Safe Operating Area
conditions: $T_j \leq T_{jmax.}$; $R_G \geq 1\ k\Omega$

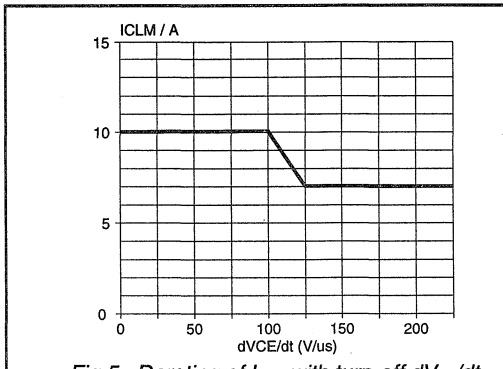


Fig.5. Derating of I_{CLM} *with turn-off* dV_{CE}/dt
conditions: $V_{CE} \leq 500\ V$; $T_j \leq T_{jmax.}$

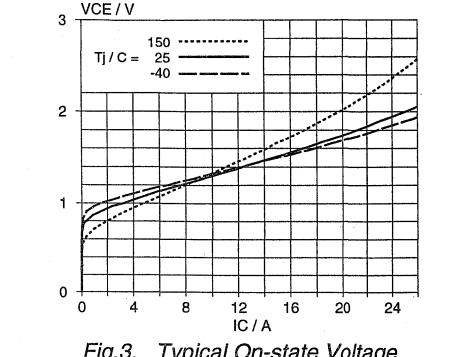


Fig.3. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 3.5\ V$

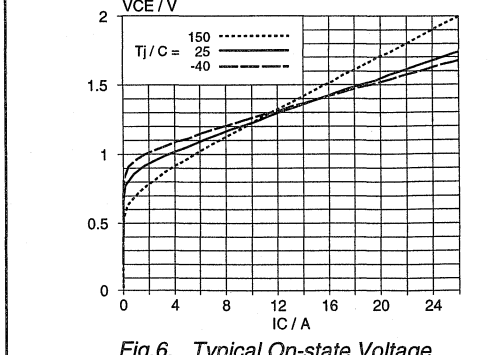


Fig.6. Typical On-state Voltage
$V_{CEsat} = f(I_C)$; *parameter* T_j; *conditions:* $V_{GE} = 5\ V$

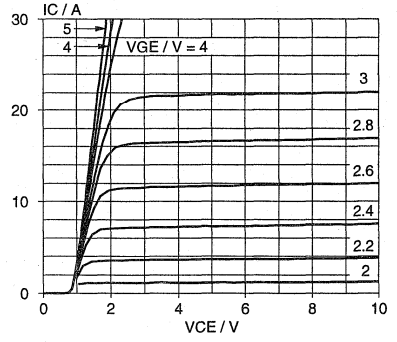


Fig.7. Typical Output Characteristics
$I_C = f(V_{CE})$; parameter V_{GE}; conditions: $T_j = 25°C$

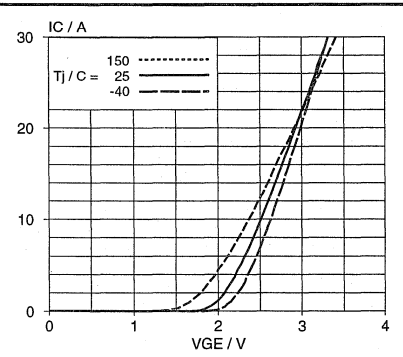


Fig.8. Typical Transfer Characteristics
$I_C = f(V_{GE})$, parameter T_j; conditions: $V_{CE} = 10$ V

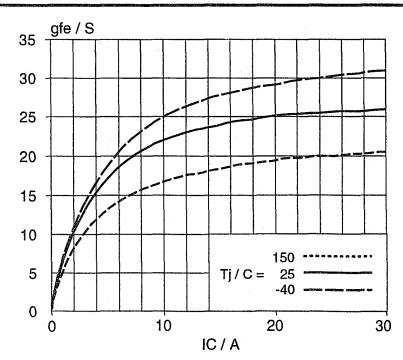


Fig.9. Typical Forward Transconductance
$g_{fe} = f(I_C)$; parameter T_j; conditions: $V_{CE} = 10$ V

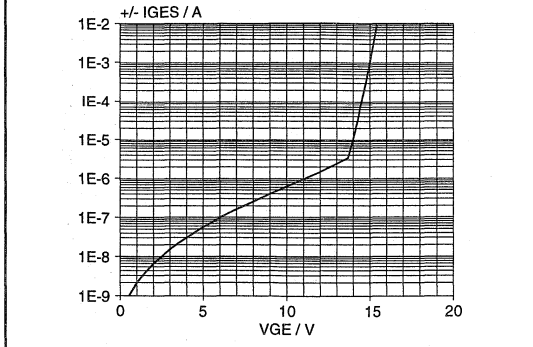


Fig.10. Typical gate-emitter charcteristics
$I_{GES} = f(V_{GE})$; conditions: $V_{CE} = 0$ V; $T_j = 25°C$

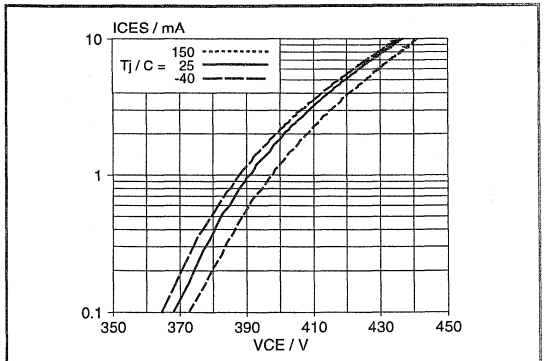


Fig.11. Typical collector clamp characteristics
$I_{CES} = f(V_{CE})$; parameter T_j; conditions: $V_{GE} = 0$ V

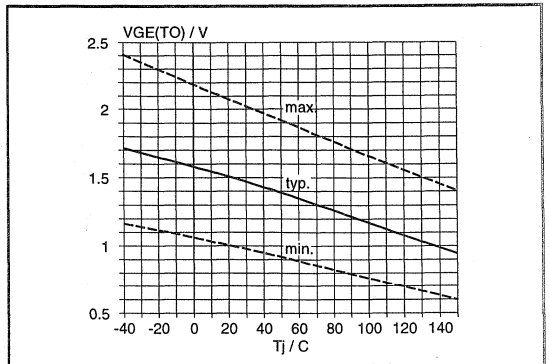


Fig.12. Gate Threshold Voltage
$V_{GE(TO)} = f(T_j)$; conditions: $I_C = 1$ mA; $V_{CE} = V_{GE}$

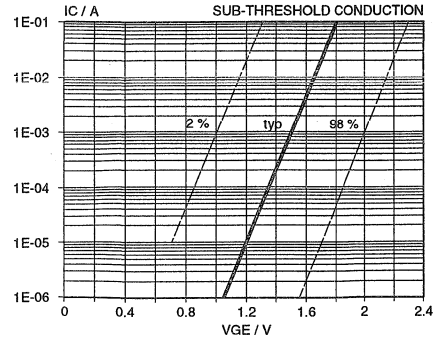


Fig.13. Sub-threshold collector current $I_C = f(V_{GE})$; $T_j = 25°C$; $V_{CE} = V_{GE}$

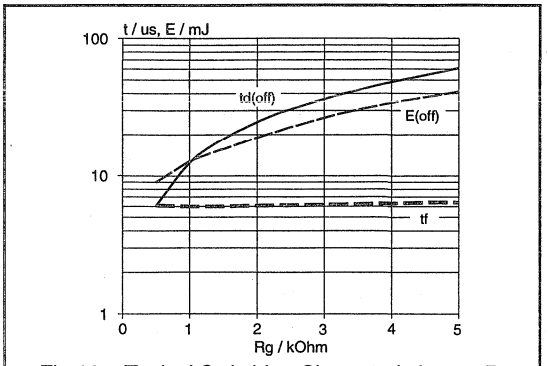


Fig.16. Typical Switching Characteristics vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

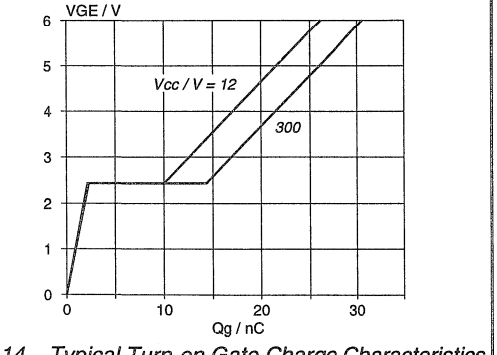


Fig.14. Typical Turn-on Gate Charge Characteristics $V_{GE} = f(Q_G)$; conditions: I_C = 8 A.

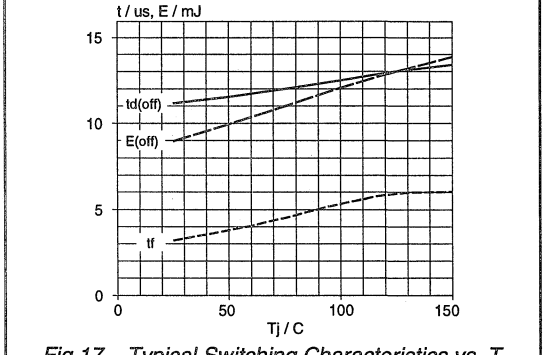


Fig.17. Typical Switching Characteristics vs. T_j conditions: I_C=8 A; V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

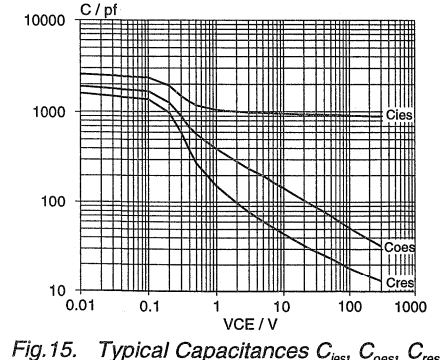


Fig.15. Typical Capacitances C_{ies}, C_{oes}, C_{res} $C = f(V_{CE})$; conditions: V_{GE} = 0 V; f = 1 MHz

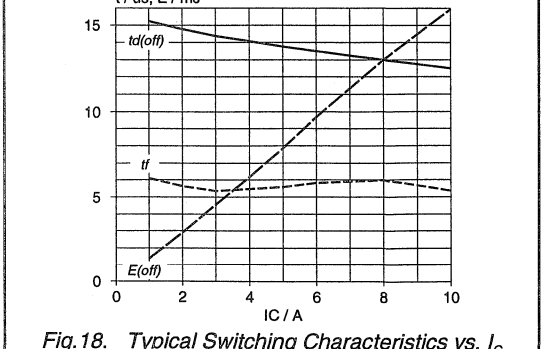


Fig.18. Typical Switching Characteristics vs. I_C conditions: T_j=125 °C V_{CL}=300 V; R_G=1 kΩ; L_C=5 mH.

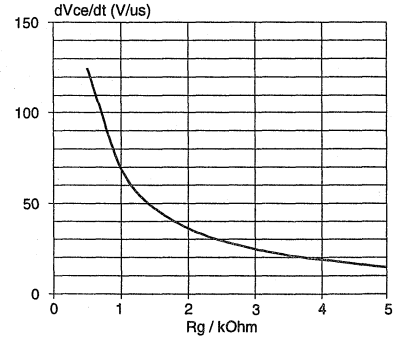


Fig.19. Typical Turn-off dV_{CE}/dt vs. R_G conditions: T_j=125 °C; I_C=8 A; V_{CL}=300 V; L_C=5 mH.

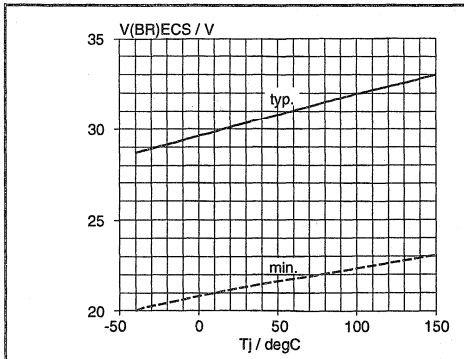


Fig.22. Reverse Breakdown Voltage $V_{(BR)ECS} = f(T_j)$; conditions: I_{EC} = 50 mA

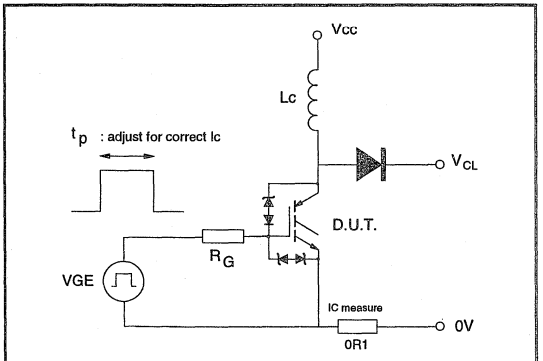


Fig.20. Test circuit for inductive load switching times.

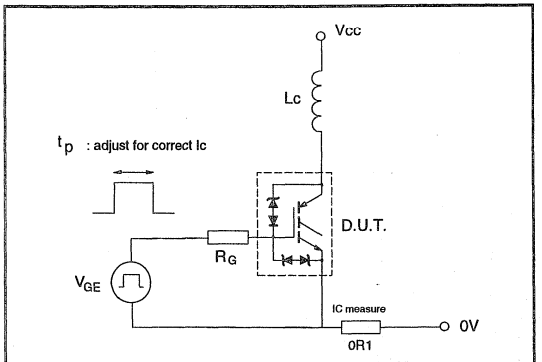


Fig.23. Test circuit for clamped turn-off energy test

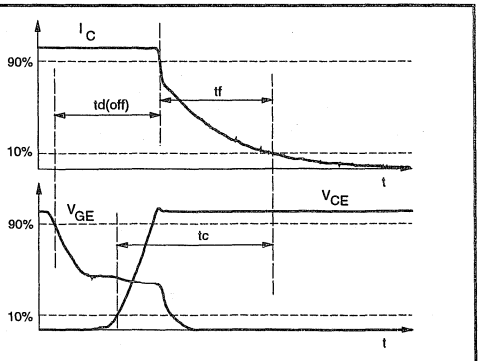


Fig.21. Definitions of inductive load switching times.

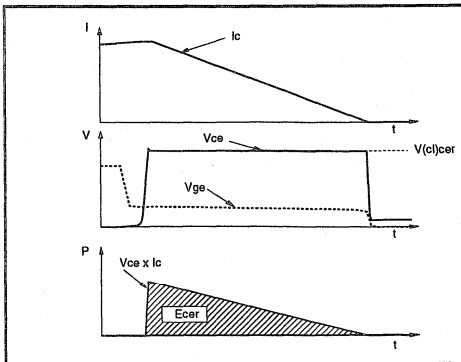


Fig.24. Definition of clamping energy E_{CER}

TrenchMOS™ transistor
Standard level FET

BUK7508-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

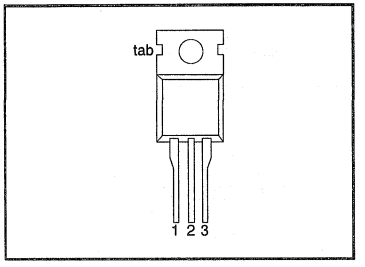
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	8	mΩ

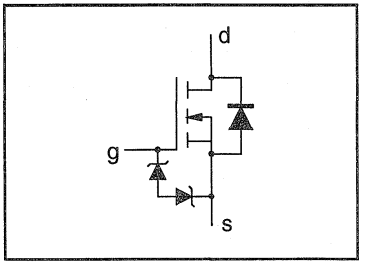
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	65	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	6.5	8	mΩ
		T_j = 175˚C	-	-	17	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	10	45	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	3600	4500	pF
C_{oss}	Output capacitance		-	830	1000	pF
C_{rss}	Feedback capacitance		-	320	440	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	27	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	70	105	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	100	140	ns
t_f	Turn-off fall time		-	50	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

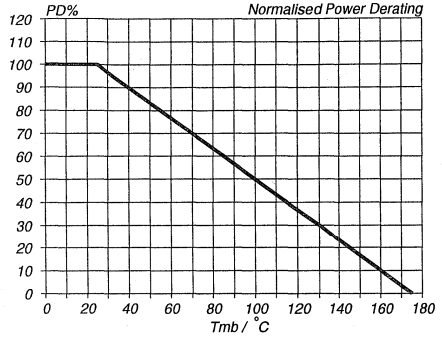


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

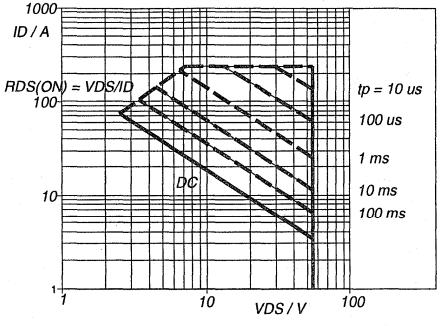


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

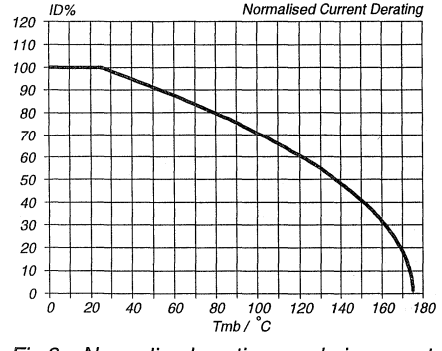


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

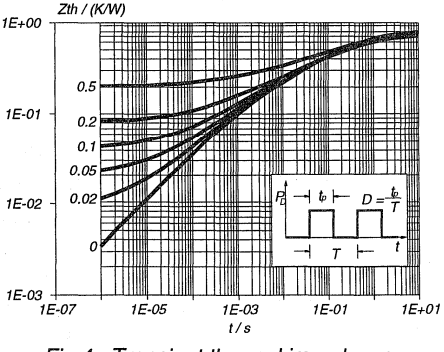


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

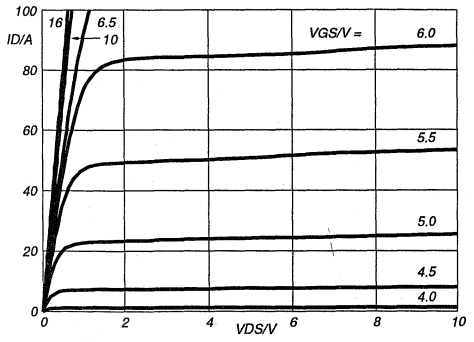


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

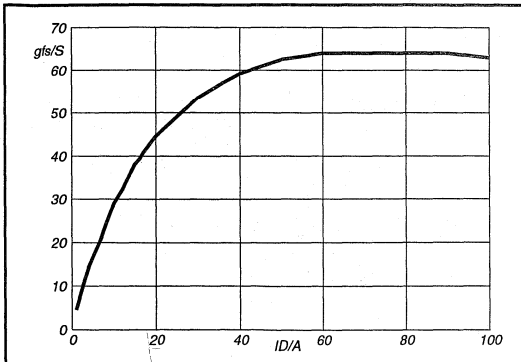


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

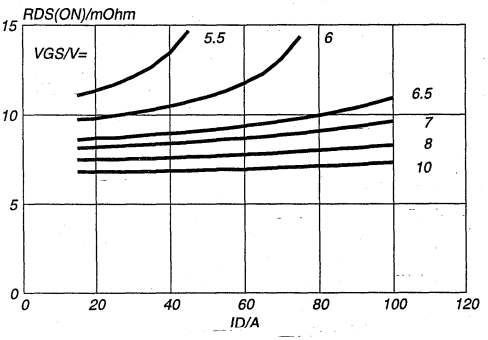


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

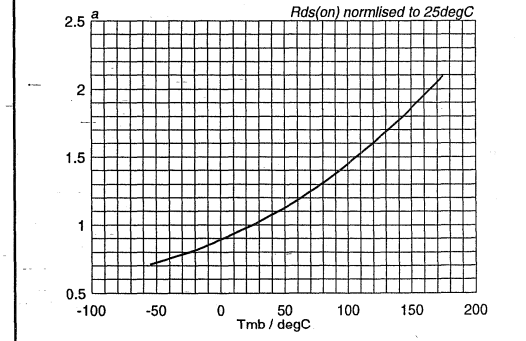


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

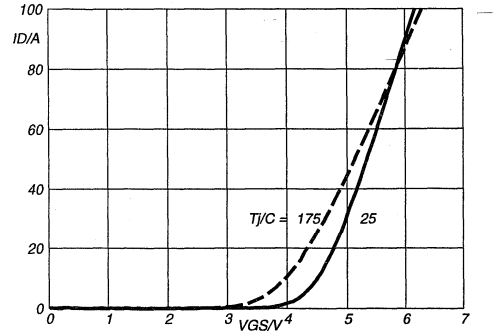


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

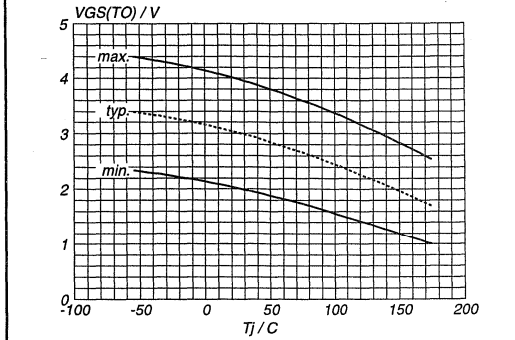


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

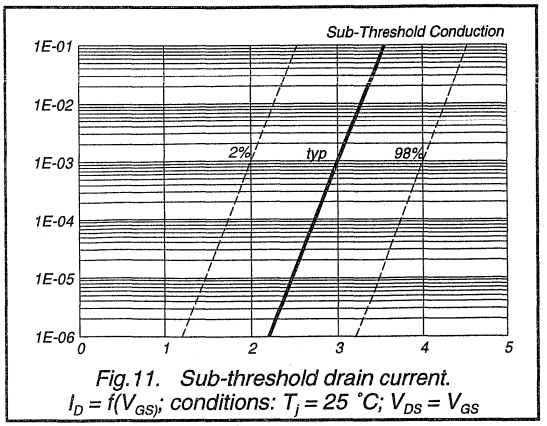


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

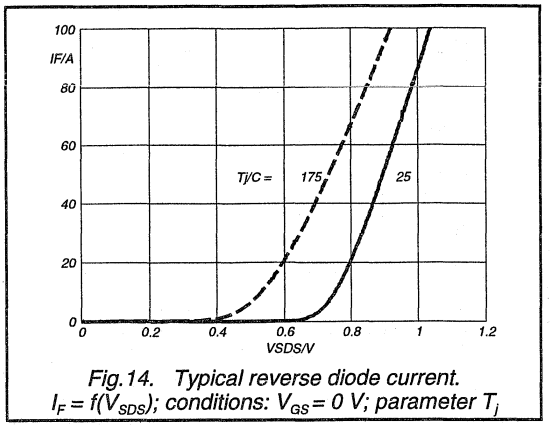


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

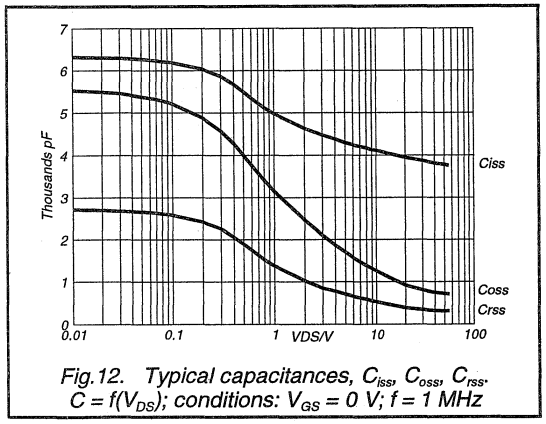


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

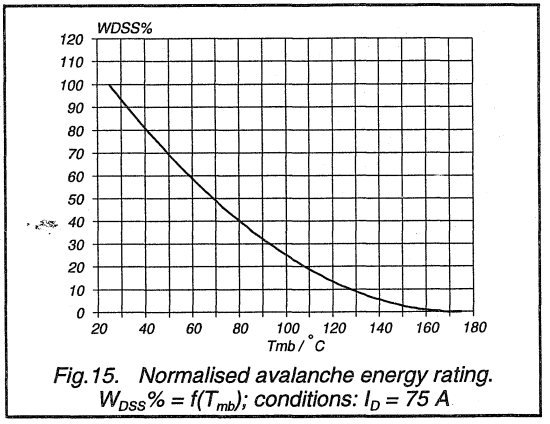


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

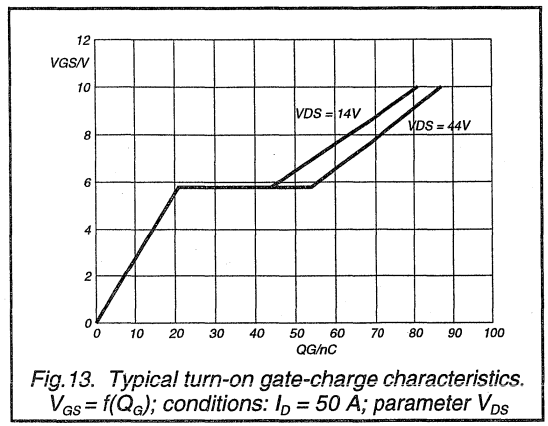


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

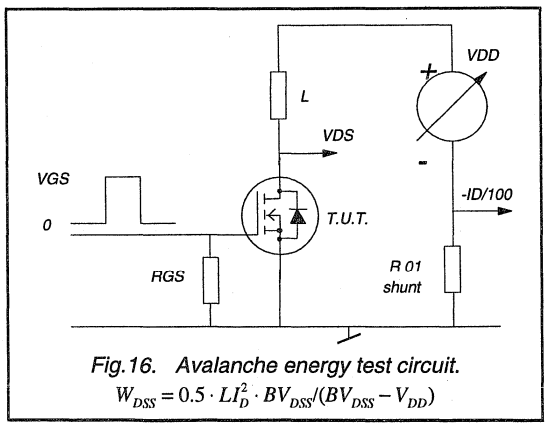


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

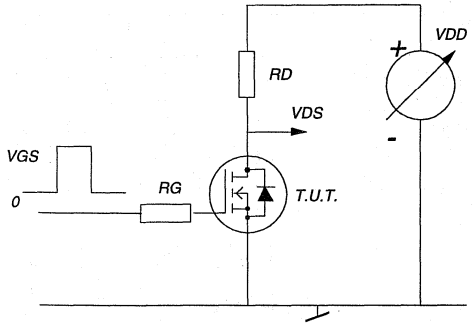


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7514-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

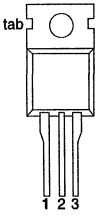
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	68	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	14	mΩ

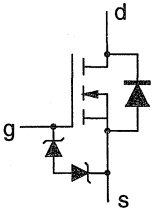
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	68	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3.0	4.0	V
		T_j = 175˚C	1	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	8	39	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2200	2900	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	200	270	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	18	26	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	35	85	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	45	60	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	68	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 65 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 65 A; -dI_F/dt = 100 A/µs;	-	57	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 65 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

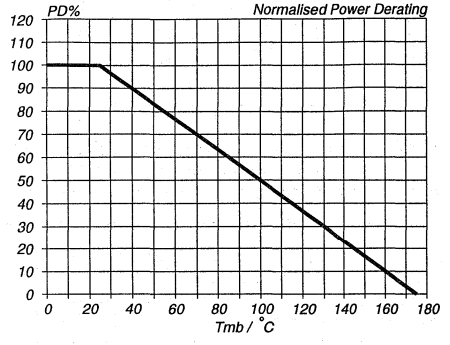


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

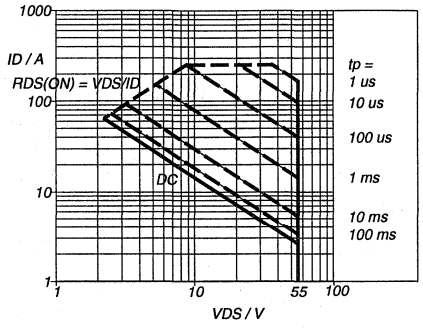


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

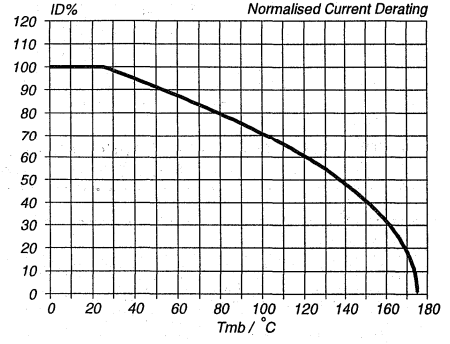


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

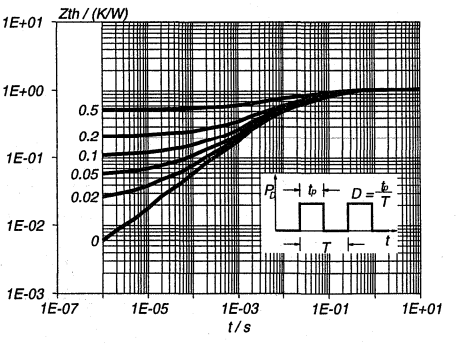


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

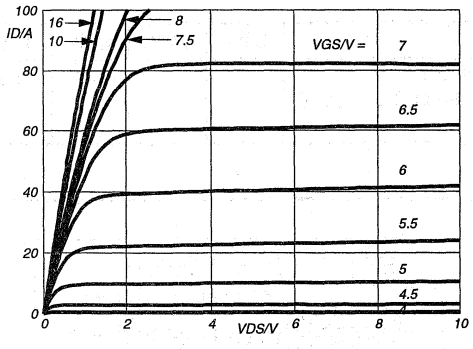


Fig.5. Typical output characteristics, $T_j = 25$ °C. $I_D = f(V_{DS})$; parameter V_{GS}

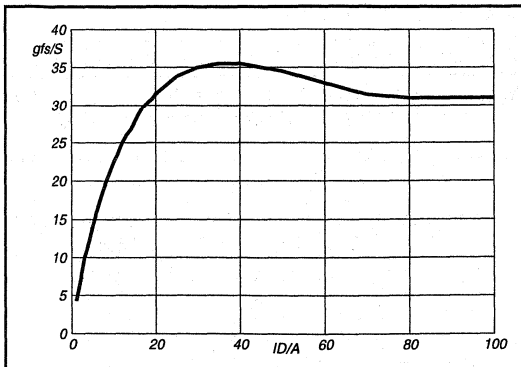


Fig.8. Typical transconductance, $T_j = 25$ °C. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

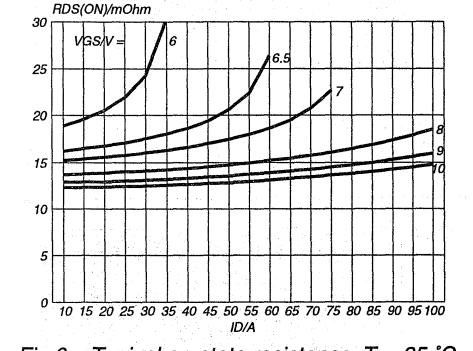


Fig.6. Typical on-state resistance, $T_j = 25$ °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

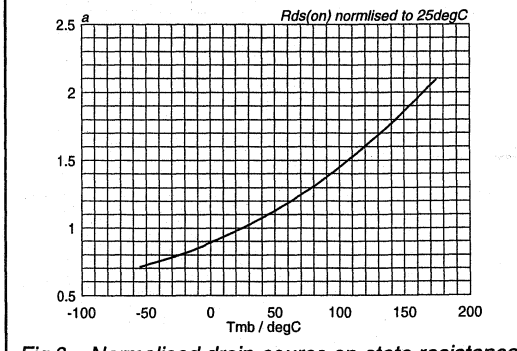


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 5$ V

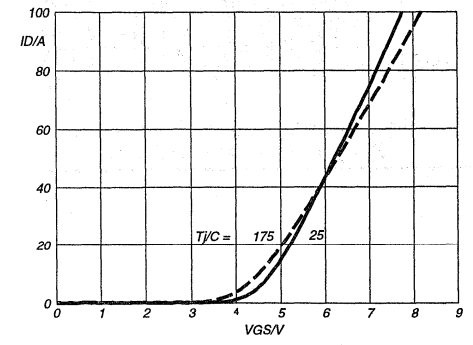


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

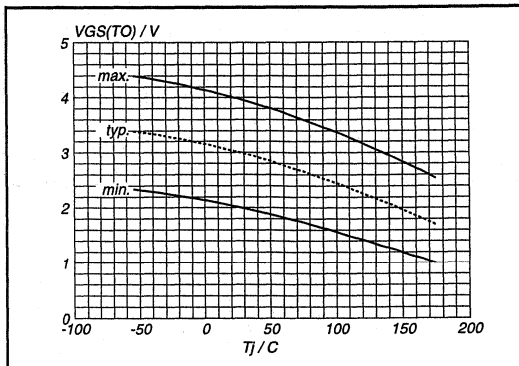


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

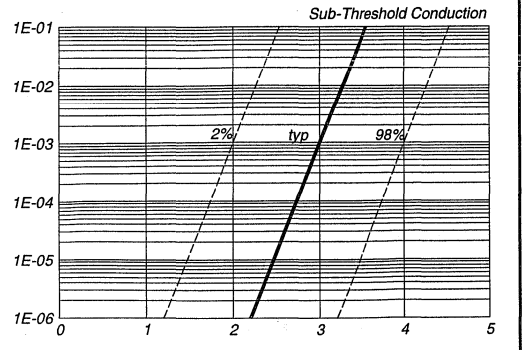


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

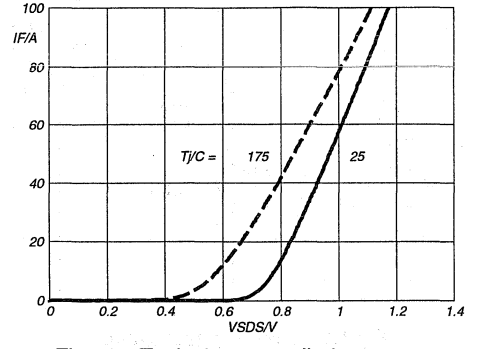


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

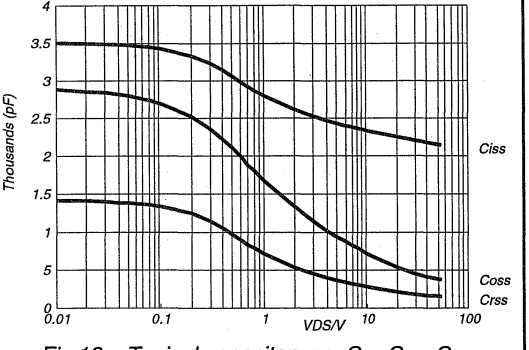


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

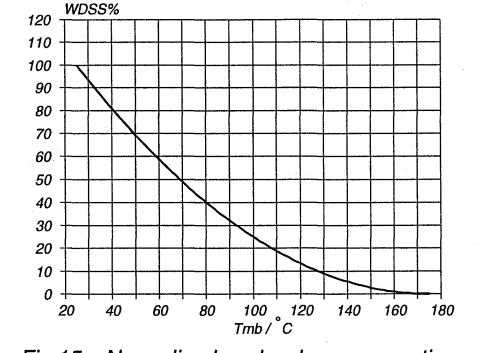


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

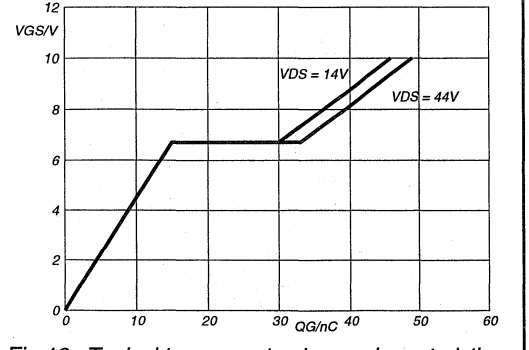


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

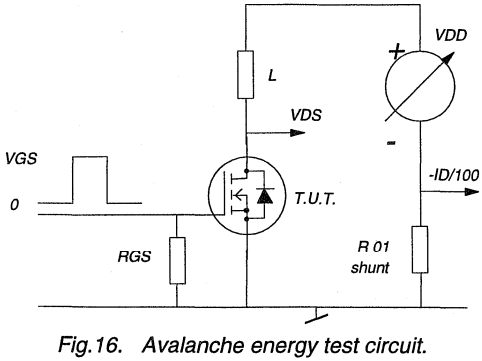


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

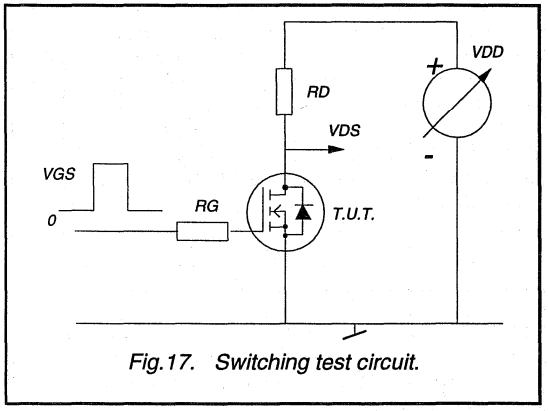


Fig.17. Switching test circuit.

TrenchMOS™ transistor Standard level FET

BUK7518-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

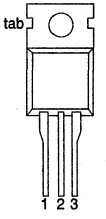
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	57	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	18	mΩ

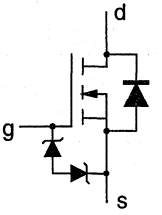
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	57	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	40	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	228	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	30	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	370	470	pF
C_{rss}	Feedback capacitance		-	170	250	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	15	22	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	30	60	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	35	50	ns
t_f	Turn-off fall time		-	25	38	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	57	A
I_{DRM}	Pulsed reverse drain current		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	48	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

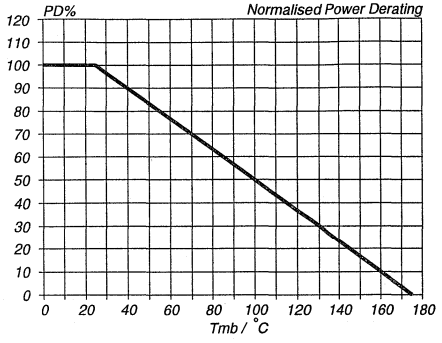


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

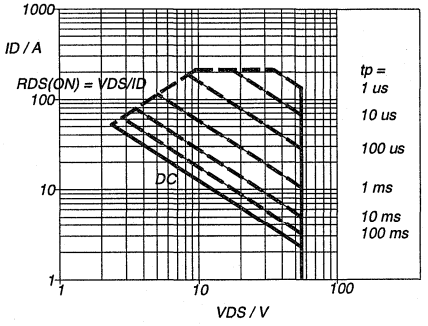


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

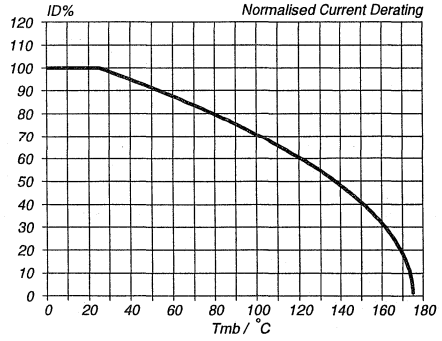


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

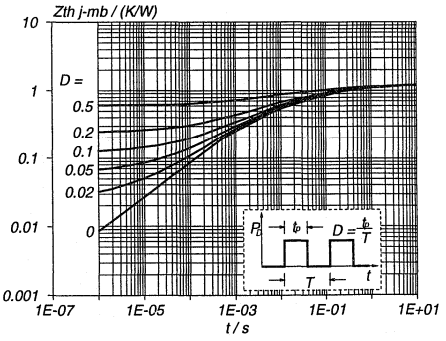


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

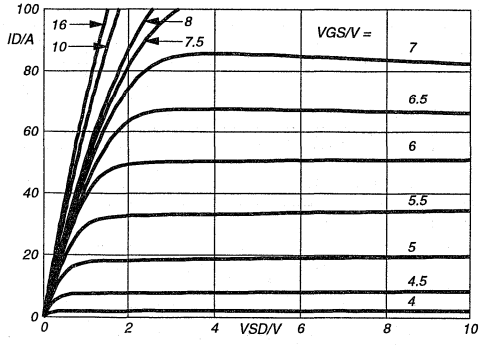


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

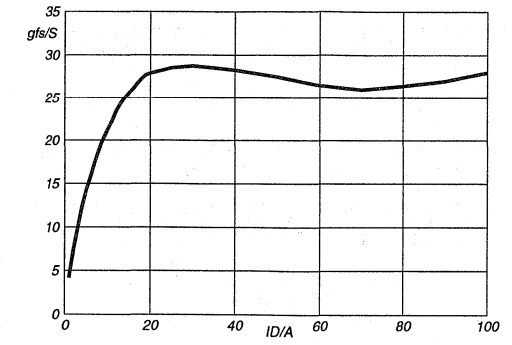


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

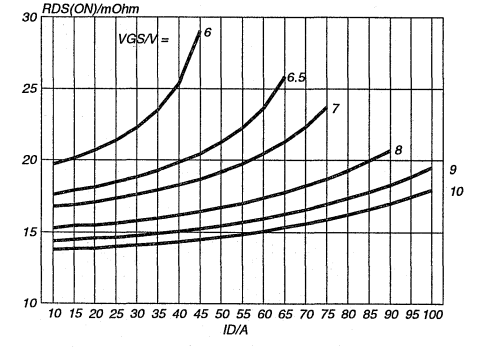


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

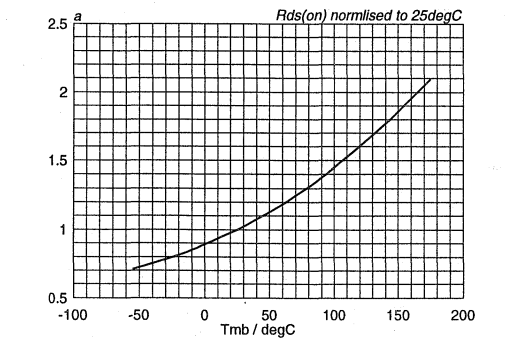


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ °C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

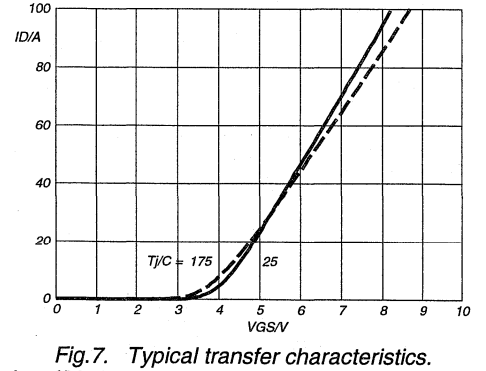


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

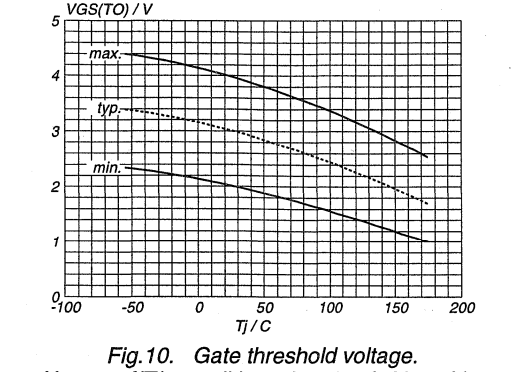


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

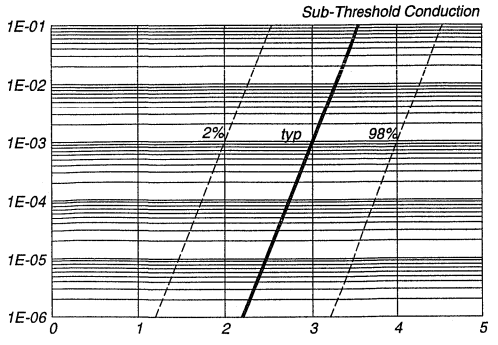


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

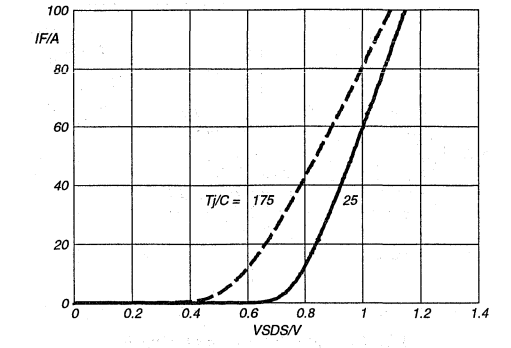


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

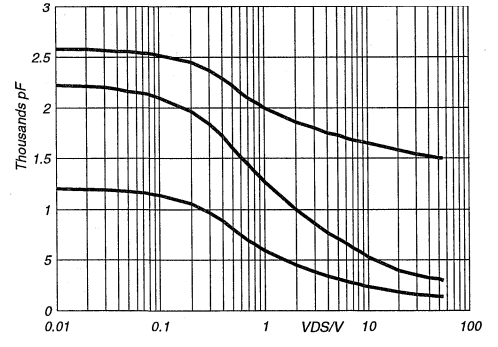


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

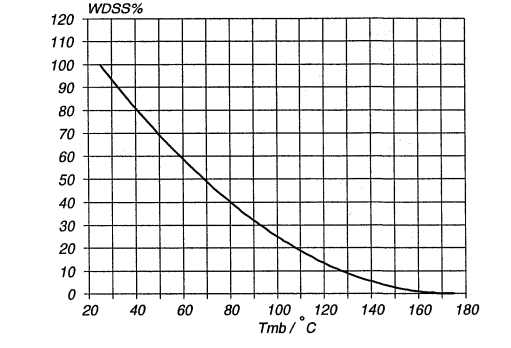


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

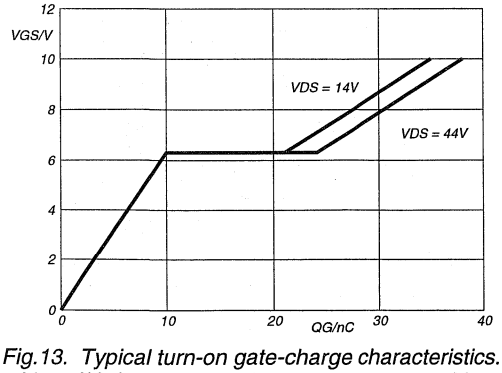


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

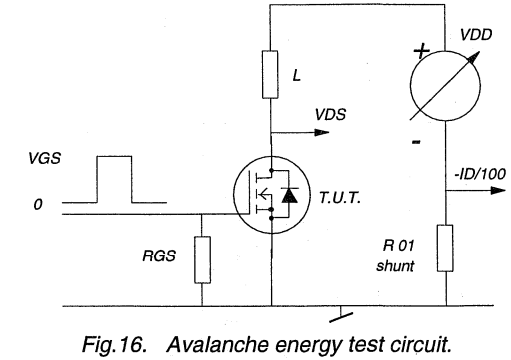


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

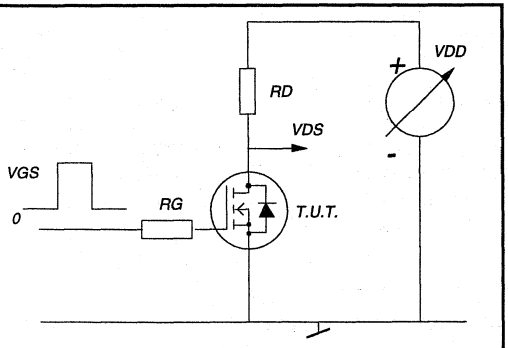


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Standard level FET

BUK7524-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

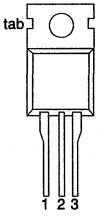
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	24	mΩ

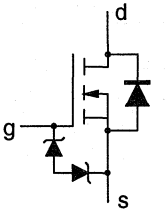
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	31	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	180	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	19	24	mΩ
		T_j = 175˚C	-	-	50	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	4	11	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1100	1500	pF
C_{oss}	Output capacitance		-	280	340	pF
C_{rss}	Feedback capacitance		-	130	180	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	12	18	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	19	35	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	25	35	ns
t_f	Turn-off fall time		-	18	25	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	45	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.07	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 40 A; $V_{DD} \leq 25$ V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

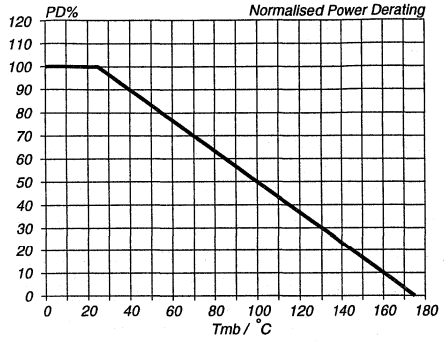


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

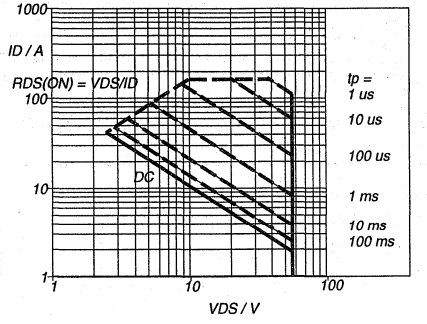


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

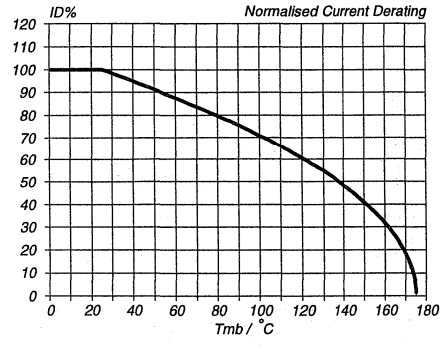


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

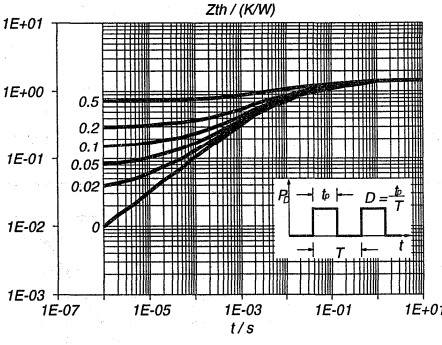


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

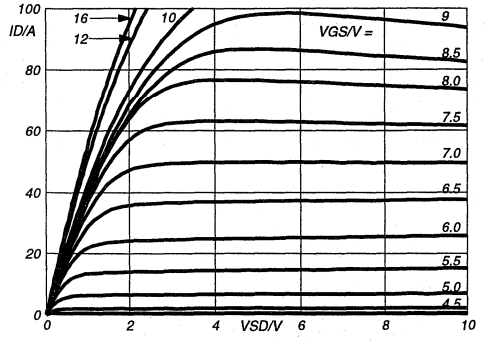


Fig.5. Typical output characteristics, $T_j = 25$ °C. $I_D = f(V_{DS})$; parameter V_{GS}

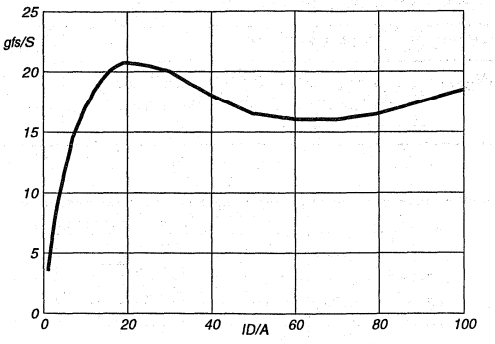


Fig.8. Typical transconductance, $T_j = 25$ °C. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

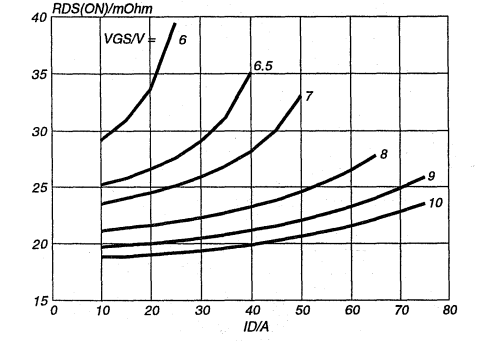


Fig.6. Typical on-state resistance, $T_j = 25$ °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

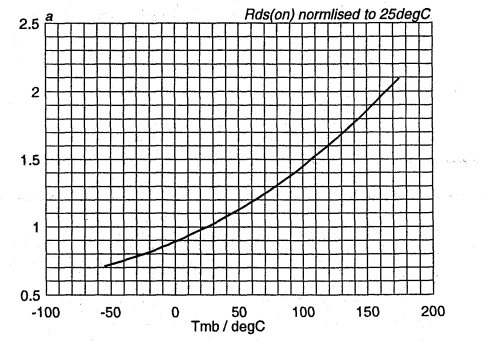


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 5$ V

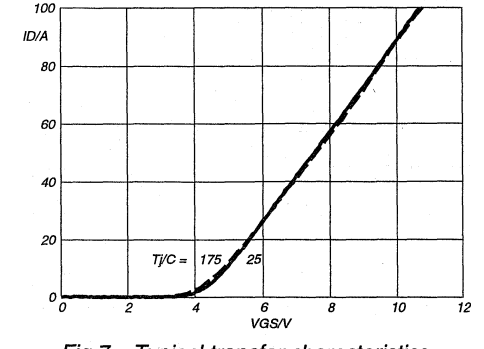


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

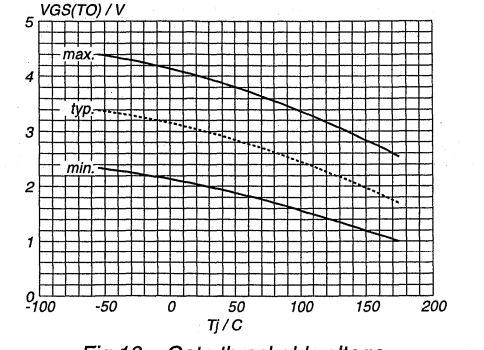


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

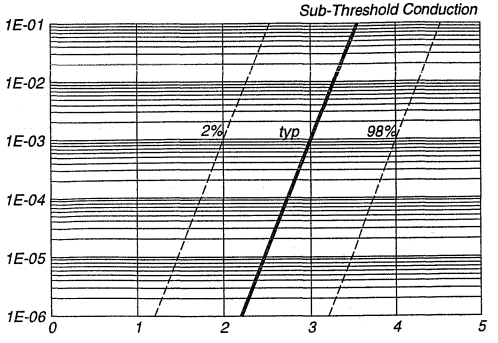


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

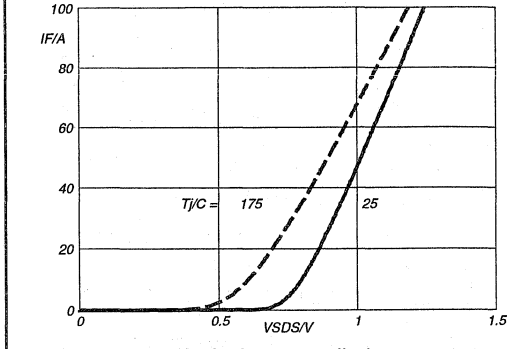


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

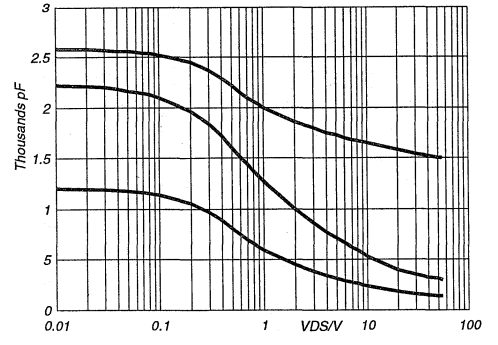


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

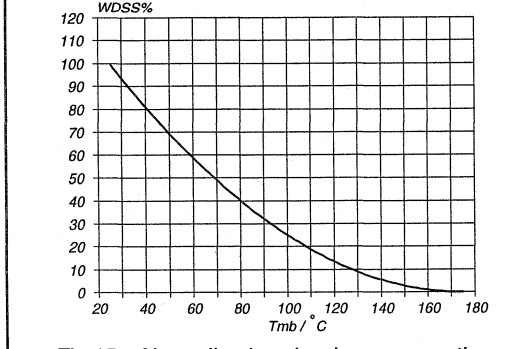


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

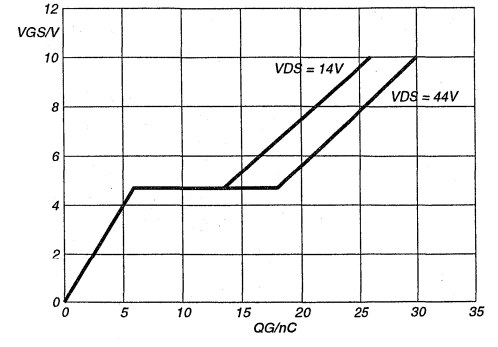


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

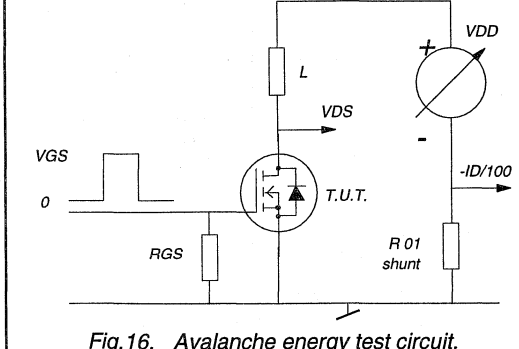


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

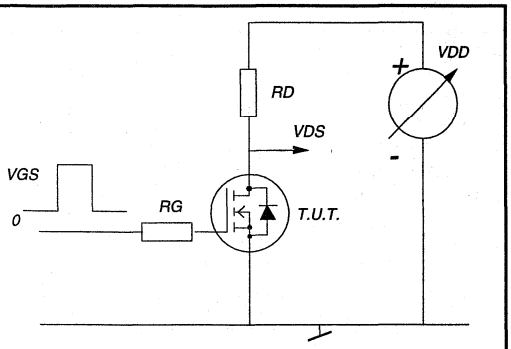


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Logic level FET

BUK9508-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

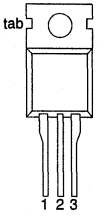
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	187	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	8	mΩ

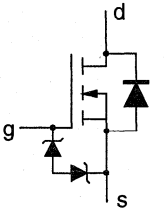
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	75	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	65	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	187	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	6.5	8	mΩ
		T_j = 175˚C	-	-	17	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	40	90	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5200	6900	pF
C_{oss}	Output capacitance		-	840	1000	pF
C_{rss}	Feedback capacitance		-	350	480	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	45	60	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	120	170	ns
$t_{d\,off}$	Turn-off delay time		-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.85	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 75 A; -dI_F/dt = 100 A/µs;	-	65	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 75 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	500	mJ

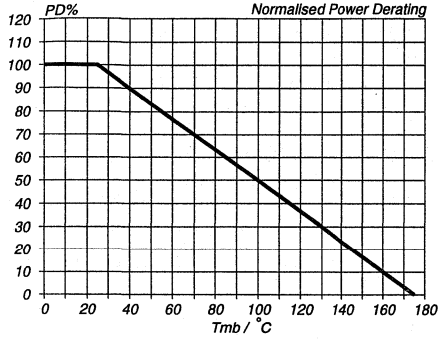


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

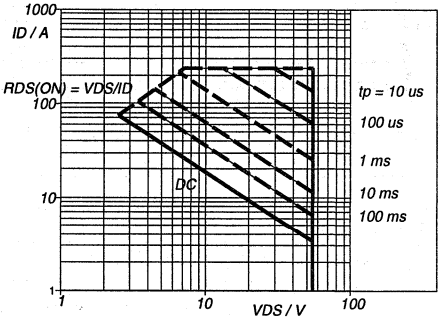


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

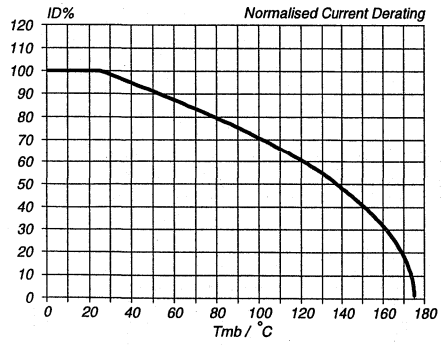


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

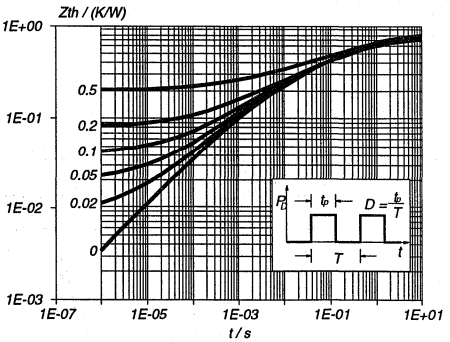


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

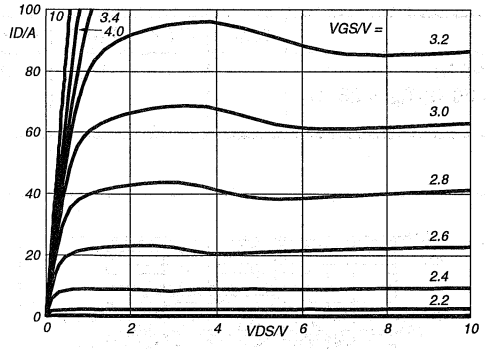


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

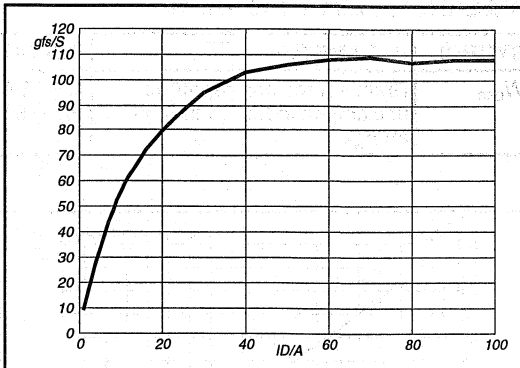


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

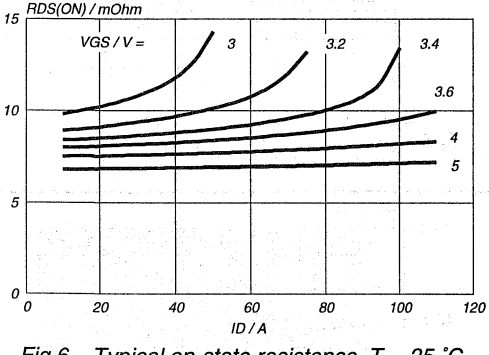


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

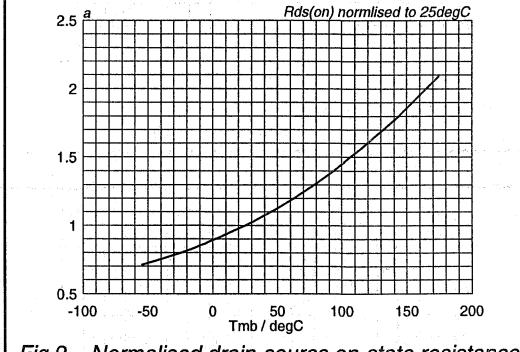


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

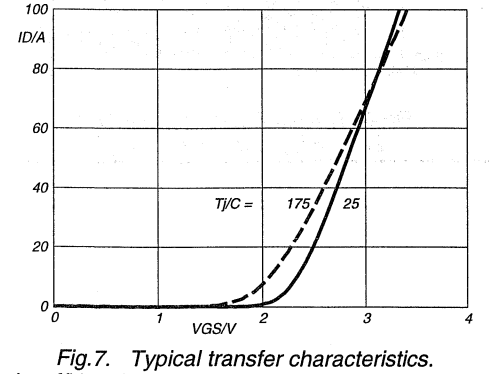


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

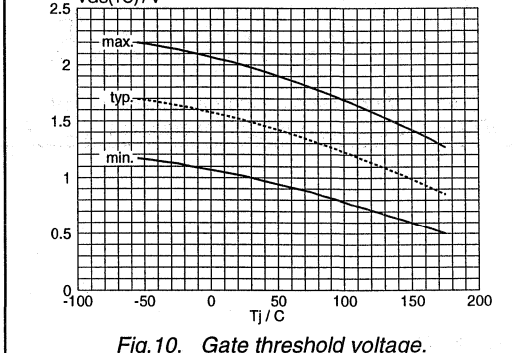


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

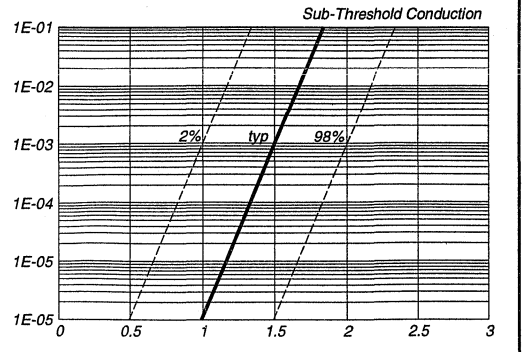


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

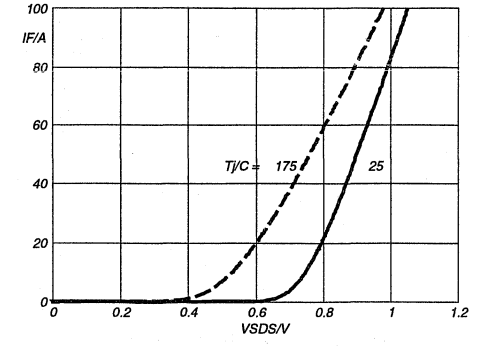


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

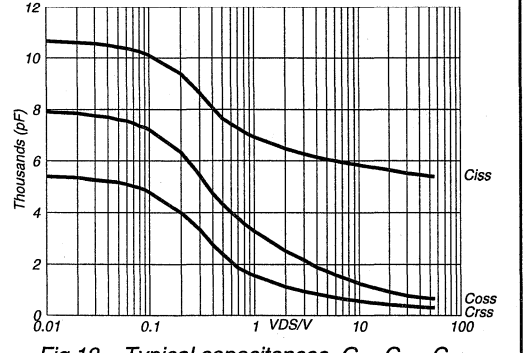


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

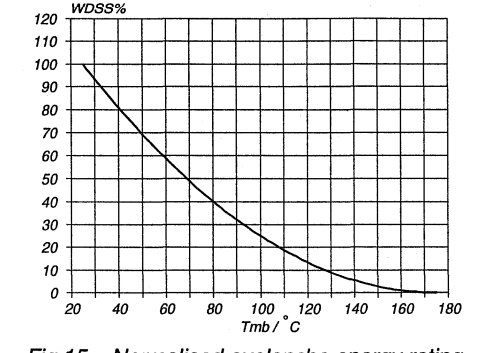


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

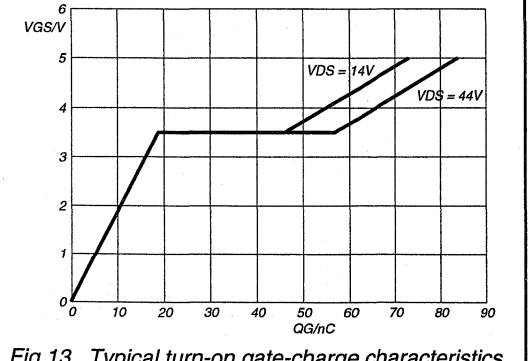


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

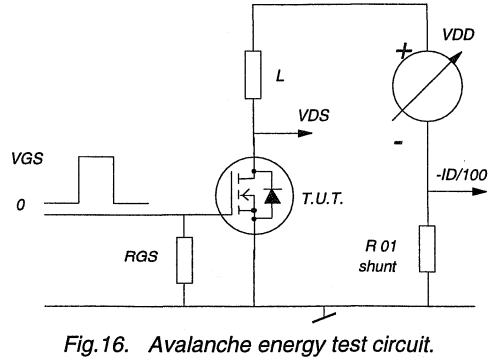


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

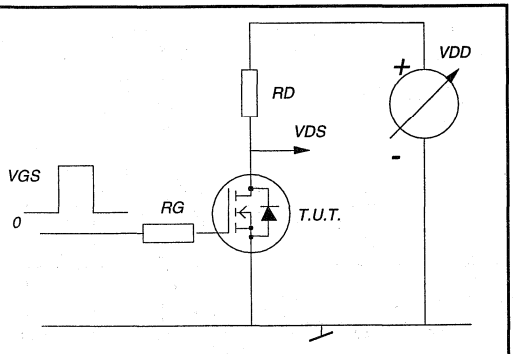


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9514-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

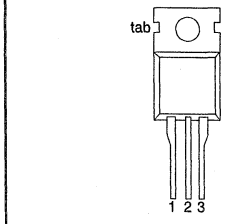
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	68	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	14	mΩ

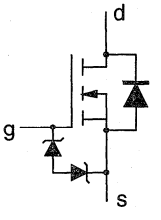
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	68	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	48	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	240	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	12	14	mΩ
		T_j = 175˚C	-	-	30	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	30	65	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2900	3800	pF
C_{oss}	Output capacitance		-	500	600	pF
C_{rss}	Feedback capacitance		-	240	330	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	35	50	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	95	145	ns
$t_{d\,off}$	Turn-off delay time		-	130	180	ns
t_f	Turn-off fall time		-	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	68	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 65 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 65 A; -dI_F/dt = 100 A/µs;	-	57	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.14	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 65 A; $V_{DD} \leq 25$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	200	mJ

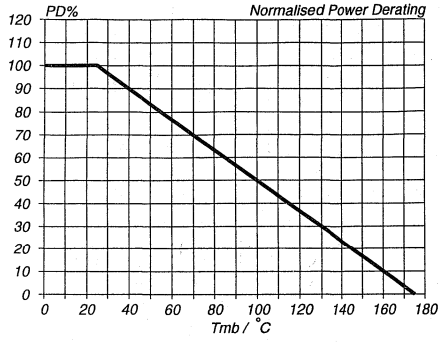


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

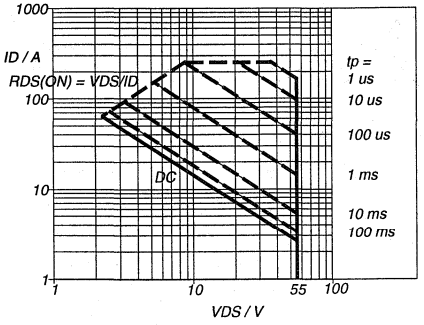


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

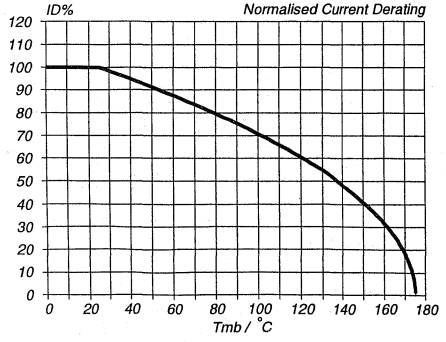


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

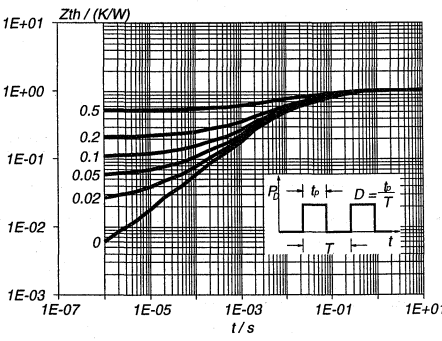


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

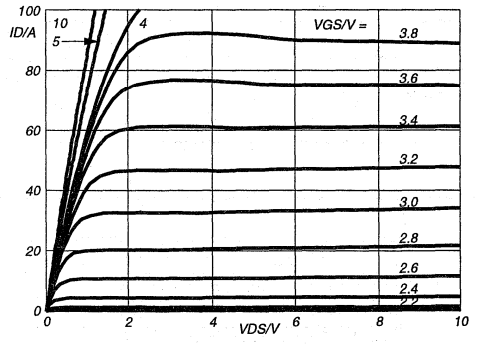


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

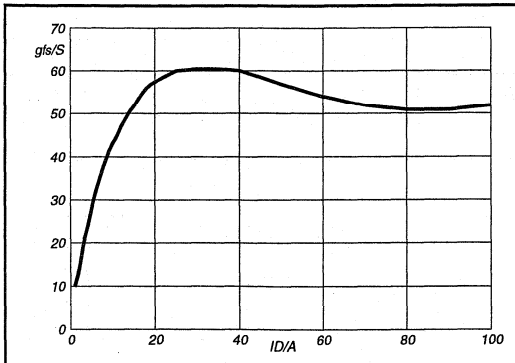


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

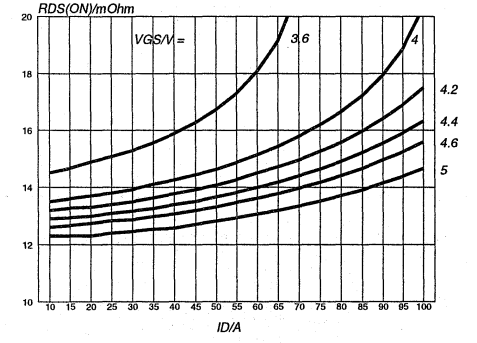


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

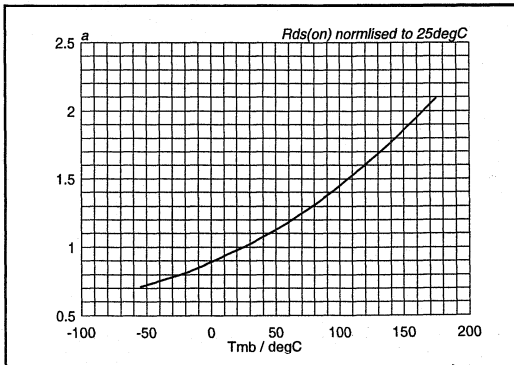


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

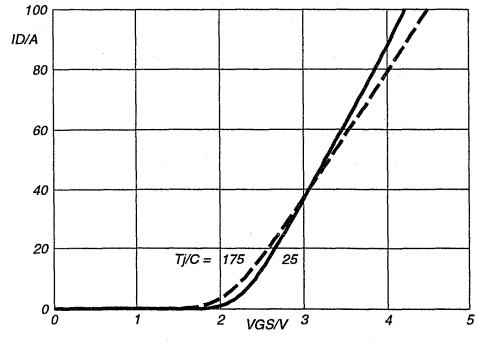


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

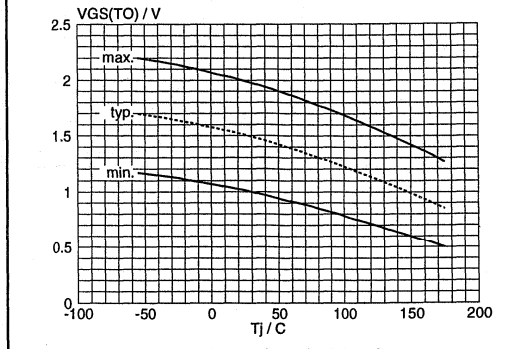


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

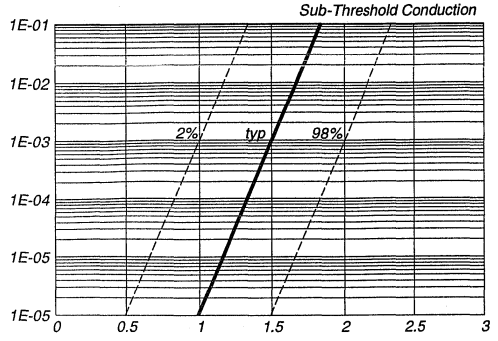


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

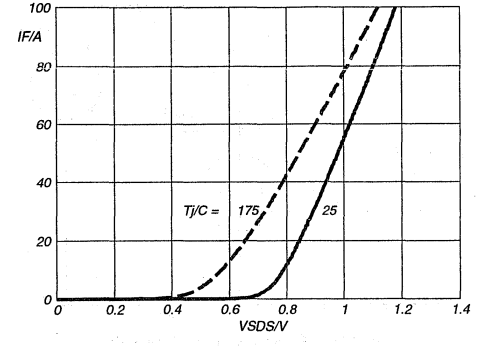


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

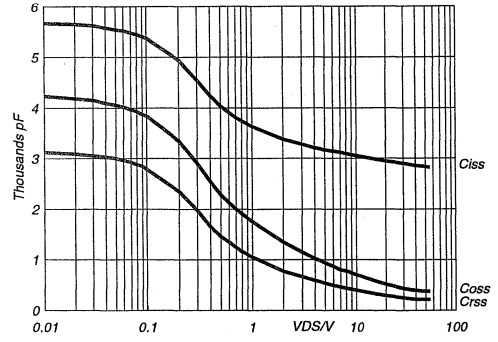


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

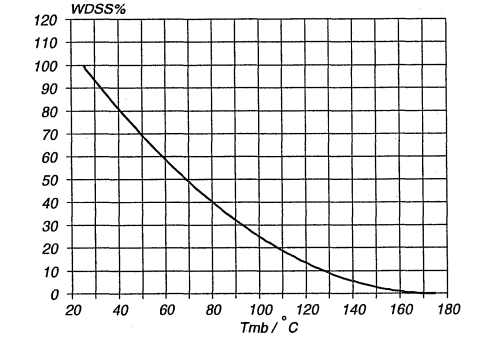


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

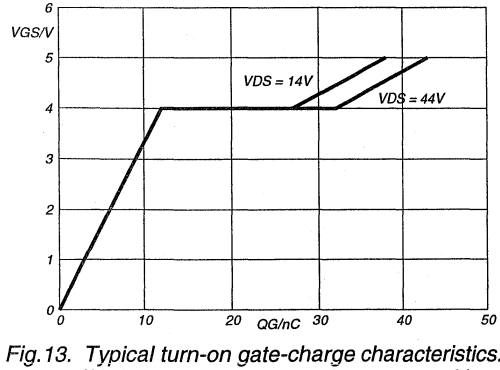


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

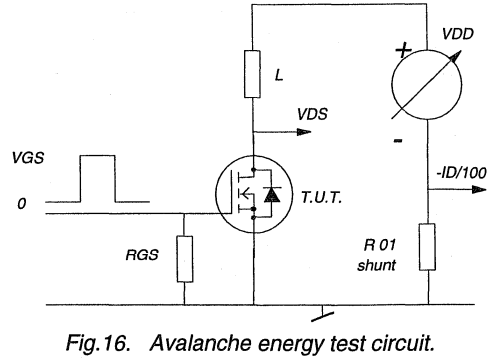


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

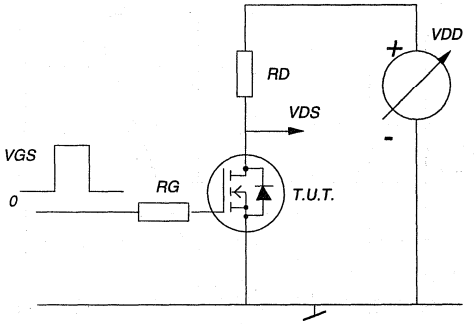


Fig.17. Switching test circuit.

TrenchMOS™ transistor
Logic level FET

BUK9518-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using **'trench'** technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

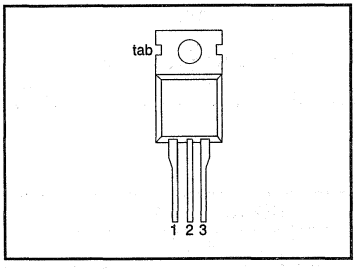
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	57	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	18	mΩ

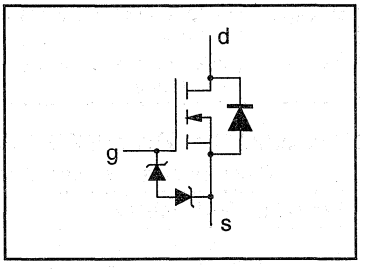
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	57	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	40	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	228	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	uA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	15	18	mΩ
		T_j = 175˚C	-	-	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	25	52	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2000	2600	pF
C_{oss}	Output capacitance		-	390	490	pF
C_{rss}	Feedback capacitance		-	200	290	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time		-	100	140	ns
t_f	Turn-off fall time		-	50	75	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	57	A
I_{DRM}	Pulsed reverse drain current		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	48	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.1	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 50 A; $V_{DD} \leq 25$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	125	mJ

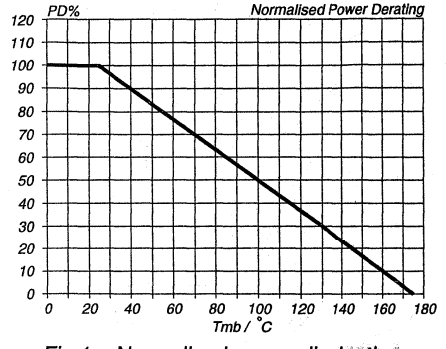


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

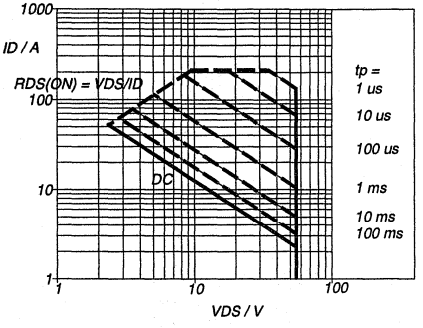


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

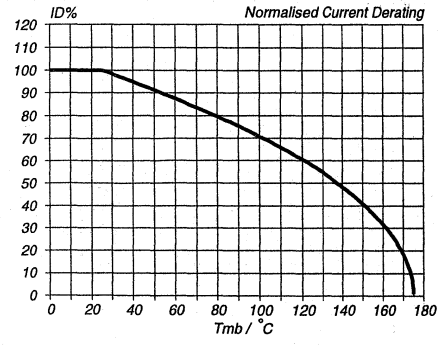


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

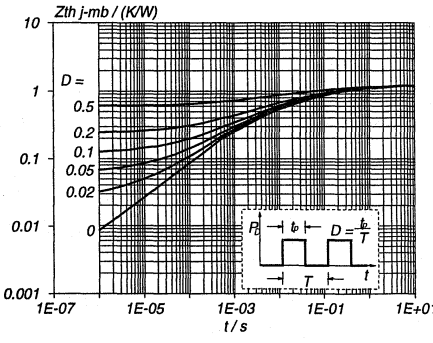


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

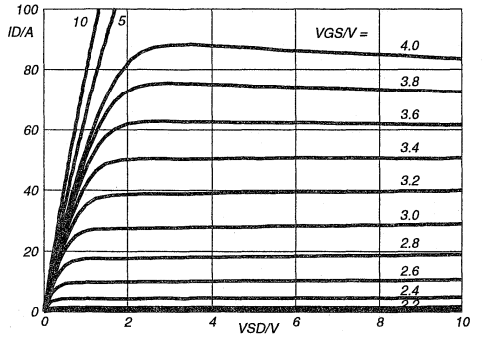


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

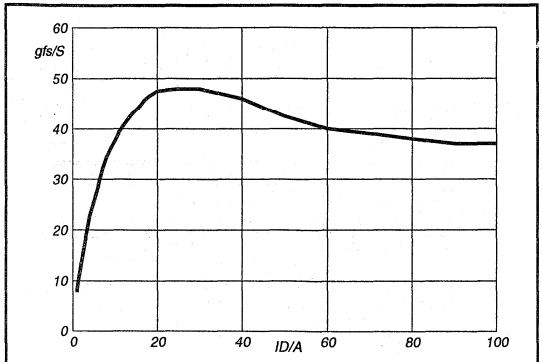


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

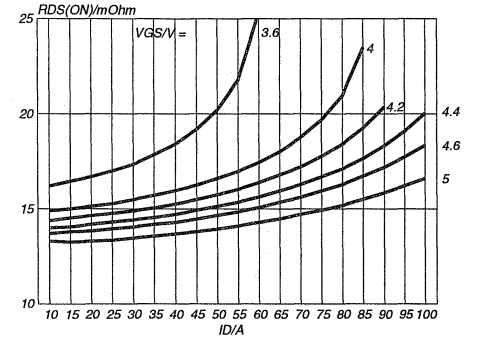


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

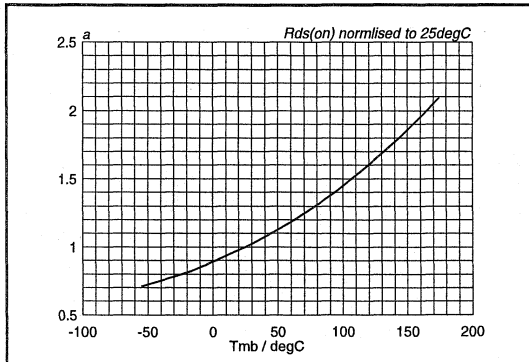


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 5$ V

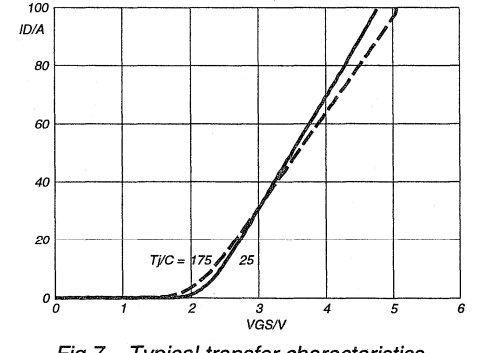


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

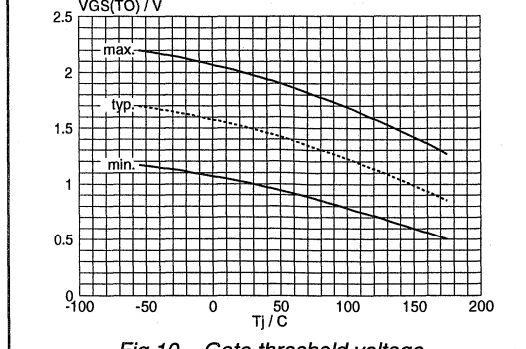


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

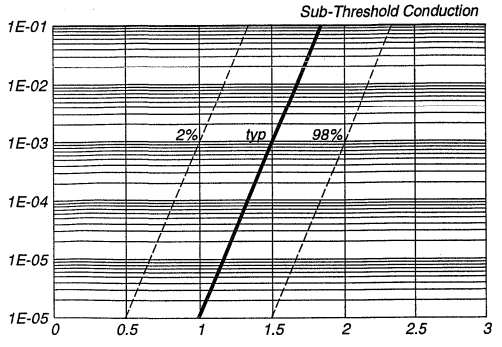


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

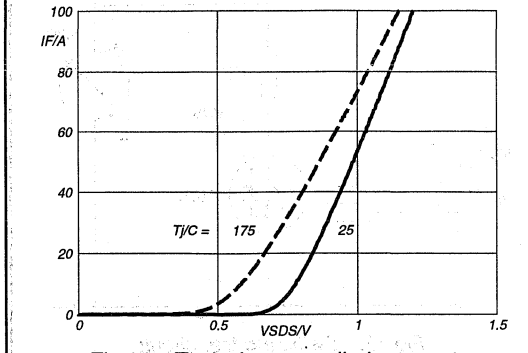


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

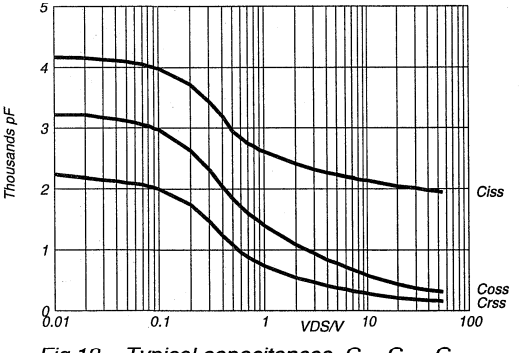


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

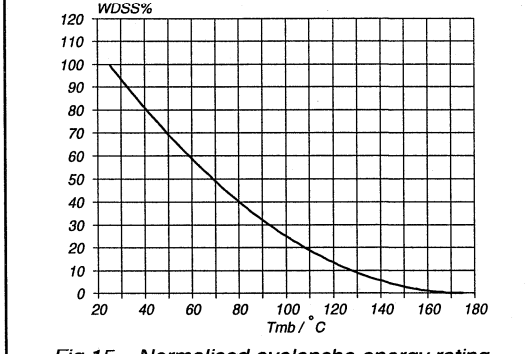


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

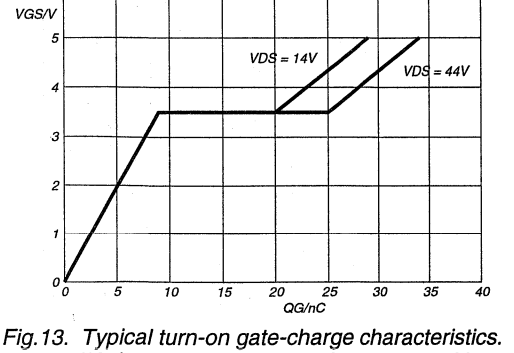


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

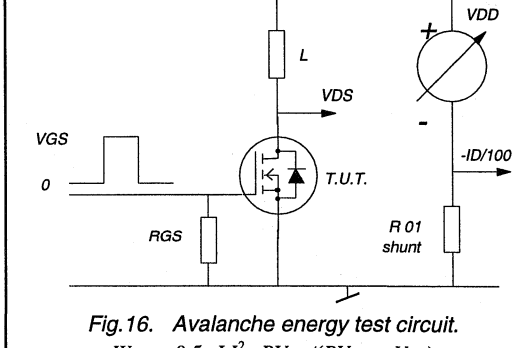


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

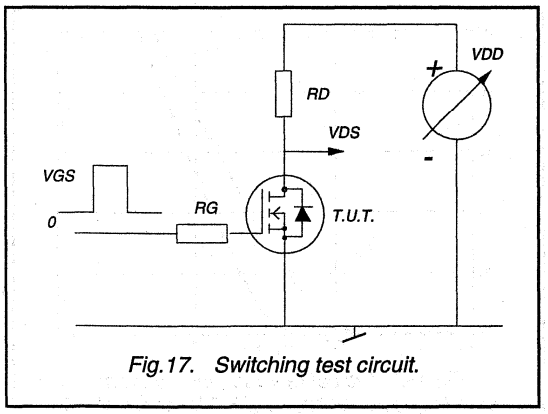


Fig.17. Switching test circuit.

TrenchMOS™ transistor Logic level FET

BUK9524-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

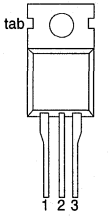
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	45	A
P_{tot}	Total power dissipation	103	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	24	mΩ

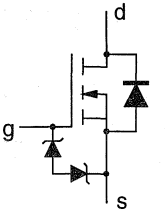
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	45	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	31	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	180	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	103	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.45	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-		10	µA
$\pm V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	-	19	24	mΩ
		T_j = 175˚C	-	-	50	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	15	40	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	300	360	pF
C_{rss}	Feedback capacitance		-	150	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	30	45	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	80	130	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	45	A
I_{DRM}	Pulsed reverse drain current		-	-	160	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.07	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 40 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 °C	-	-	80	mJ

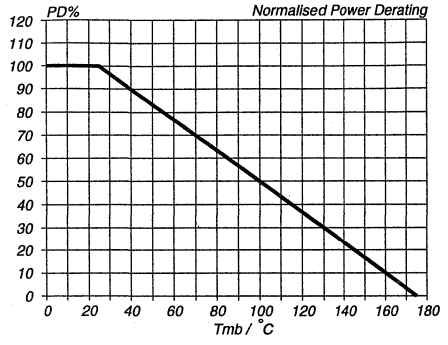


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

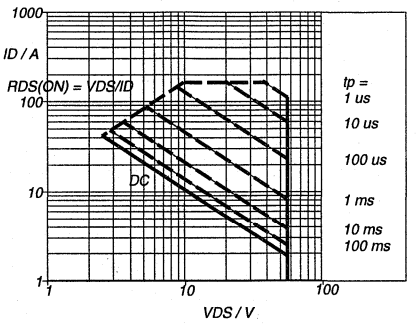


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

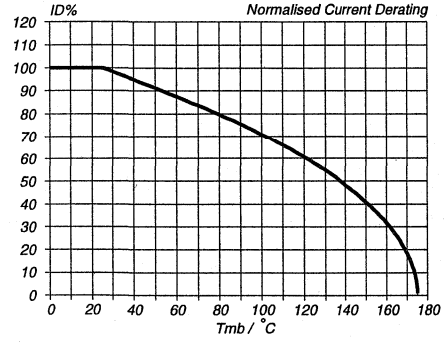


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

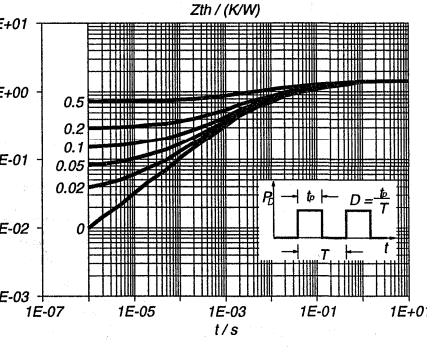


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

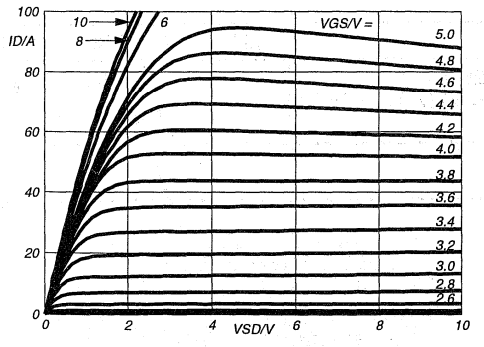


Fig.5. Typical output characteristics, $T_j = 25$ °C. $I_D = f(V_{DS})$; parameter V_{GS}

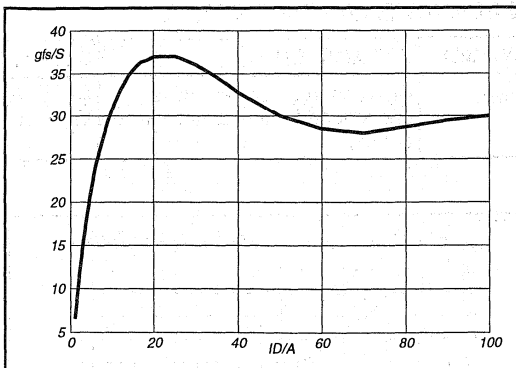


Fig.8. Typical transconductance, $T_j = 25$ °C. $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

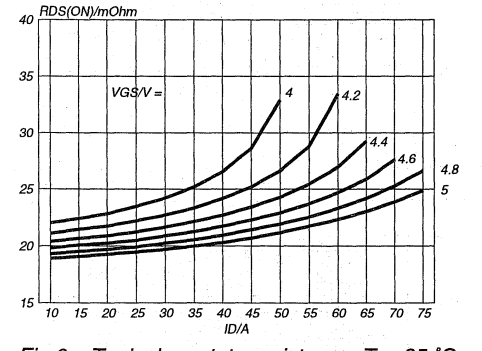


Fig.6. Typical on-state resistance, $T_j = 25$ °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

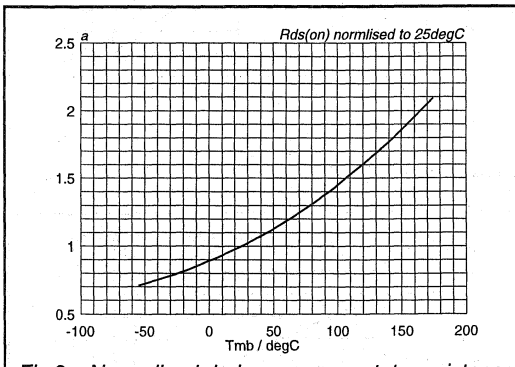


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 25$ A; $V_{GS} = 5$ V

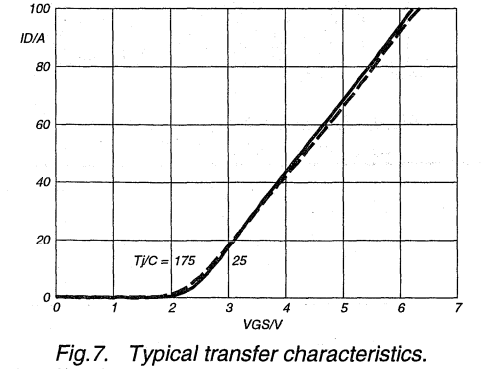


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

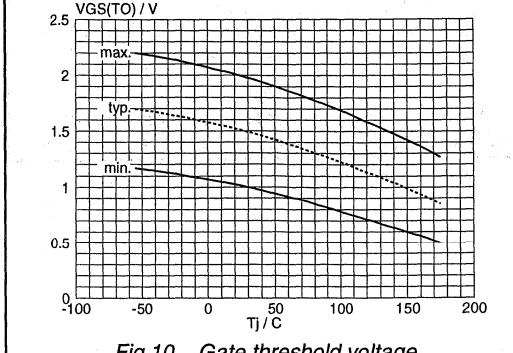


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

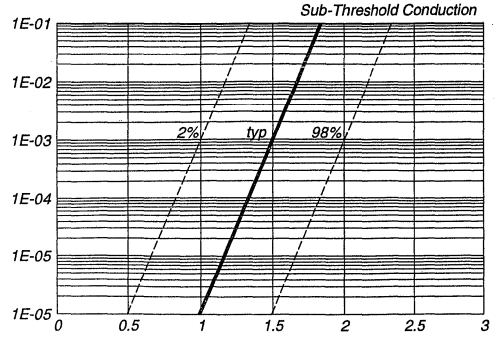


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

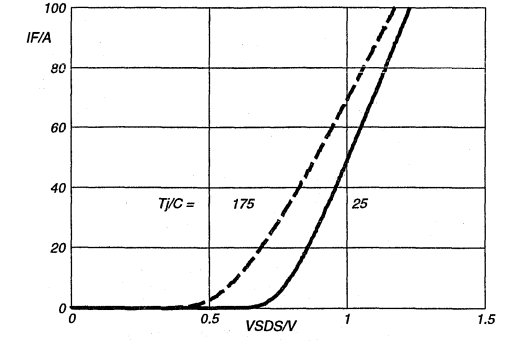


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

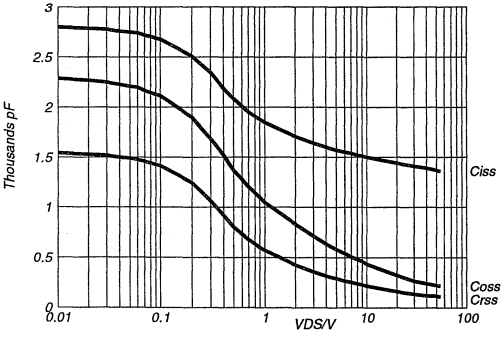


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

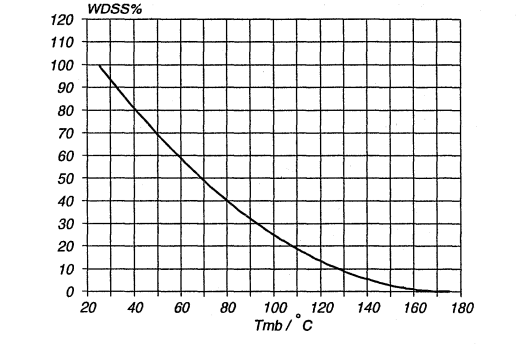


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

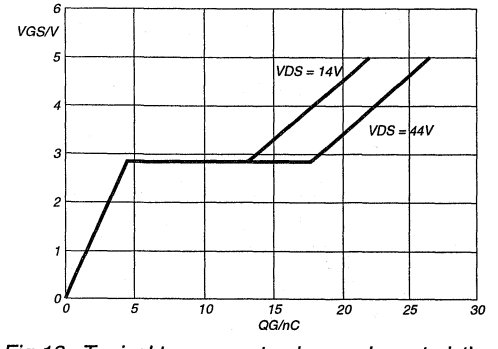


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

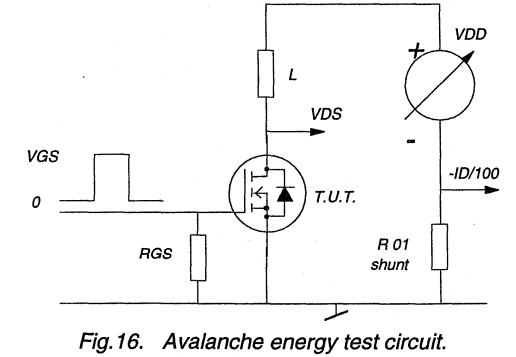


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

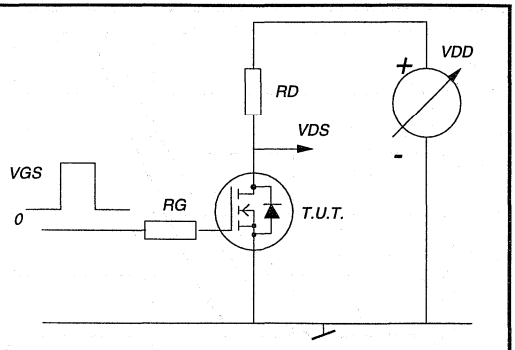


Fig.17. Switching test circuit.

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

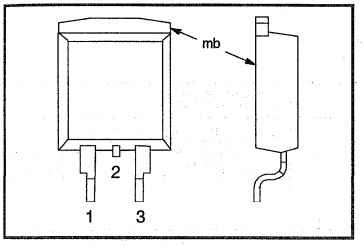
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	41	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	38	mΩ

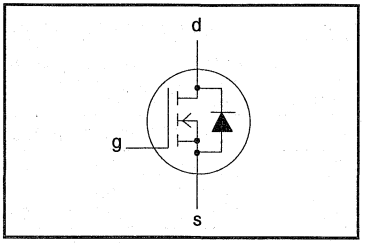
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig. 18).	50	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	30	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	7	14	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	900	1600	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	55	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	75	125	ns
t_f	Turn-off fall time		-	60	100	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

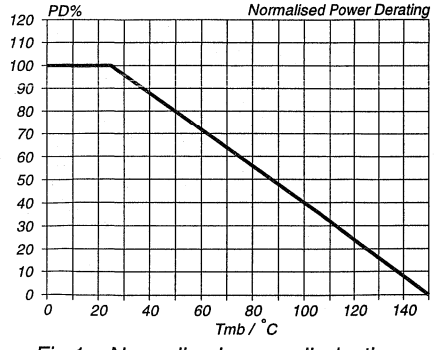


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

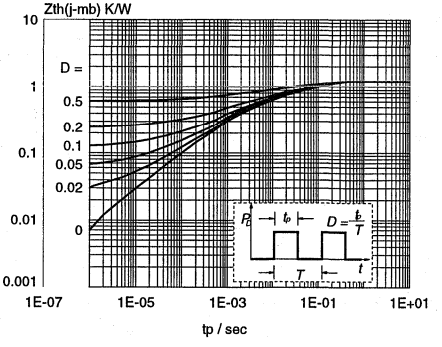


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

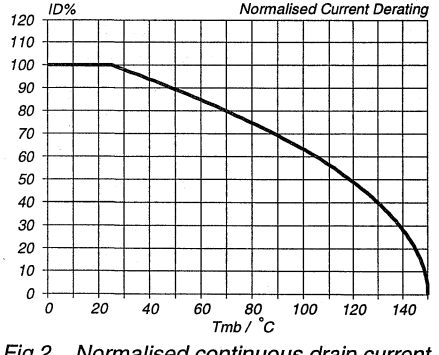


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

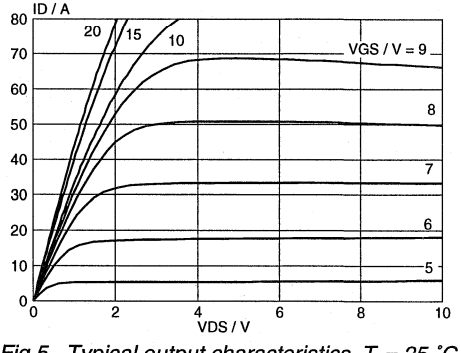


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

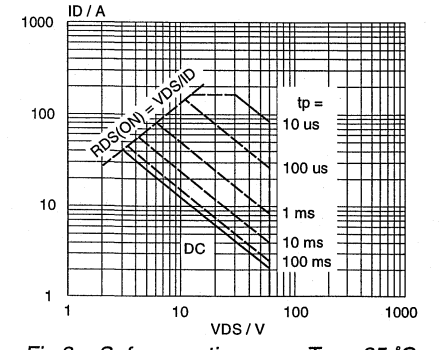


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

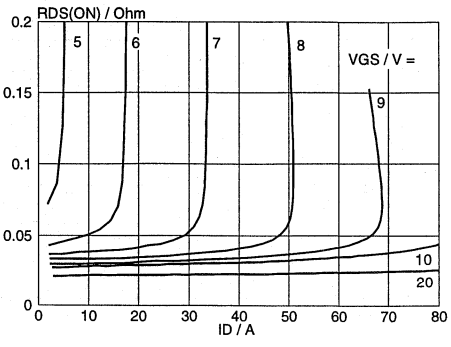


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

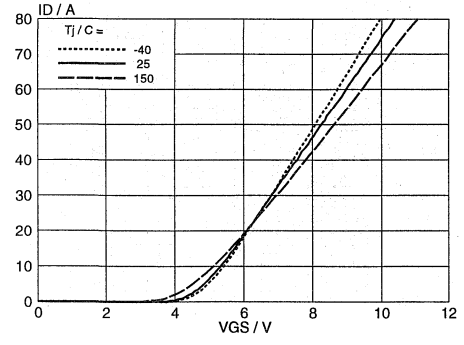


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 15 V; parameter T_j

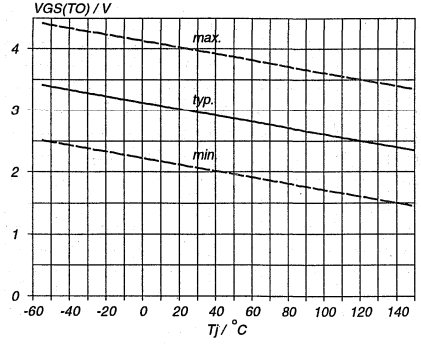


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

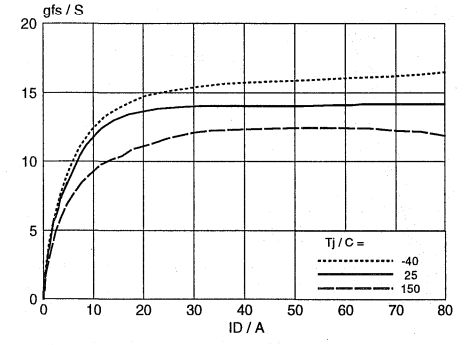


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

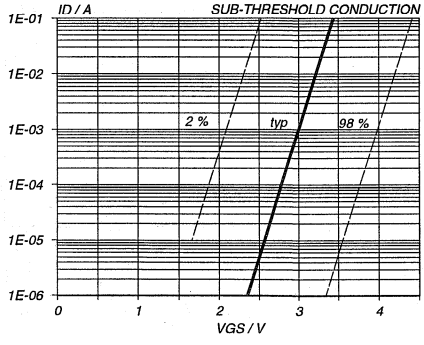


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

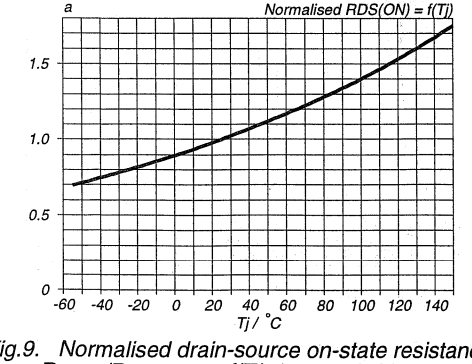


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

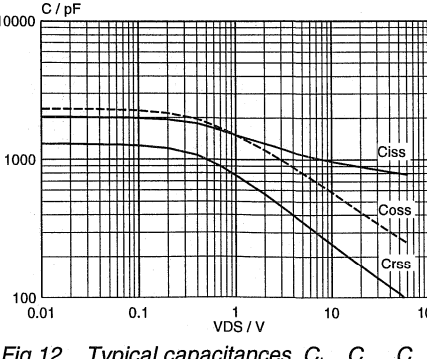


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

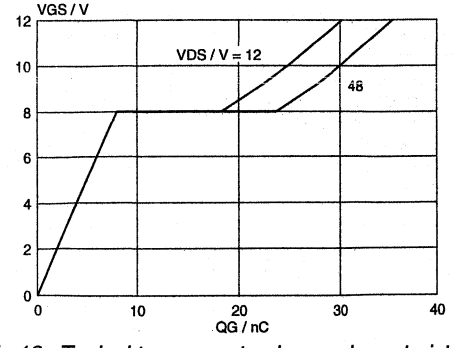


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

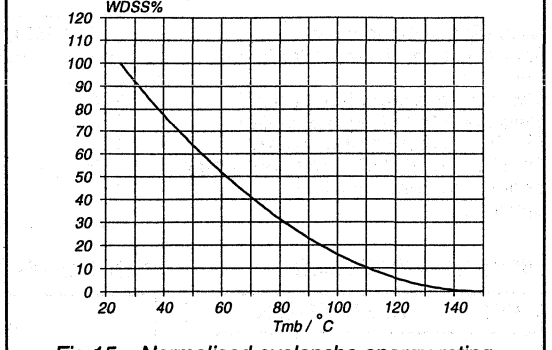


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

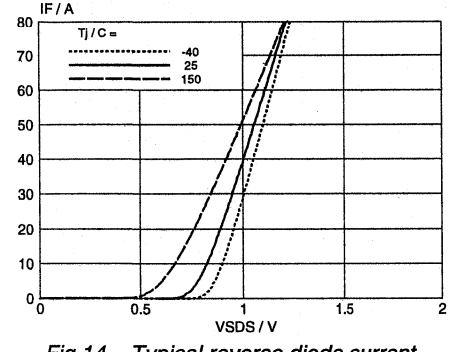


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

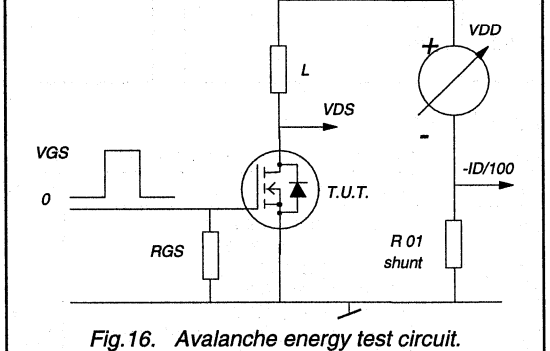


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

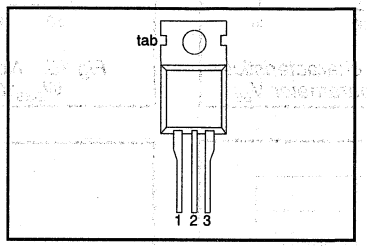
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	11	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.25	Ω

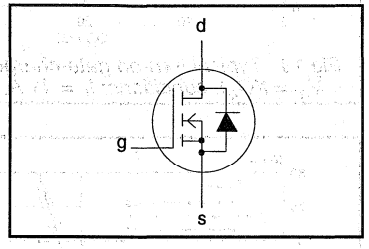
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	11	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	7.7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	44	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A	-	0.22	0.25	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	3	4.2	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	11	A
I_{DRM}	Pulsed reverse drain current	-	-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.35	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 11 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	35	mJ

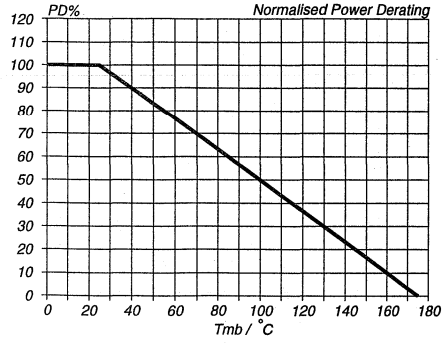


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

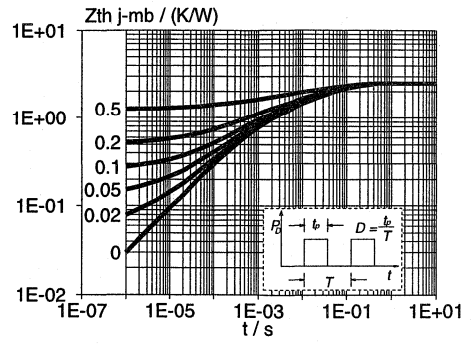


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

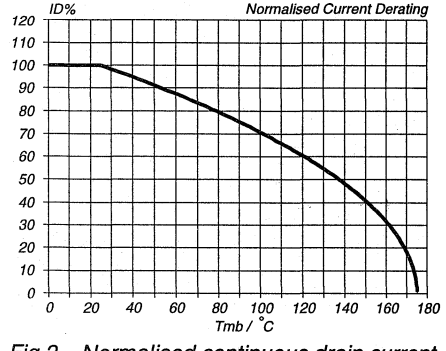


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

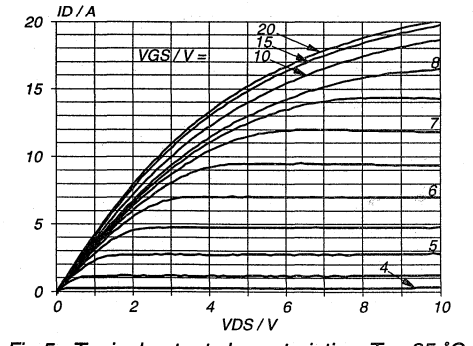


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

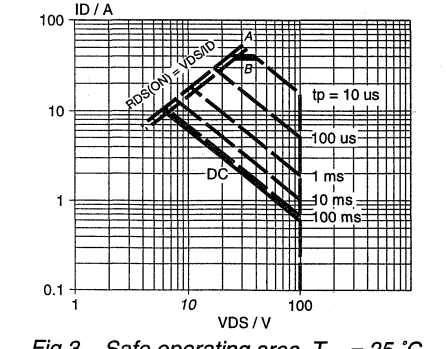


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

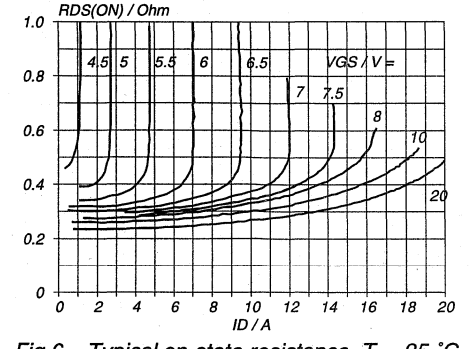


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

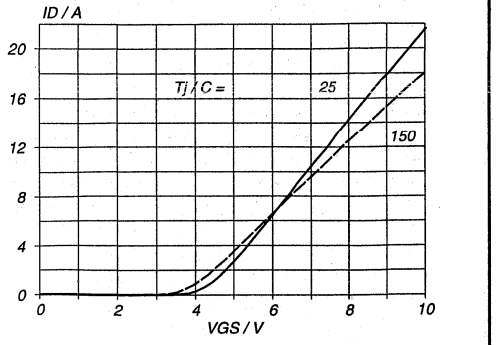


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

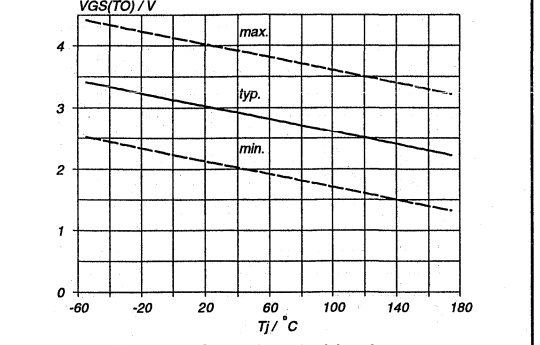


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

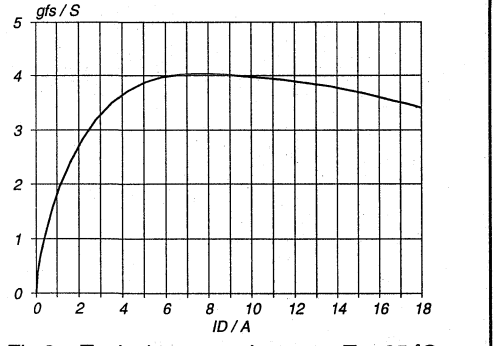


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

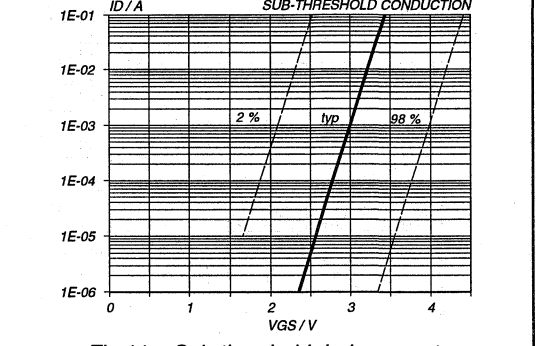


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

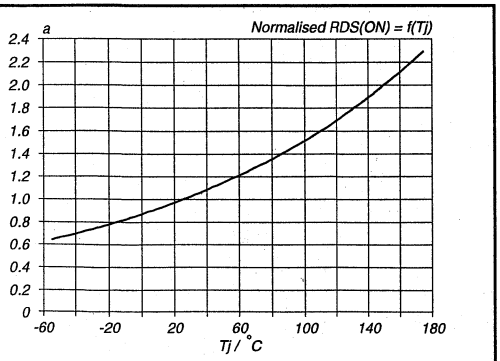


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

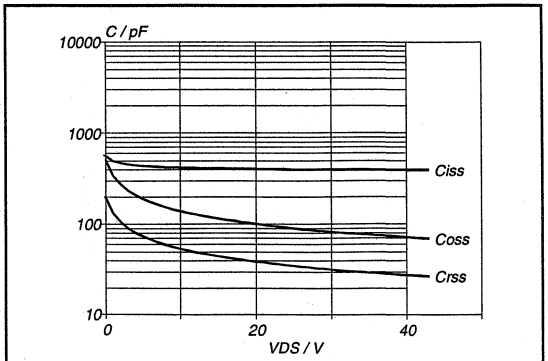


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

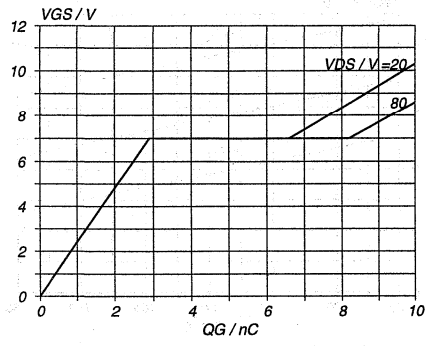


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 11$ A; parameter V_{DS}

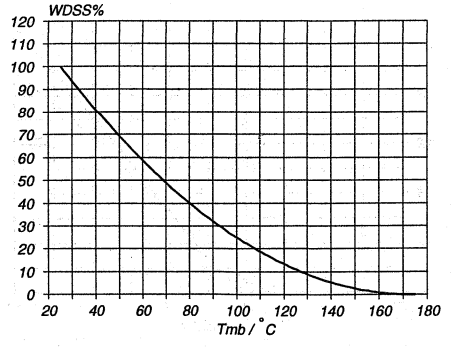


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 11$ A

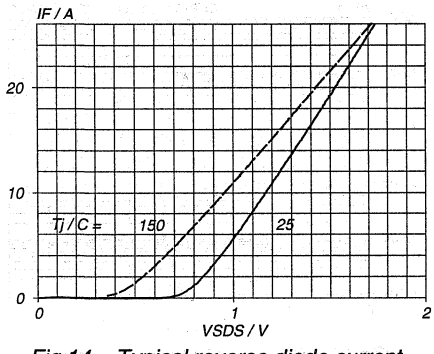


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

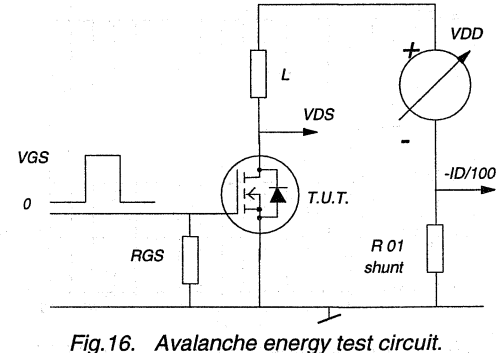


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor PHP10N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

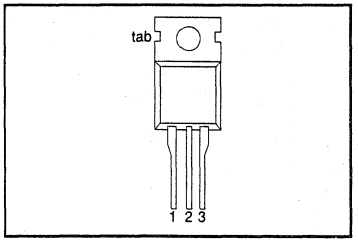
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	10	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.55	Ω

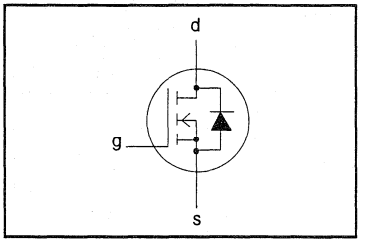
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	10	A
		T_{mb} = 100 °C	-	6.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	40	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	10	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	520	mJ
		T_j = 100°C prior to surge	-	83	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	13	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	0.4	0.55	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 10 A ;V_{GS} = 0 V	-	1.4	2.0	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 5 A	4	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	1800	pF
C_{oss}	Output capacitance		-	170	270	pF
C_{rss}	Feedback capacitance		-	70	120	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 10 A; V_{DS} = 320 V	-	65	-	nC
Q_{gs}	Gate to source charge		-	8	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	37	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.8 A;	-	20	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	200	250	ns
t_f	Turn-off fall time		-	75	90	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	500	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6.0	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor PHP12N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

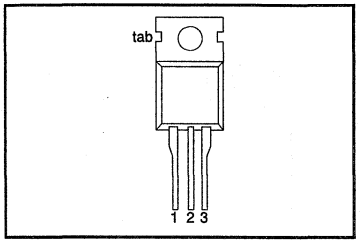
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	Ω

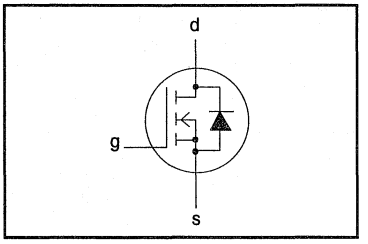
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	14	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	10	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	4.0	5.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	I_F = 14 A ; V_{GS} = 0 V	-	1.2	1.5	V
t_{rr}	Reverse recovery time	I_F = 14 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 14 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	70	mJ

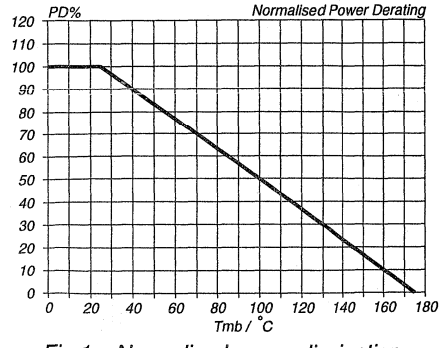


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

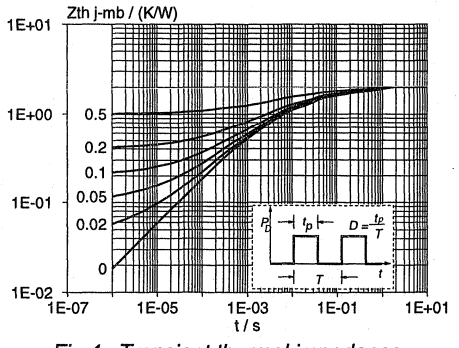


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

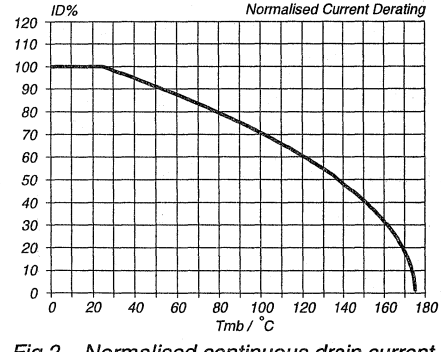


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

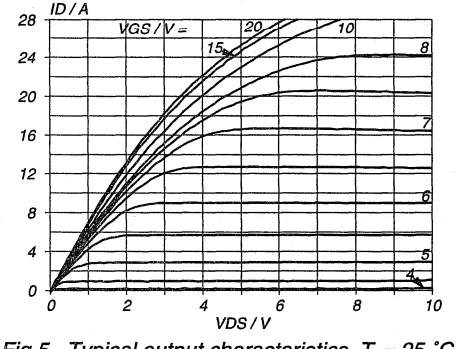


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

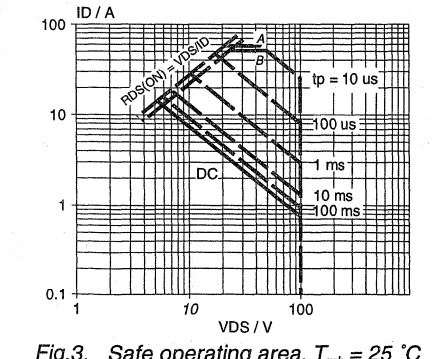


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

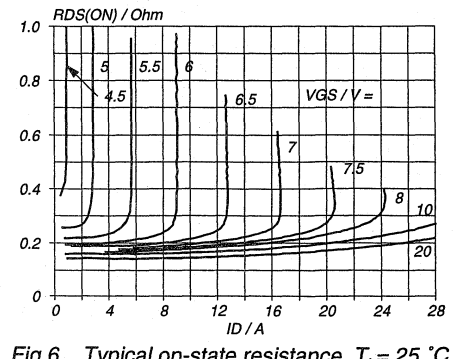


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

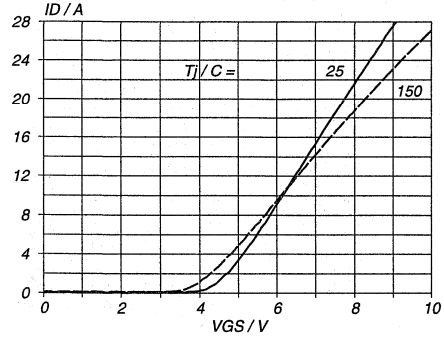


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

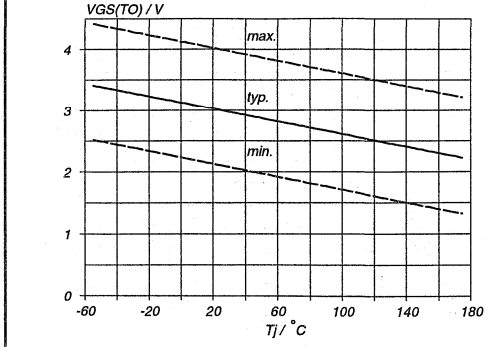


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

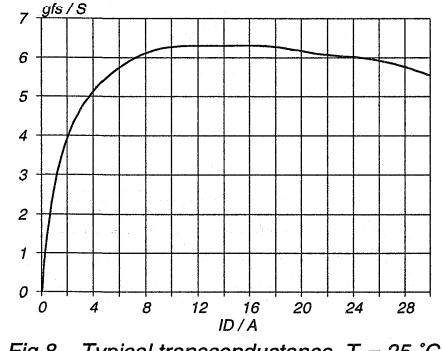


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

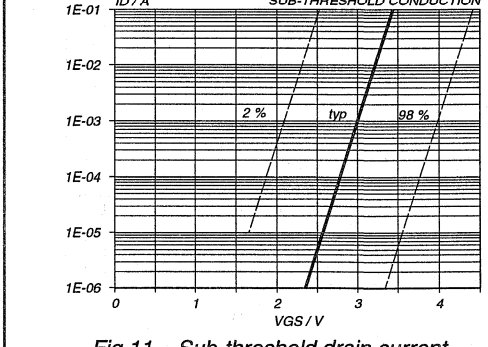


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

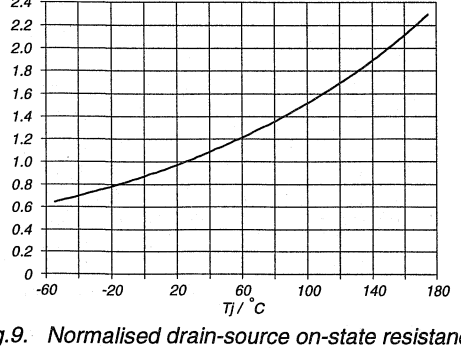


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 5$ A; $V_{GS} = 10$ V

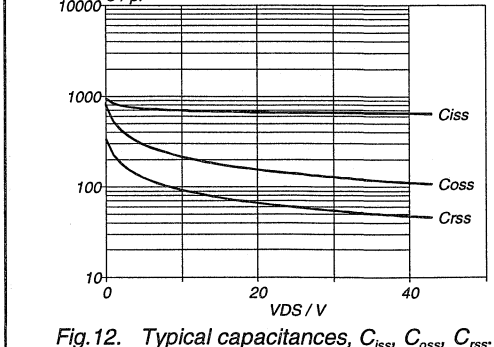


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

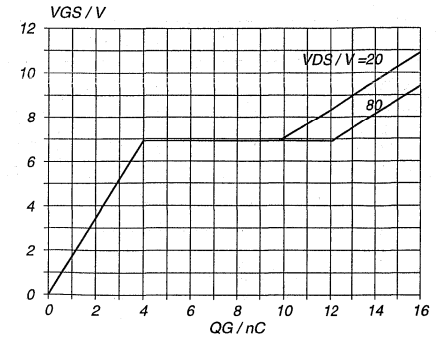


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

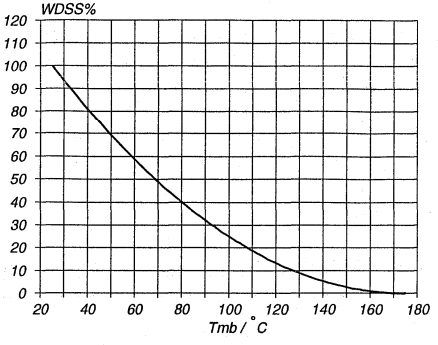


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

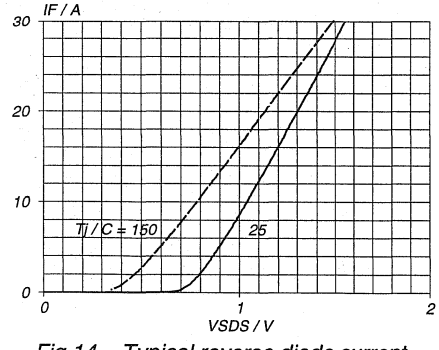


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

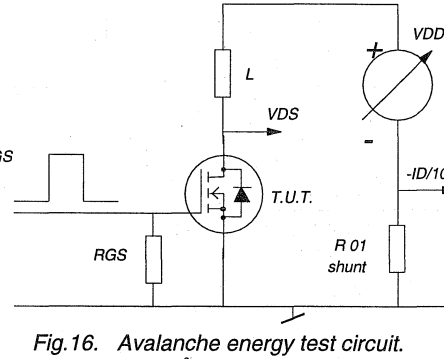


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

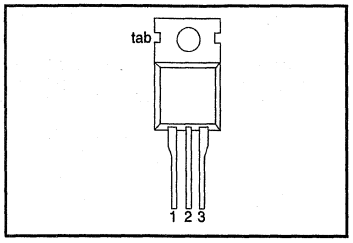
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	15	A
P_{tot}	Total power dissipation	60	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.13	Ω

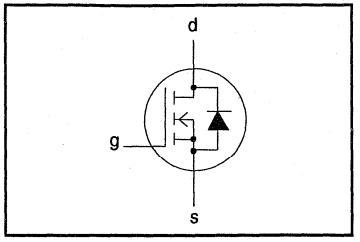
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	15	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	11	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	60	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	60	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 8.5 A	-	0.11	0.13	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8.5 A	3.5	4.7	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	150	200	pF
C_{rss}	Feedback capacitance		-	70	100	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	8	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	45	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	15	A
I_{DRM}	Pulsed reverse drain current	-	-	-	60	A
V_{SD}	Diode forward voltage	I_F = 15 A ; V_{GS} = 0 V	-	1.4	1.7	V
t_{rr}	Reverse recovery time	I_F = 15 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.18	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 15 A ; $V_{DD} \leq$ 30 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	30	mJ

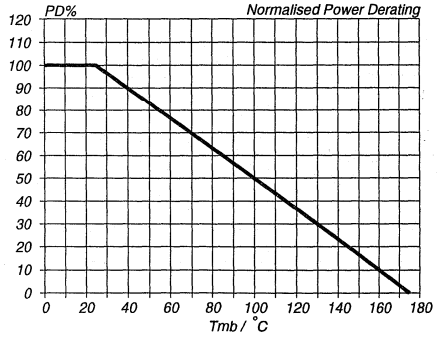


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

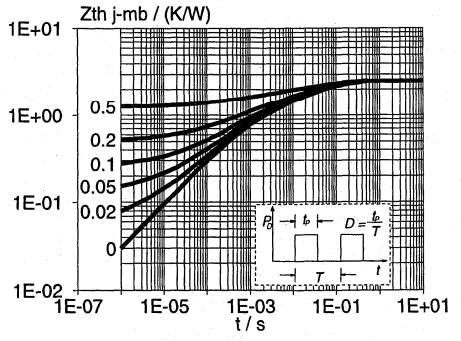


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

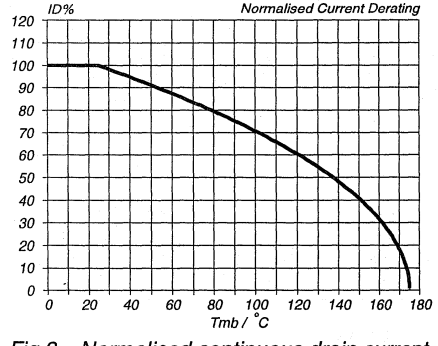


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

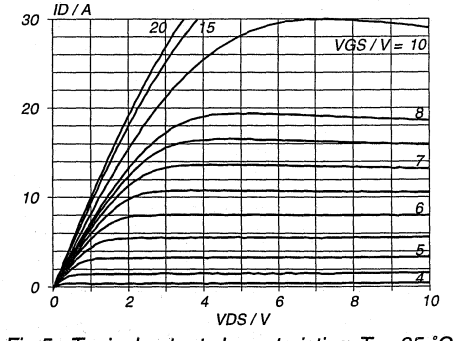


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

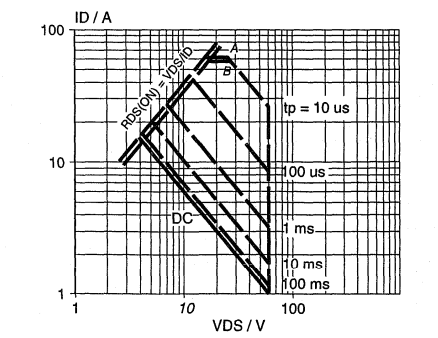


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

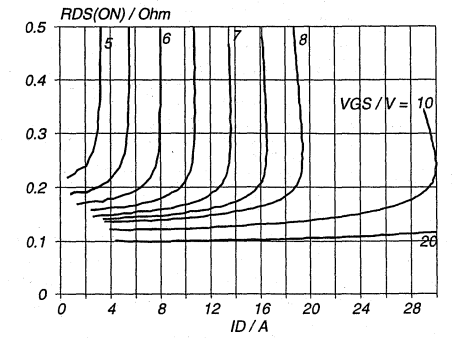


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

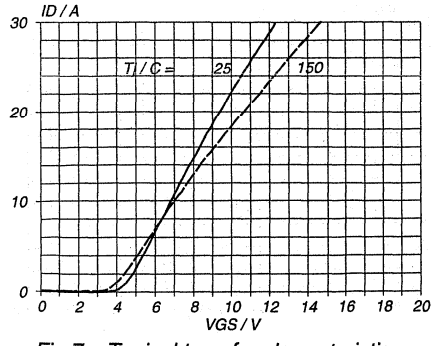


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

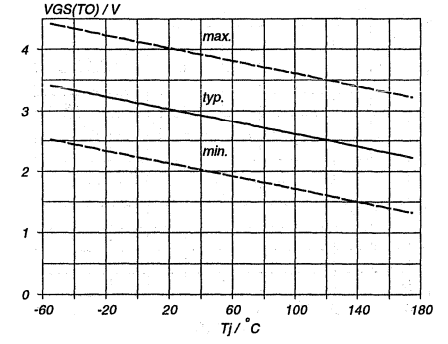


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

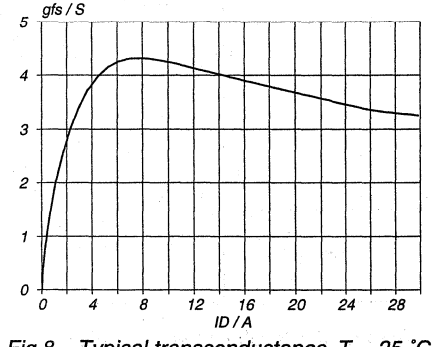


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

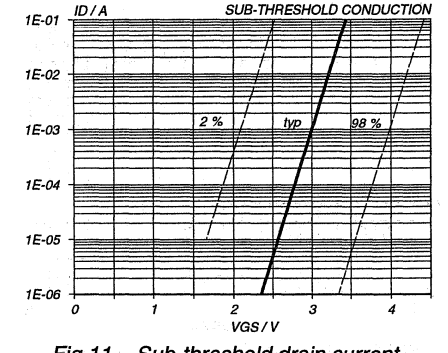


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

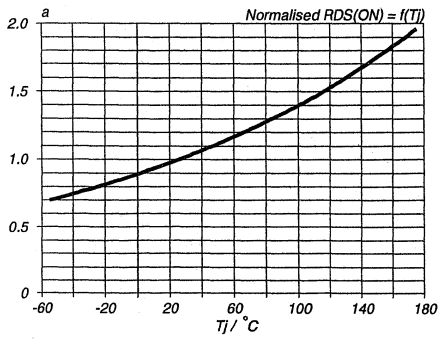


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 8.5 A; V_{GS} = 10 V

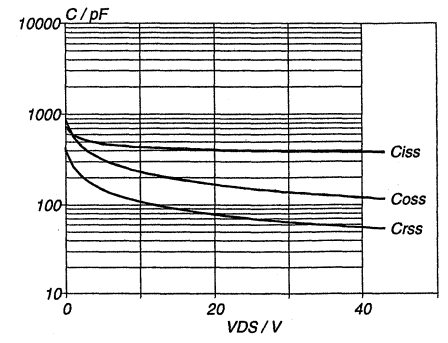


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

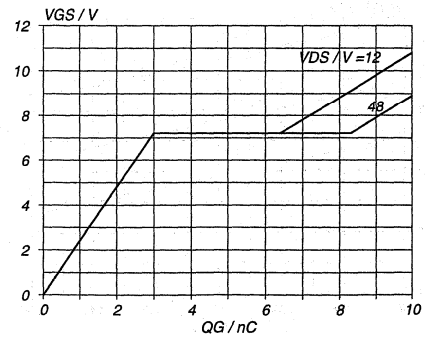


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 15$ A; parameter V_{DS}

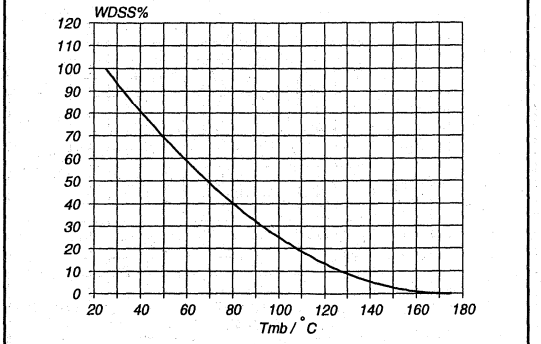


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 15$ A

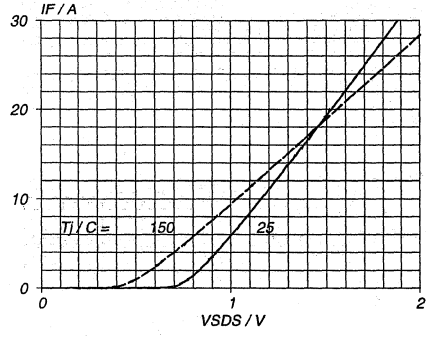


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

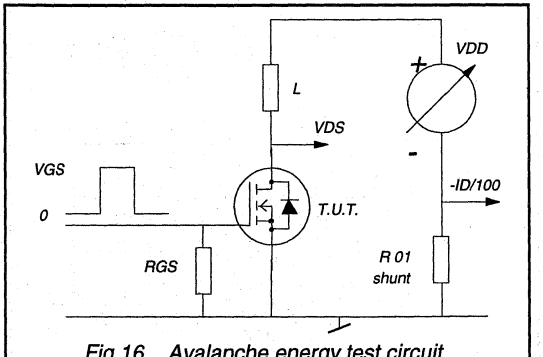


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor PHP18N20E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

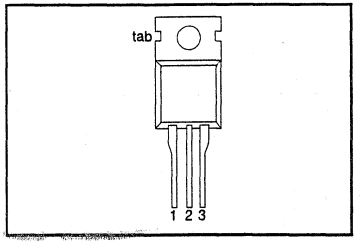
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	18	A
P_{tot}	Total power dissipation	136	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.18	Ω

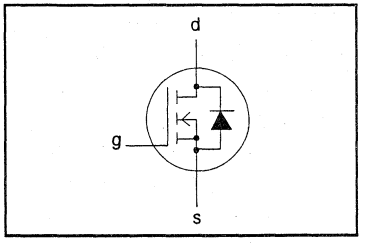
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	18	A
		T_{mb} = 100 °C	-	12.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	72	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	18	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	72	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature		-55	175	°C
T_j	Junction temperature		-	175	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 18 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_j = 25°C prior to surge	-	100	mJ

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1.0	10	µA
		V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 11 A	-	0.16	0.18	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 18 A ;V_{GS} = 0 V	-	1.0	1.6	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 11 A	6.7	8.4	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1450	1850	pF
C_{oss}	Output capacitance		-	245	325	pF
C_{rss}	Feedback capacitance		-	45	90	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_d = 18 A; V_{DS} = 160 V	-	40	-	nC
Q_{gs}	Gate to source charge		-	7	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	20	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	18	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	85	120	ns
t_f	Turn-off fall time		-	35	50	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 18 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	2.0	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor PHP1N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

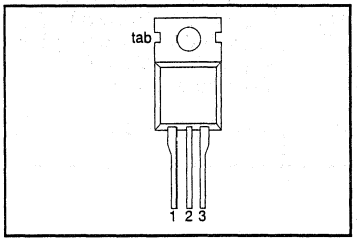
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	2	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	5	Ω

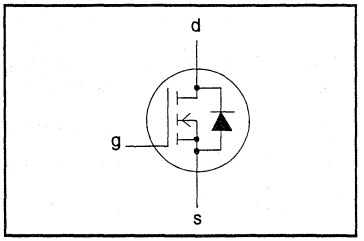
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	2.0	A
		T_{mb} = 100 °C	-	1.3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	8.0	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	2.0	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	8.0	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	50	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	120	mJ
		T_j = 100°C prior to surge	-	20	mJ
W_{DSR} [1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \leq$ 150 °C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1 A	-	4.5	5.0	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2 A ;V_{GS} = 0 V	-	0.8	1.2	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1 A	0.5	0.9	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	230	300	pF
C_{oss}	Output capacitance		-	35	50	pF
C_{rss}	Feedback capacitance		-	14	30	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 2 A; V_{DS} = 400 V	-	10	-	nC
Q_{gs}	Gate to source charge		-	1	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	5	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	45	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	40	ns
t_f	Turn-off fall time		-	20	30	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	2.5	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

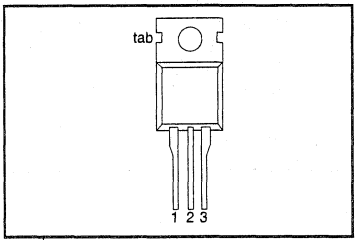
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	1.9	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	6	Ω

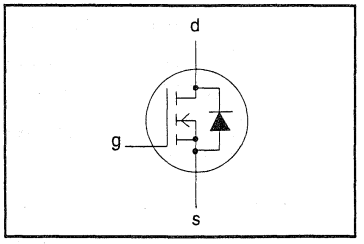
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	1.9	A
		T_{mb} = 100 °C	-	1.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	7.6	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	1.9	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	7.6	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	50	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.9 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	120	mJ
		T_j = 100°C prior to surge	-	20	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 1.9 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.9 A	-	5.3	6	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 1.9 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 0.9 A	0.5	0.8	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	224	310	pF
C_{oss}	Output capacitance		-	27	40	pF
C_{rss}	Feedback capacitance		-	6	10	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 1.9 A; V_{DS} = 480 V	-	10	-	nC
Q_{gs}	Gate to source charge		-	1	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	5	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1.9 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	45	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	40	ns
t_f	Turn-off fall time		-	20	30	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 1.9 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	3.5	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

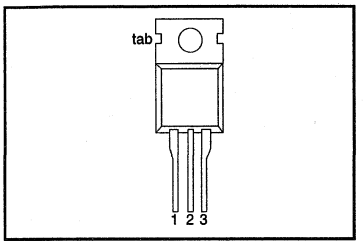
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	22	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	Ω

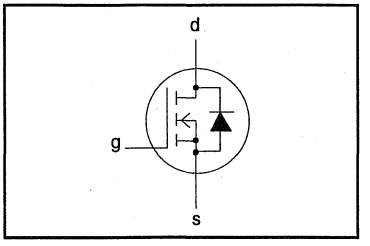
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	22	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	15	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	88	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	0.07	0.08	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	4.5	6.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	120	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	55	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	22	A
I_{DRM}	Pulsed reverse drain current	-	-	-	88	A
V_{SD}	Diode forward voltage	I_F = 22 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 22 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.25	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 22 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

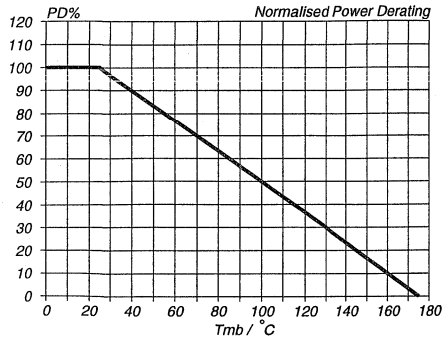


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\ 25\ °C} = f(T_{mb})$

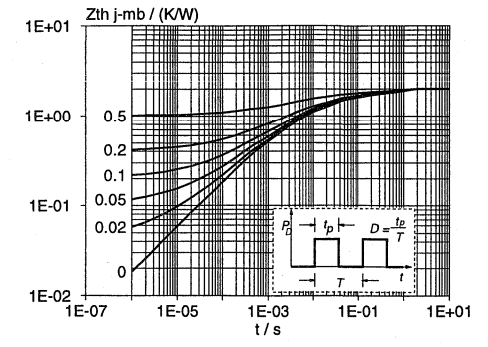


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

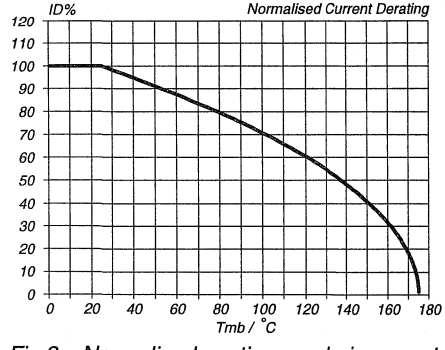


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\ 25\ °C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

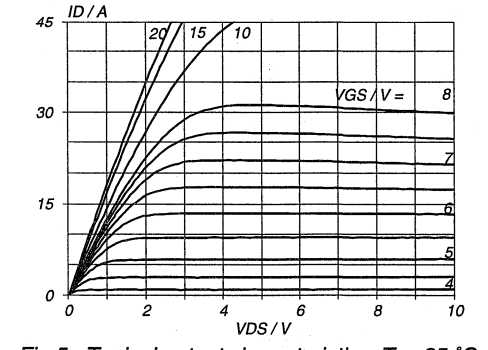


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

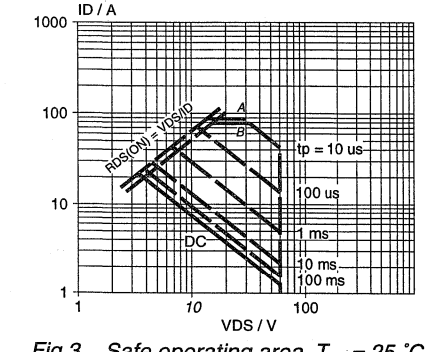


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

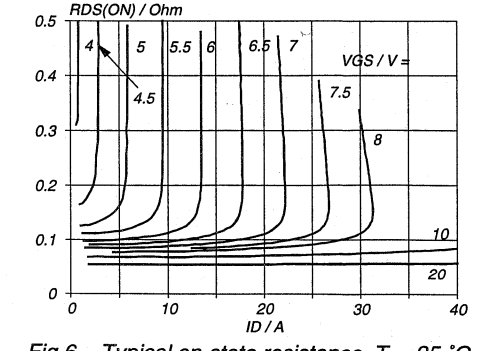


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

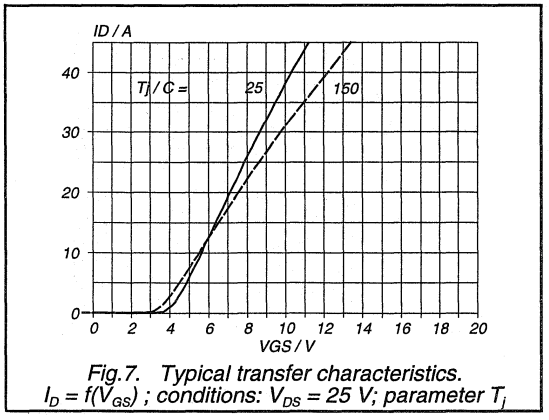


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

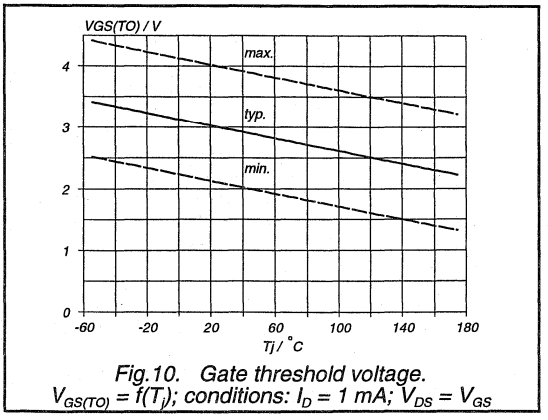


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

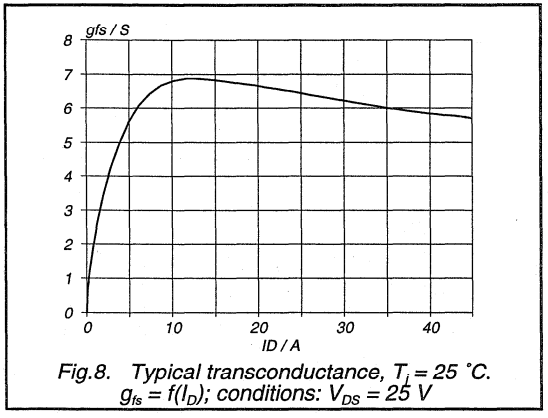


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

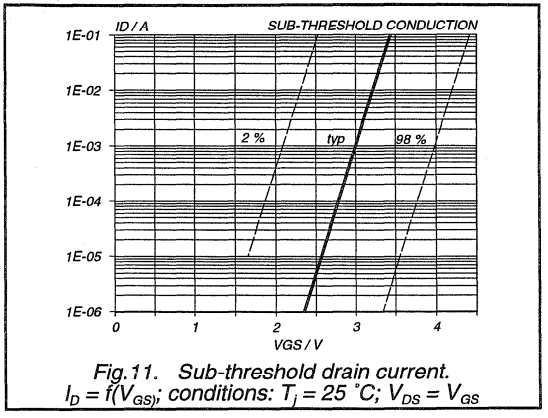


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

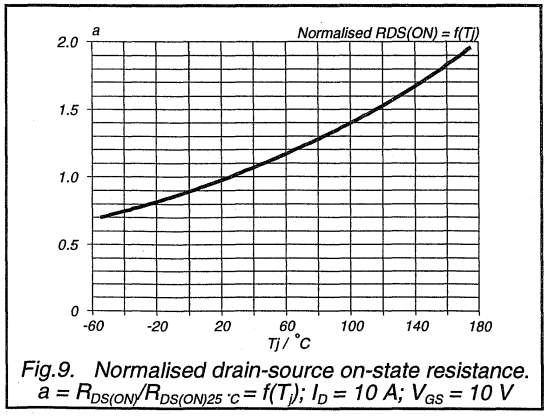


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 10$ A; $V_{GS} = 10$ V

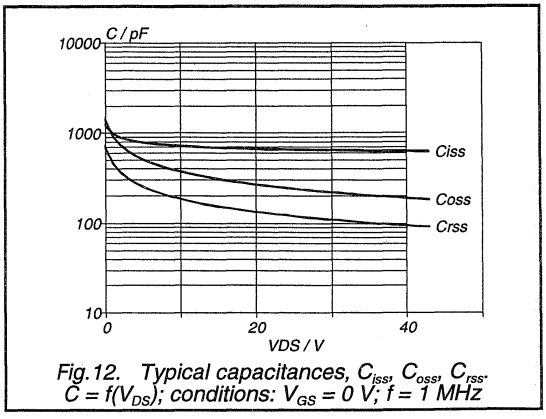


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

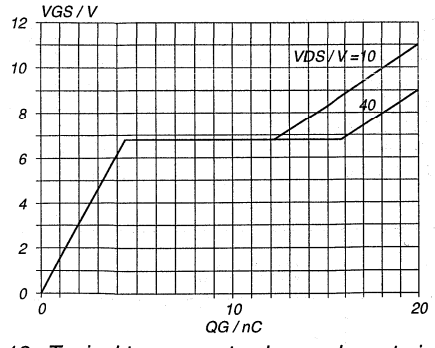


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 22$ A; parameter V_{DS}

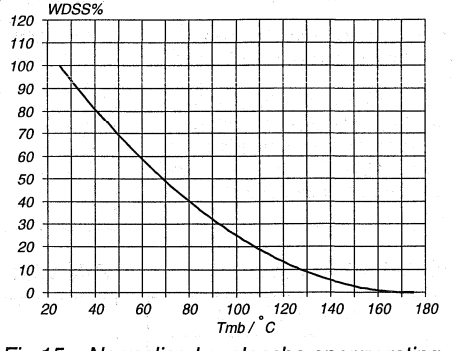


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 22$ A

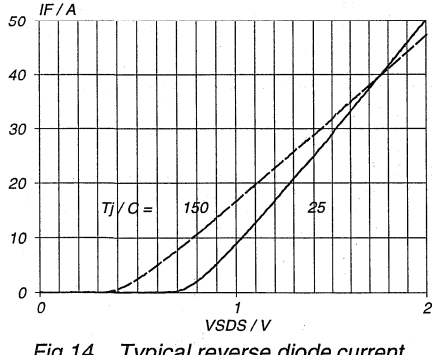


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

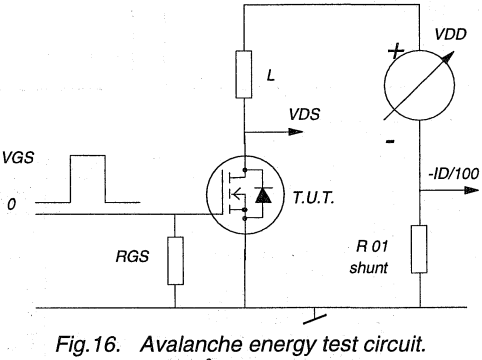


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PowerMOS transistor — PHP26N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

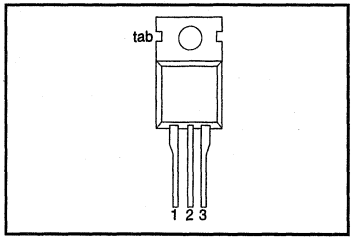
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	26	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	Ω

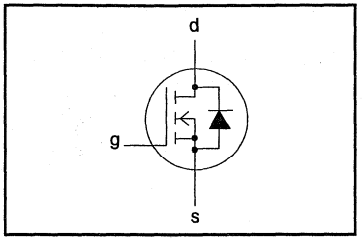
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	26	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	18	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	104	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 13 A	-	0.07	0.08	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	7.0	13.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1650	2000	pF
C_{oss}	Output capacitance		-	350	500	pF
C_{rss}	Feedback capacitance		-	100	150	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	100	160	ns
t_f	Turn-off fall time		-	50	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	26	A
I_{DRM}	Pulsed reverse drain current	-	-	-	104	A
V_{SD}	Diode forward voltage	I_F = 26 A ; V_{GS} = 0 V	-	1.3	1.7	V
t_{rr}	Reverse recovery time	I_F = 26 A; -dI_F/dt = 100 A/µs;	-	90	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.8	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 26 A ; V_{DD} ≤ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

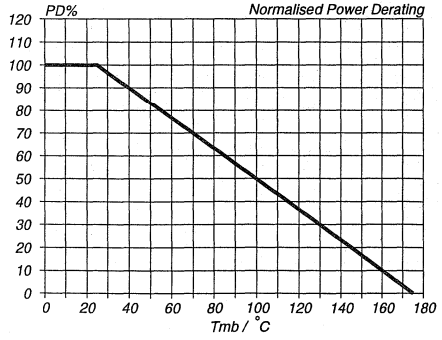


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

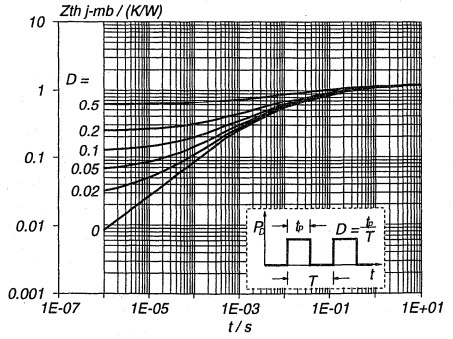


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

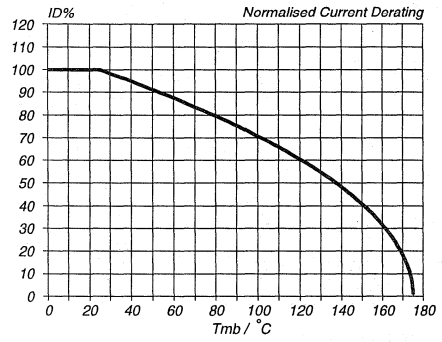


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

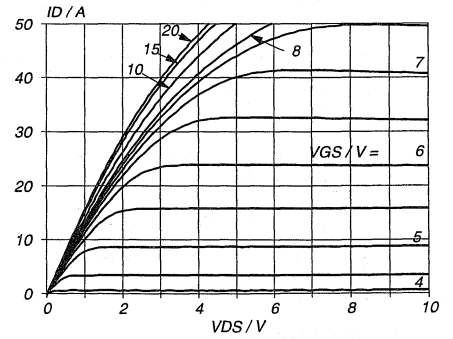


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

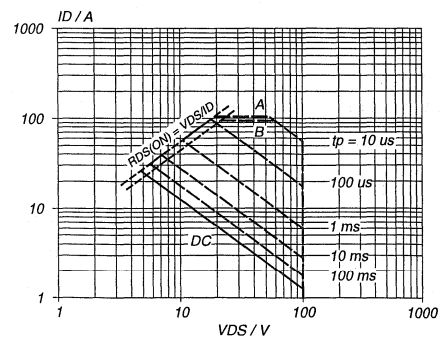


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

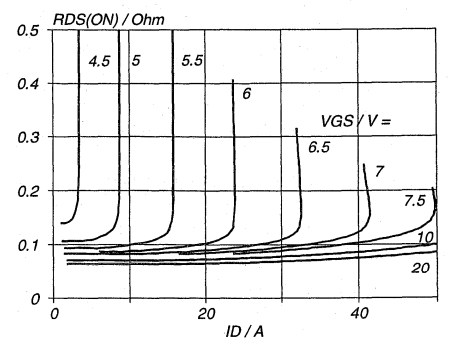


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

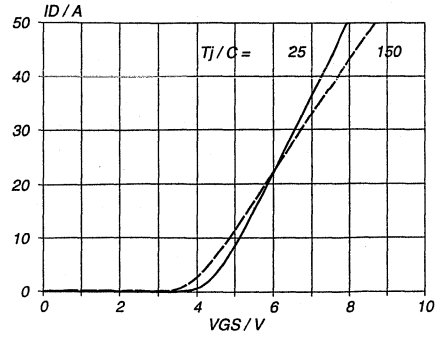


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

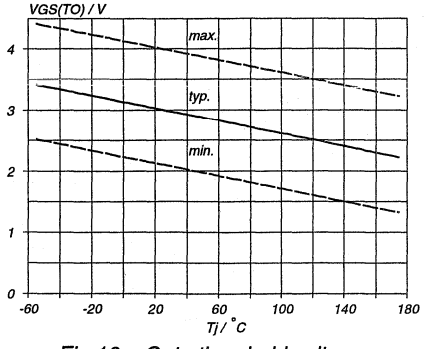


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

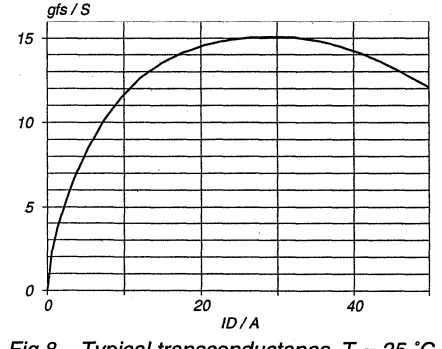


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

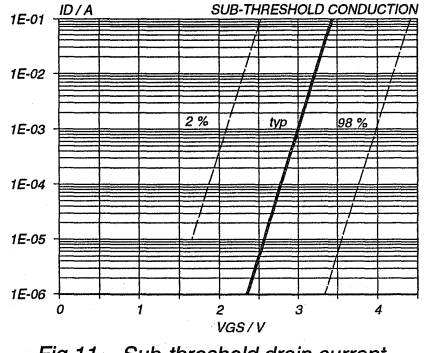


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

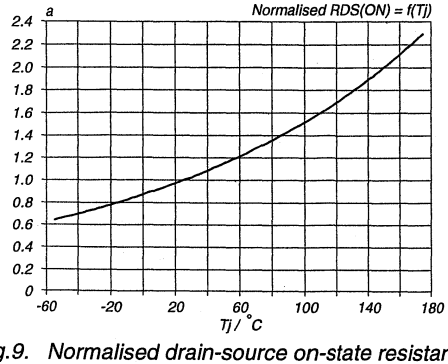


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 13 A; V_{GS} = 10 V

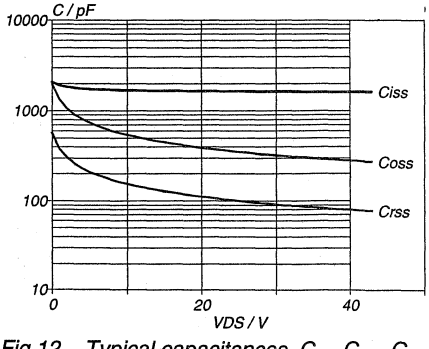


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

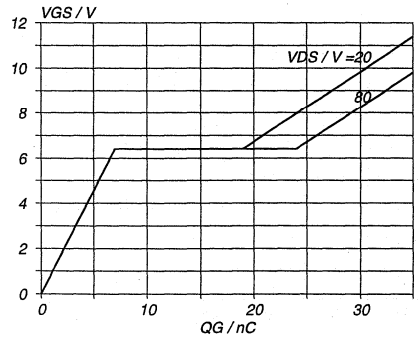


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 26$ A; parameter V_{DS}

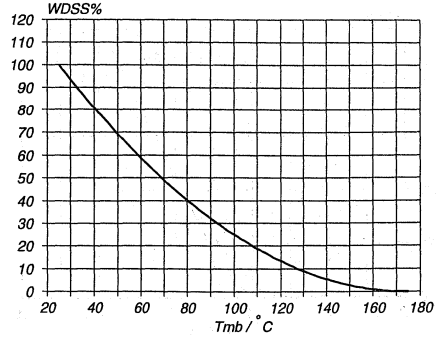


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 26$ A

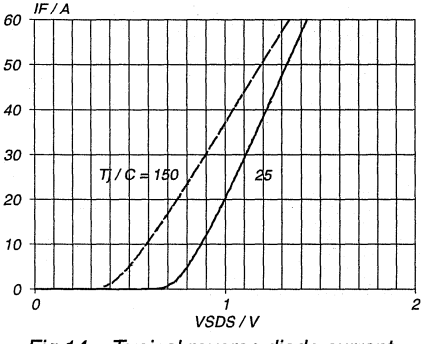


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

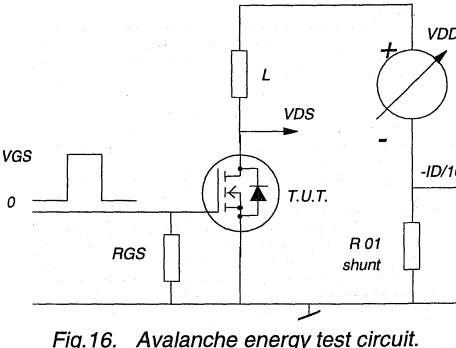


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

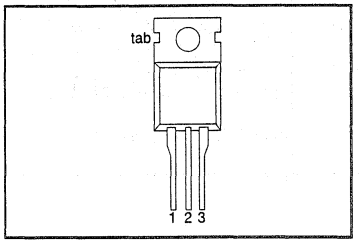
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	2.5	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	3.5	Ω

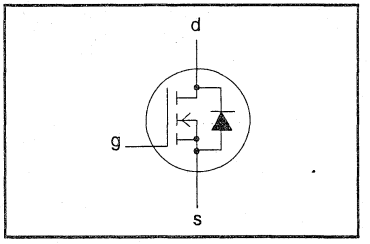
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	2.5	A
		T_{mb} = 100 °C	-	1.6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	10	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	2.5	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	10	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	50	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.5 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	120	mJ
		T_j = 100°C prior to surge	-	20	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 2.5 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS}= 50 Ω ; $T_j \leq$ 150 °C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.25 A	-	3.1	3.5	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2.5 A ;V_{GS} = 0 V	-	1.4	2.0	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1.25 A	0.5	0.9	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	225	315	pF
C_{oss}	Output capacitance		-	30	42	pF
C_{rss}	Feedback capacitance		-	6.0	12	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 2.5 A; V_{DS} = 320 V	-	12	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	6	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.2 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	45	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	40	ns
t_f	Turn-off fall time		-	20	30	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 2.5 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	2.5	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

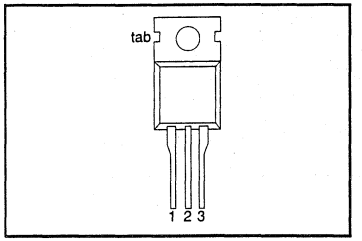
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	2.6	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	4.4	Ω

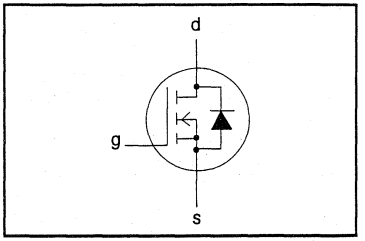
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	2.6	A
		T_{mb} = 100 °C	-	1.7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	10	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	2.6	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	10	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.6 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	190	mJ
		T_j = 100°C prior to surge	-	35	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 2.6 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.3 A	-	4.0	4.4	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2.6 A ;V_{GS} = 0 V	-	1.1	1.6	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1.3 A	1.0	2.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	600	pF
C_{oss}	Output capacitance		-	50	60	pF
C_{rss}	Feedback capacitance		-	30	55	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 2.6 A; V_{DS} = 480 V	-	18	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	7.5	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.1 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	40	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
t_{rr}	Source-drain diode Reverse recovery time	I_F = 2.6 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	3.5	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor | PHP3055E

GENERAL DESCRIPTION

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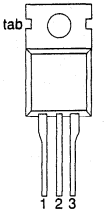
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	12	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.15	Ω

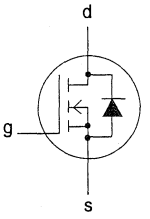
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	12	A
		T_{mb} = 100 °C	-	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	26	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	12	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	26	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40	W
T_{stg}	Storage temperature		-55	175	°C
T_j	Junction temperature		-	175	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 12 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_j = 25°C prior to surge	-	25	mJ

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1.0	10	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6 A	-	-	0.15	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 6 A ;V_{GS} = 0 V	-	1.0	1.5	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 6 A	4	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	345	-	pF
C_{oss}	Output capacitance		-	130	-	pF
C_{rss}	Feedback capacitance		-	60	-	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_d = 12 A; V_{DS} = 48 V	-	12	-	nC
Q_{gs}	Gate to source charge		-	6.5	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	5.5	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 25 V; I_D = 6 A;	-	-	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	-	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	-	65	ns
t_f	Turn-off fall time		-	-	65	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 6 A; -dI_F/dt = 100 A/µs;	-	50	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.15	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Logic level FET

PHP3055L

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

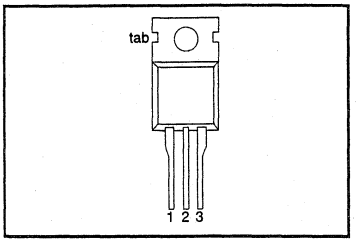
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	12	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 5 V	0.18	Ω

PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



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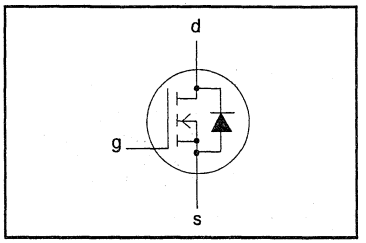


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage		-	15	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	12	A
		T_{mb} = 100 °C	-	9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	26	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	12	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	26	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40	W
T_{stg}	Storage temperature		-55	175	°C
T_j	Junction temperature		-	175	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 12 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_j = 25°C prior to surge	-	25	mJ

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1.0	10	µA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 6 A	-	-	0.18	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 6 A ;V_{GS} = 0 V	-	1.0	1.5	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 6 A	5	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	345	-	pF
C_{oss}	Output capacitance		-	130	-	pF
C_{rss}	Feedback capacitance		-	60	-	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_d = 12 A; V_{DS} = 48 V	-	7	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	8	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 25 V; I_D = 6 A;	-	-	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	-	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	-	65	ns
t_f	Turn-off fall time		-	-	65	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 12 A; -dI_F/dt = 100 A/µs;	-	50	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.15	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

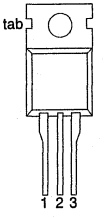
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	34	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.057	Ω

PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



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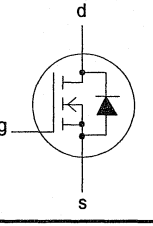


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	34	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	24	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	136	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A	-	0.052	0.057	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	16	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	450	600	pF
C_{rss}	Feedback capacitance		-	130	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω;	-	150	200	ns
t_f	Turn-off fall time	R_{GS} = 50 Ω	-	65	85	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	34	A
I_{DRM}	Pulsed reverse drain current	-	-	-	136	A
V_{SD}	Diode forward voltage	I_F = 34 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	1.0	-	µC

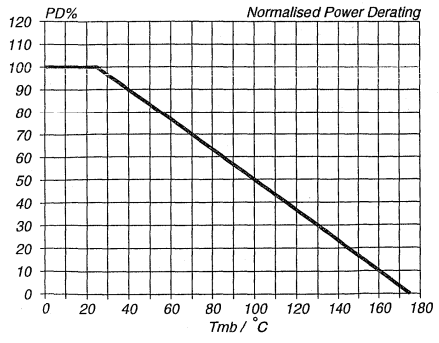


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D / P_{D\,25\,°C} = f(T_{mb})$

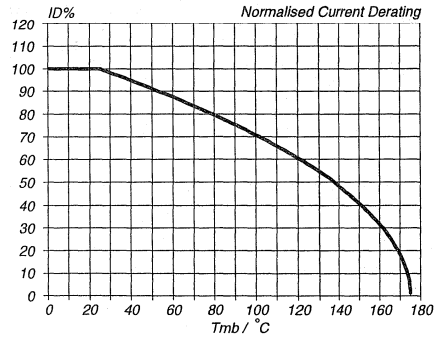


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D / I_{D\,25\,°C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

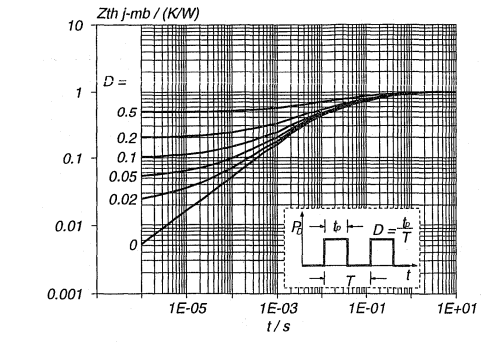


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

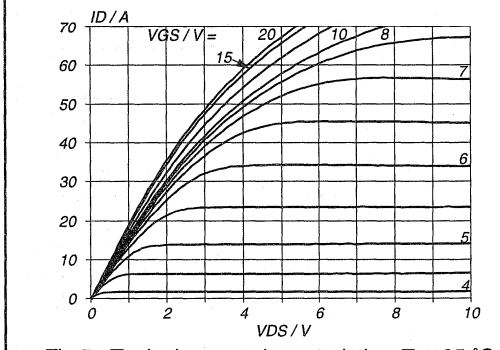


Fig.5. Typical output characteristics, $T_j = 25$ °C.
$I_D = f(V_{DS})$; parameter V_{GS}

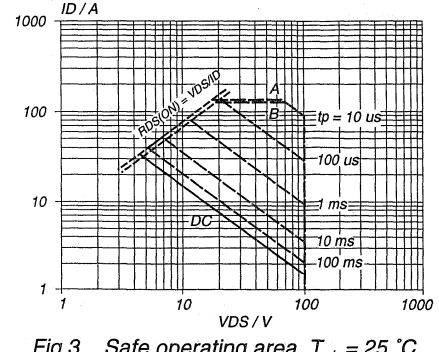


Fig.3. Safe operating area. $T_{mb} = 25$ °C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

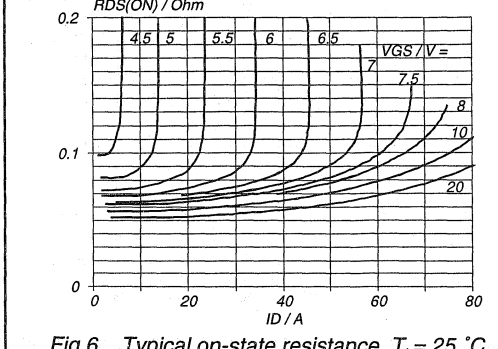


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

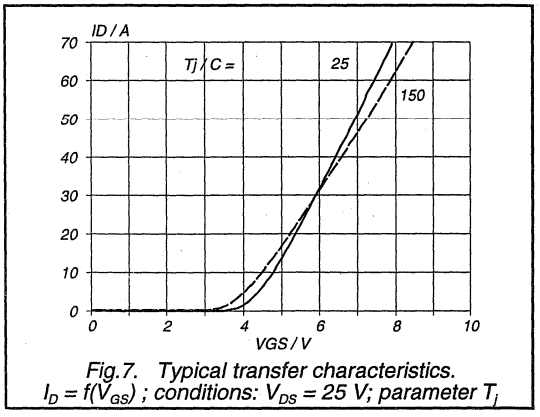


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

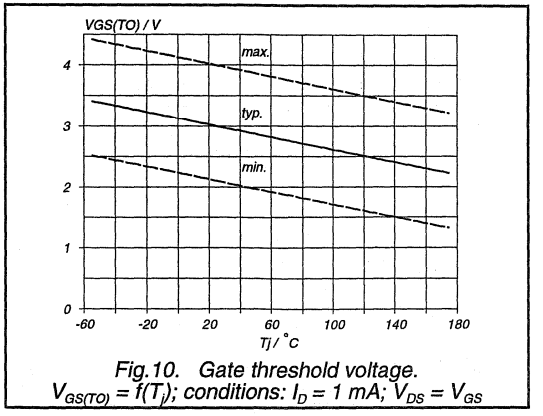


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

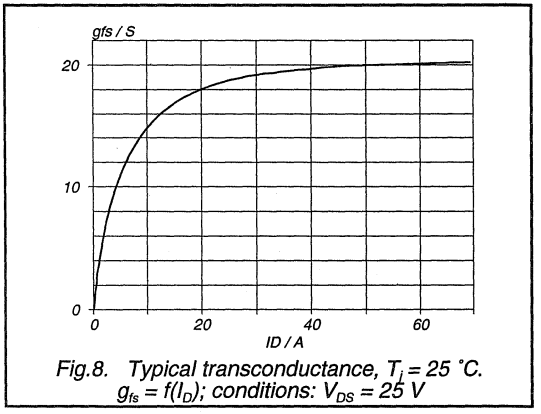


Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

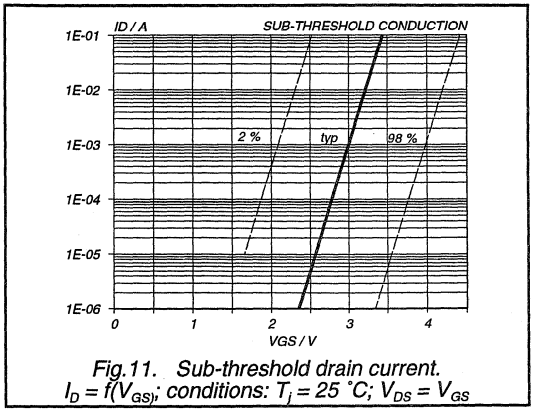


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

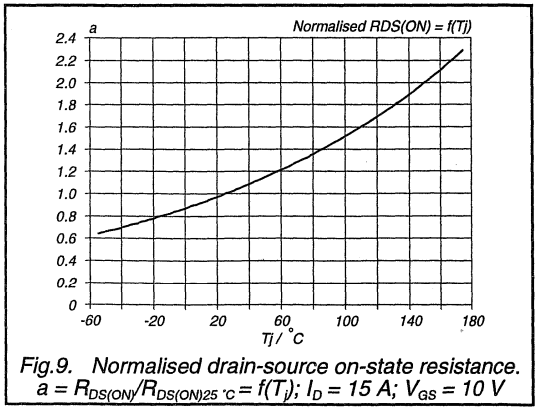


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 15$ A; $V_{GS} = 10$ V

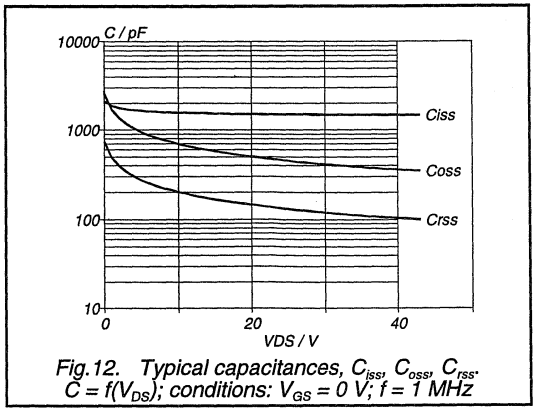


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

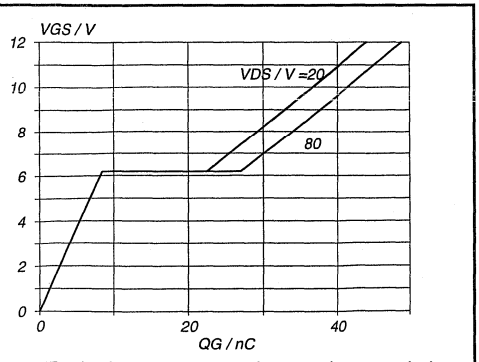


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 34$ A; parameter V_{DS}

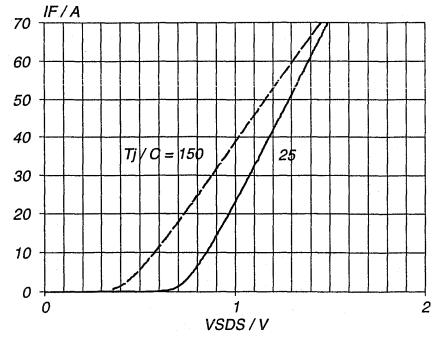


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in automotive applications, Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

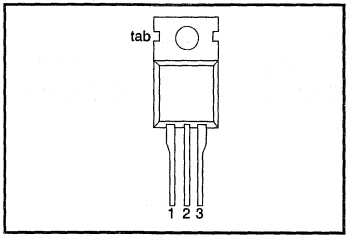
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	41	A
P_{tot}	Total power dissipation	125	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	38	mΩ

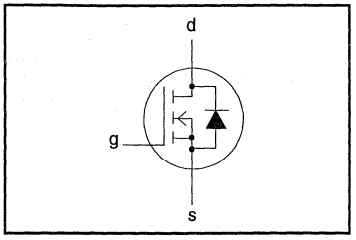
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	41	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	164	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	1.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A	-	30	38	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 20 A	7	14	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	900	1600	pF
C_{oss}	Output capacitance		-	420	600	pF
C_{rss}	Feedback capacitance		-	160	275	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	15	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	55	90	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	75	125	ns
t_f	Turn-off fall time		-	60	100	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	41	A
I_{DRM}	Pulsed reverse drain current	-	-	-	164	A
V_{SD}	Diode forward voltage	I_F = 41 A ; V_{GS} = 0 V	-	0.95	2.0	V
t_{rr}	Reverse recovery time	I_F = 41 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 41 A ; V_{DD} ≤ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	100	mJ

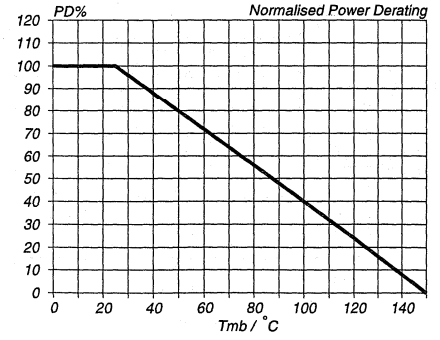


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

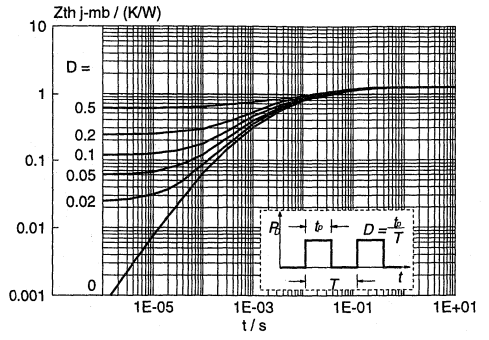


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

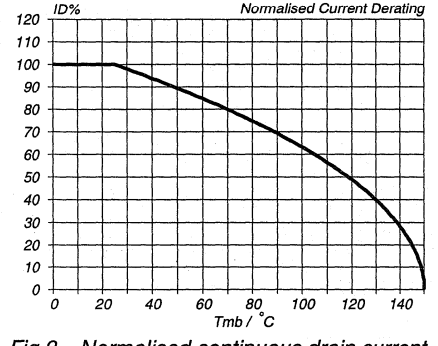


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

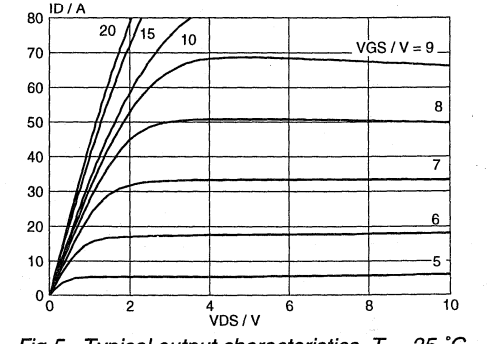


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

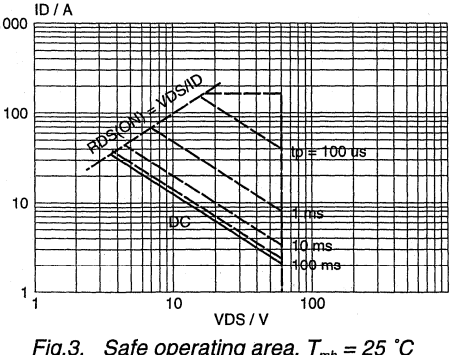


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

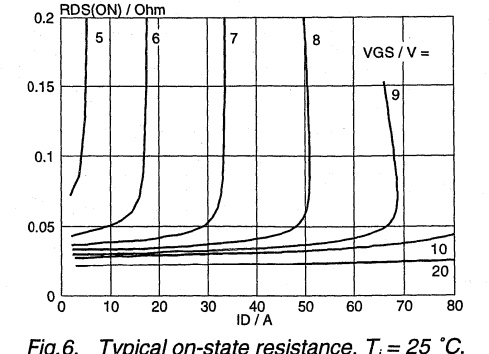


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

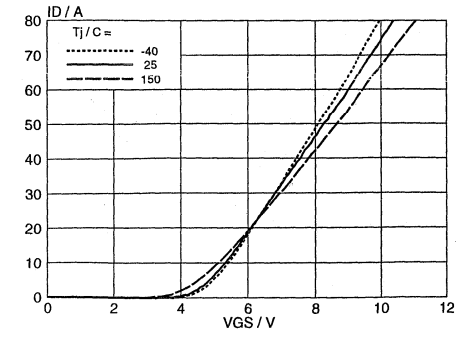


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 15 V; parameter T_j

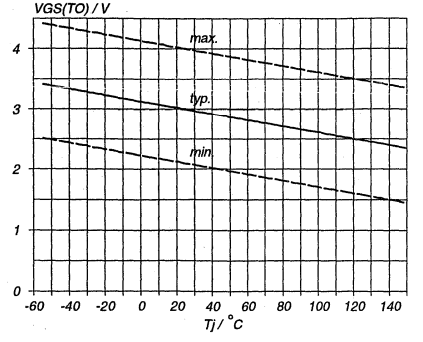


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

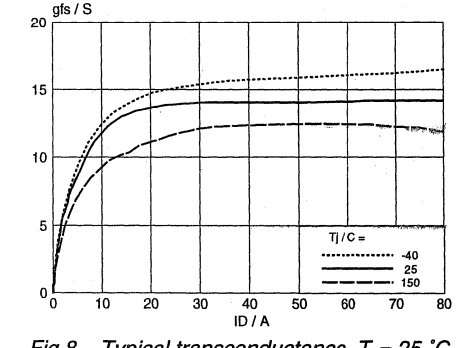


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

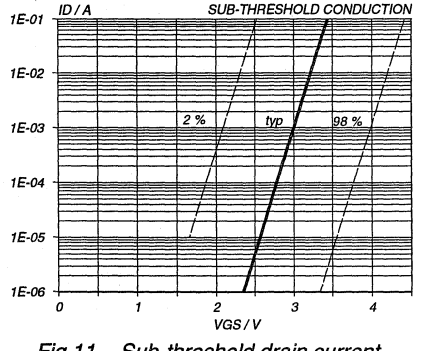


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

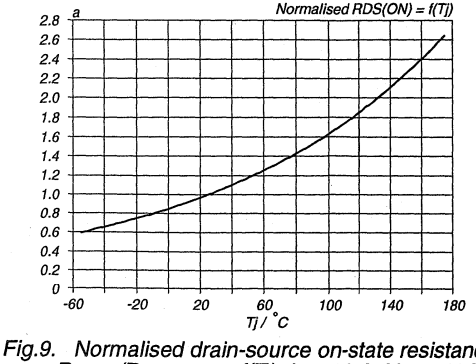


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 20 A; V_{GS} = 10 V

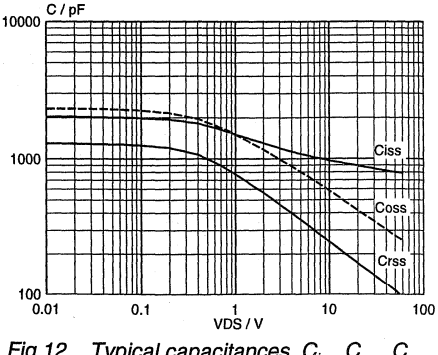


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

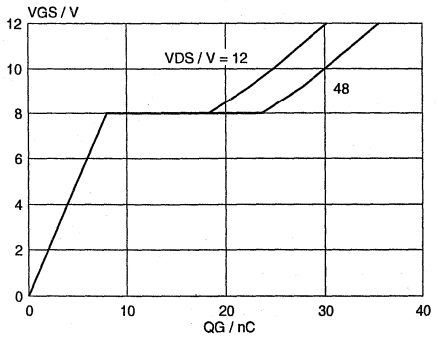


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 41$ A; parameter V_{DS}

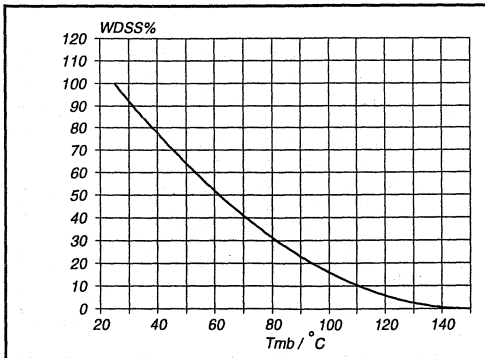


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 41$ A

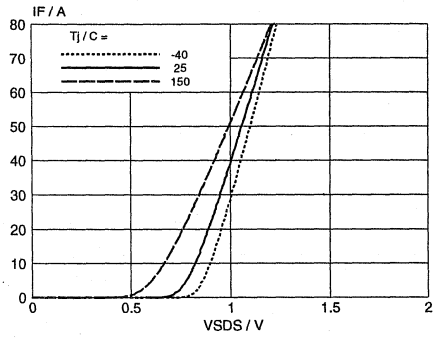


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

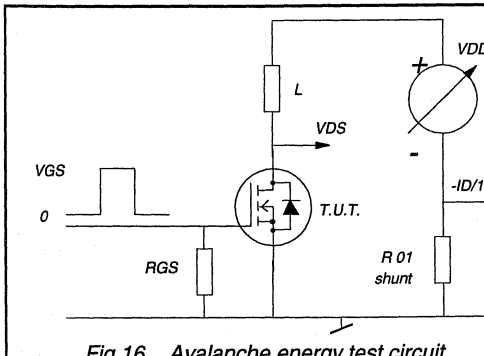


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor — PHP3N20E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

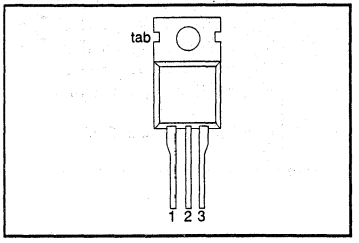
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	3.5	A
P_{tot}	Total power dissipation	20	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	Ω

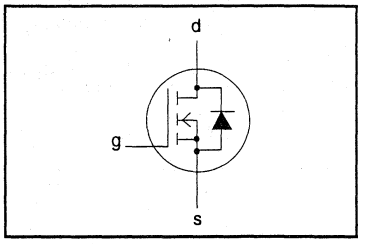
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	3.5	A
		T_{mb} = 100 °C	-	2.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	14	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	3.5	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	14	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	20	W
T_{stg}	Storage temperature		-55	175	°C
T_j	Junction temperature		-	175	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_j = 25°C prior to surge	-	40	mJ

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	3.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1.0	10	µA
		V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.25 A	-	-	1.5	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 3.5 A ;V_{GS} = 0 V	-	1.5	2.0	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1.7 A	0.8	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_d = 3.5 A; V_{DS} = 160 V	-	-	8	nC
Q_{gs}	Gate to source charge		-	-	2	nC
Q_{gd}	Gate to drain (Miller) charge		-	-	4	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 100 V; I_D = 1.7 A;	-	10	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	-	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	-	ns
t_f	Turn-off fall time		-	20	-	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 3.5 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	0.35	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor PHP3N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

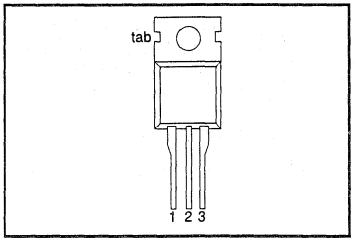
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	3.2	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	3	Ω

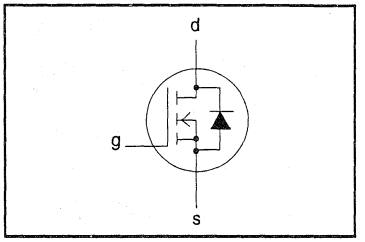
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	3.2	A
		T_{mb} = 100 °C	-	2.0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	13	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	3.2	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	13	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.2 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	210	mJ
		T_j = 100°C prior to surge	-	33	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 3.2 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.6 A	-	2.4	3.0	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 3.2 A ;V_{GS} = 0 V	-	1.1	1.5	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1.6 A	1.0	2.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	55	80	pF
C_{rss}	Feedback capacitance		-	20	55	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 3.2 A; V_{DS} = 400 V	-	20	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	40	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 3.2 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	3.5	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor | PHP3N60E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

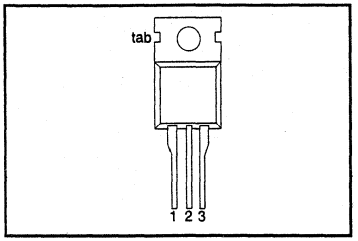
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	4.3	A
P_{tot}	Total power dissipation	100	W
$R_{DS(ON)}$	Drain-source on-state resistance	2.2	Ω

PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



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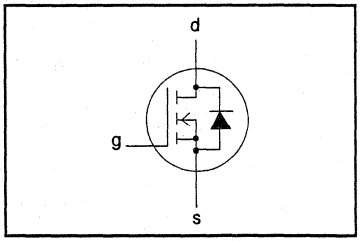


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	4.3	A
		T_{mb} = 100 °C	-	2.7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	17	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	4.3	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	17	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	100	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 4.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	290	mJ
		T_j = 100°C prior to surge	-	46	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 4.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	7.5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.25	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.15 A	-	2.1	2.2	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 4.3 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 2.15 A	1.5	2.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	750	1000	pF
C_{oss}	Output capacitance		-	90	140	pF
C_{rss}	Feedback capacitance		-	40	70	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 4.3 A; V_{DS} = 480 V	-	35	-	nC
Q_{gs}	Gate to source charge		-	8	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	14	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.5 A;	-	10	45	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	100	140	ns
t_f	Turn-off fall time		-	40	65	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 4.3 A; -dI_F/dt = 100 A/µs;	-	1200	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6.0	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor — PHP4N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

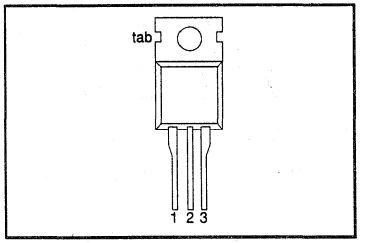
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	4.2	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.8	Ω

PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



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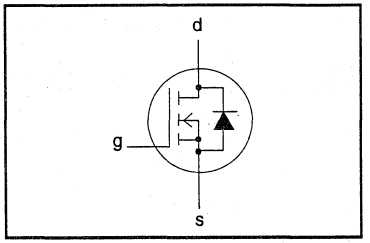


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	4.2	A
		T_{mb} = 100 °C	-	2.6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	17	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	4.2	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	17	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	75	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 4.2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	190	mJ
		T_j = 100°C prior to surge	-	35	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 4.2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \leq$ 150 °C	-	5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.1 A	-	1.5	1.8	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 4.2 A ;V_{GS} = 0 V	-	1.2	1.6	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 2.1 A	1.7	2.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	360	500	pF
C_{oss}	Output capacitance		-	60	80	pF
C_{rss}	Feedback capacitance		-	25	60	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 4.2 A; V_{DS} = 320 V	-	19	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.5 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	40	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 4.2 A; -dI_F/dt = 100 A/µs;	-	300	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	2.5	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor PHP4N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

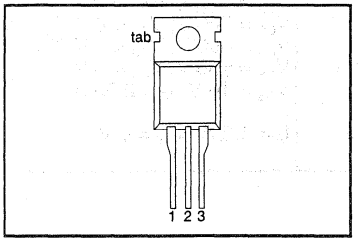
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	5.3	A
P_{tot}	Total power dissipation	100	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	Ω

PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



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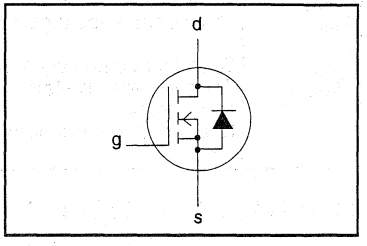


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	5.3	A
		T_{mb} = 100 °C	-	3.3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	21	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	5.3	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	21	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	100	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 5.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	280	mJ
		T_j = 100°C prior to surge	-	44	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 5.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	7.4	mJ

Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.25	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.65 A	-	1.3	1.5	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 5.3 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 2.65 A	1.5	2.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	750	1000	pF
C_{oss}	Output capacitance		-	90	140	pF
C_{rss}	Feedback capacitance		-	40	70	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 5.3 A; V_{DS} = 400 V	-	35	-	nC
Q_{gs}	Gate to source charge		-	4	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	16	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.6 A;	-	10	45	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	100	140	ns
t_f	Turn-off fall time		-	40	65	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 5.3 A; -dI_F/dt = 100 A/µs;	-	1200	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

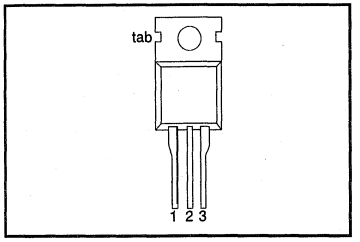
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.028	Ω

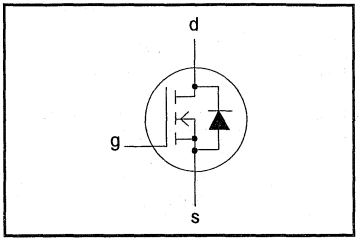
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	36	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 29 A	-	0.024	0.028	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 29 A	17	22	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C_{oss}	Output capacitance		-	800	1000	pF
C_{rss}	Feedback capacitance		-	270	400	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	20	30	ns
t_r	Turn-on rise time	V_{GS} = 10 V;	-	70	100	ns
$t_{d\,off}$	Turn-off delay time	R_{GS} = 50 Ω;	-	170	220	ns
t_f	Turn-off fall time	R_{gen} = 50 Ω	-	120	160	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	52	A
I_{DRM}	Pulsed reverse drain current	-	-	-	208	A
V_{SD}	Diode forward voltage	I_F = 52 A ; V_{GS} = 0 V	-	1.8	2.5	V
t_{rr}	Reverse recovery time	I_F = 52 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.4	-	µC

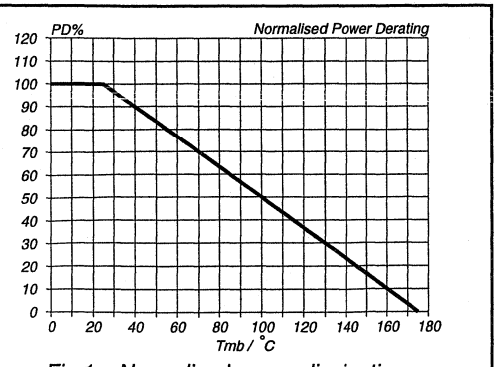


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

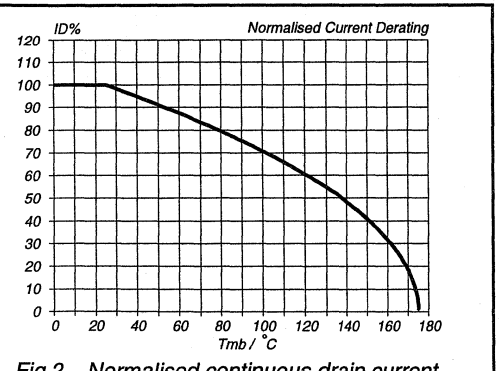


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: $V_{GS} \geq 10$ V

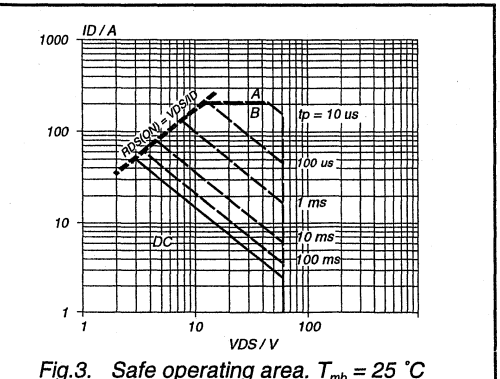


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

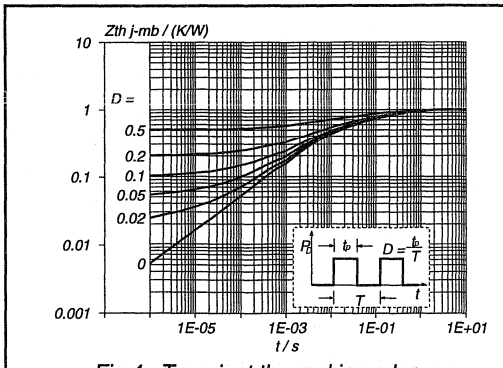


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

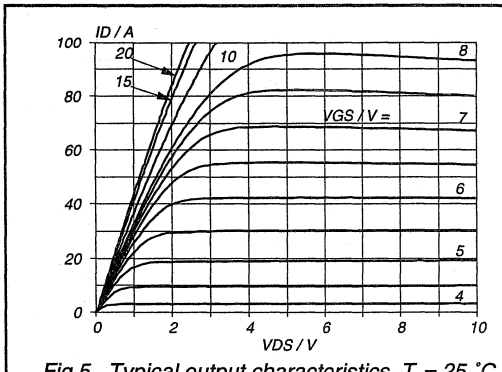


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

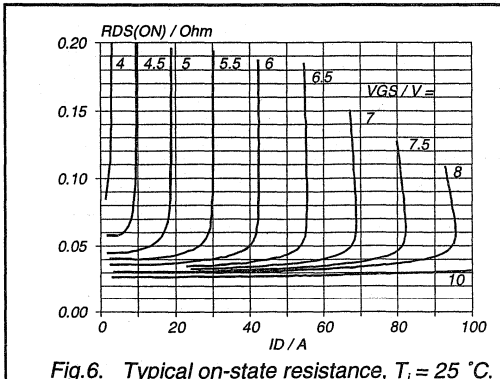


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

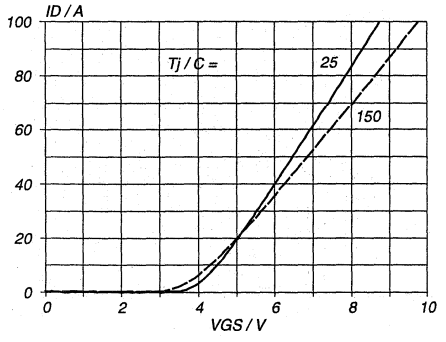


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

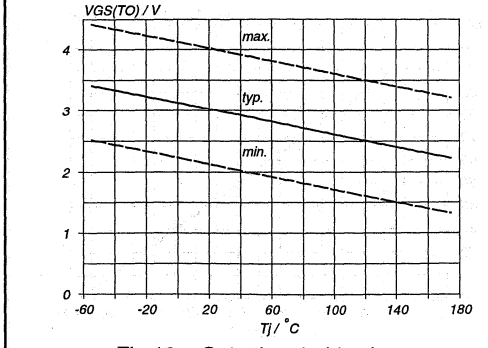


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

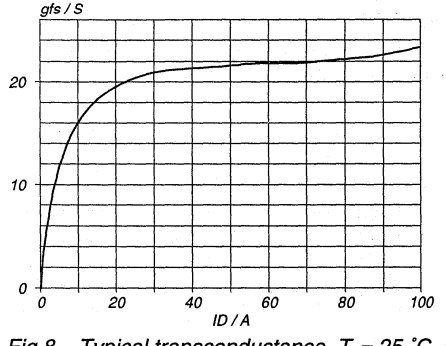


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

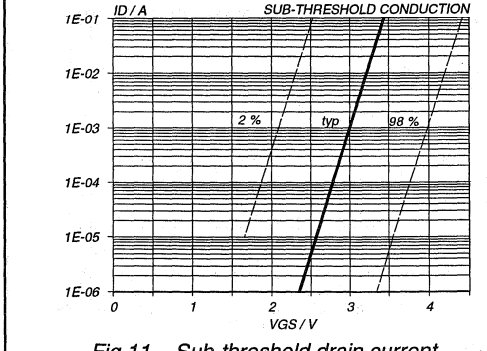


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

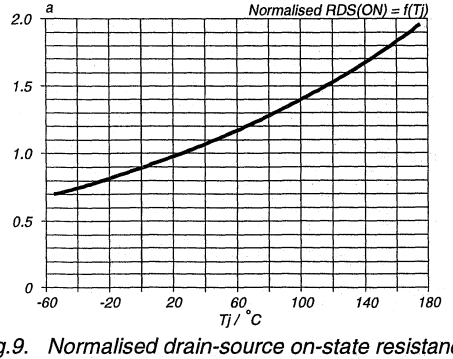


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 29 A; V_{GS} = 10 V

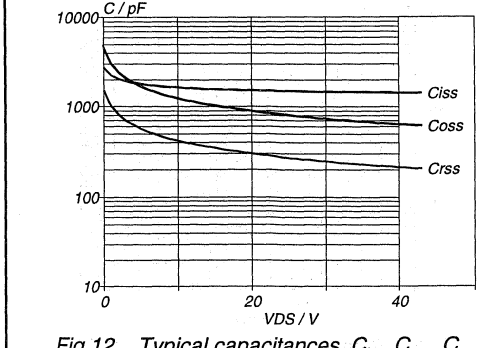


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

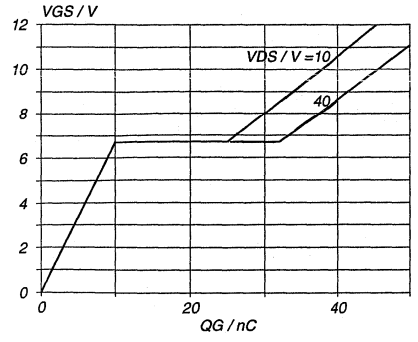


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 52$ A; parameter V_{DS}

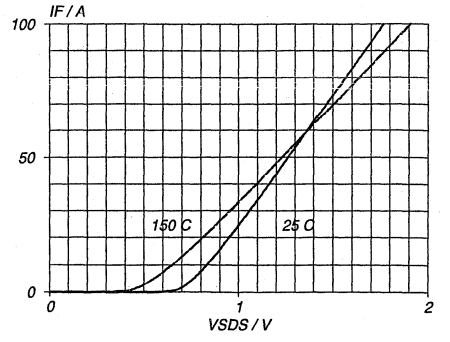


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

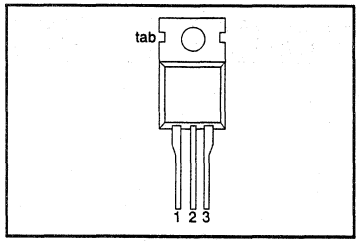
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	5	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.8	Ω

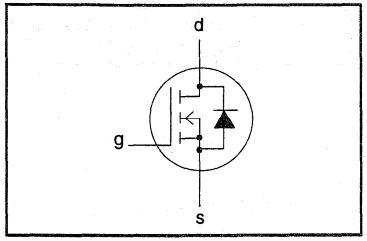
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	5	A
		T_{mb} = 100 °C	-	3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	20	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	5	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	20	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	40	W
T_{stg}	Storage temperature		-55	175	°C
T_j	Junction temperature		-	175	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_j = 25°C prior to surge	-	75	mJ

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1.0	10	µA
		V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.5 A	-	-	0.8	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 5 A ;V_{GS} = 0 V	-	1.5	2	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 4 V; I_D = 2.5 A	1.3	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	350	480	pF
C_{oss}	Output capacitance		-	70	120	pF
C_{rss}	Feedback capacitance		-	35	60	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_d = 5 A; V_{DS} = 160 V	-	11	-	nC
Q_{gs}	Gate to source charge		-	5	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	6	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 100 V; I_D = 2.5 A;	-	-	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	-	60	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	-	100	ns
t_f	Turn-off fall time		-	-	60	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 5 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	0.9	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor — PHP5N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

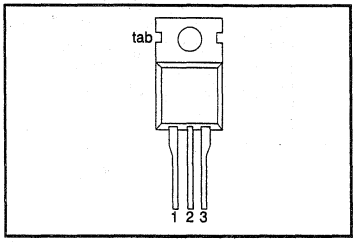
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	6.5	A
P_{tot}	Total power dissipation	100	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.0	Ω

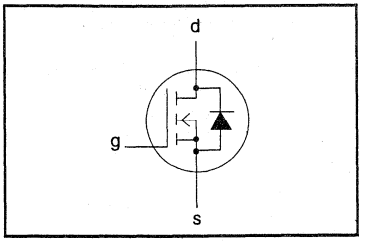
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	6.5	A
		T_{mb} = 100 °C	-	4.1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	26	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	6.5	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	26	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	100	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \le$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	290	mJ
		T_j = 100°C prior to surge	-	46	mJ
W_{DSR} [1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \le$ 50 V; V_{GS} = 10V; R_{GS} = 50 Ω; $T_j \le$ 150 °C	-	7.4	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.25	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.25 A	-	0.8	1.0	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 6.5 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 3.25 A	2.0	3.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	750	1000	pF
C_{oss}	Output capacitance		-	120	180	pF
C_{rss}	Feedback capacitance		-	50	70	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 6.5 A; V_{DS} = 320 V	-	35	-	nC
Q_{gs}	Gate to source charge		-	4	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	18	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.7 A;	-	10	25	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	120	140	ns
t_f	Turn-off fall time		-	40	65	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 6.5 A; -dI_F/dt = 100 A/µs;	-	1200	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6.0	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor — PHP6N60E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

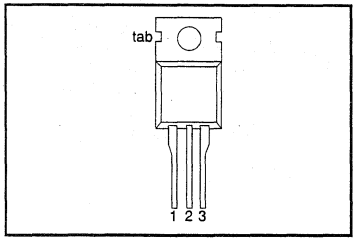
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	6.5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.2	Ω

PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



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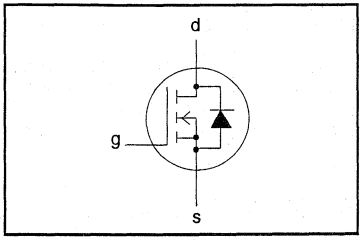


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	6.5	A
		T_{mb} = 100 °C	-	4.1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	26	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	6.5	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	26	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	570	mJ
		T_j = 100°C prior to surge	-	91	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	13	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.25 A	-	0.87	1.2	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 6.5 A ;V_{GS} = 0 V	-	1.1	1.5	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 3.25 A	2.5	5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	1800	pF
C_{oss}	Output capacitance		-	170	270	pF
C_{rss}	Feedback capacitance		-	70	120	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_d = 6.5 A; V_{DS} = 480 V	-	67	-	nC
Q_{gs}	Gate to source charge		-	7	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	33	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.8 A;	-	20	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	200	250	ns
t_f	Turn-off fall time		-	75	90	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 6.5 A; -dI_F/dt = 100 A/µs;	-	500	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

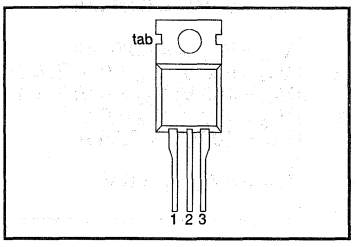
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (DC)	9.2	A
P_{tot}	Total power dissipation	90	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.4	Ω

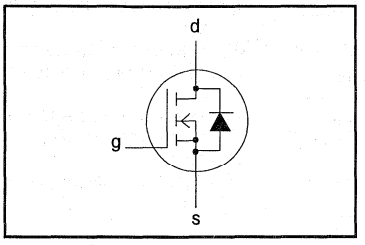
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	200	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	9.2	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	6.5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	90	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.67	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	200	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.5 A	-	0.35	0.4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3.5 A	3.5	5.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	700	850	pF
C_{oss}	Output capacitance		-	100	160	pF
C_{rss}	Feedback capacitance		-	50	80	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.9 A;	-	12	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	70	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	80	120	ns
t_f	Turn-off fall time		-	40	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current	-	-	-	36	A
V_{SD}	Diode forward voltage	I_F = 9.2 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 9.2 A; -dI_F/dt = 100 A/µs;	-	180	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.2	-	µC

AVALANCHE LIMITING VALUE

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 9 A ; $V_{DD} \leq$ 100 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

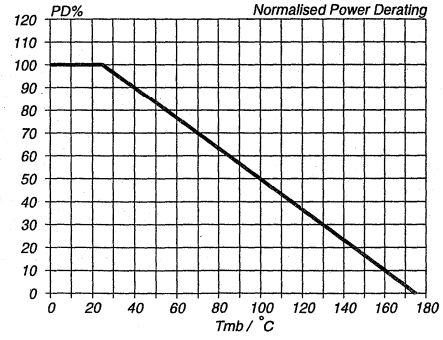


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

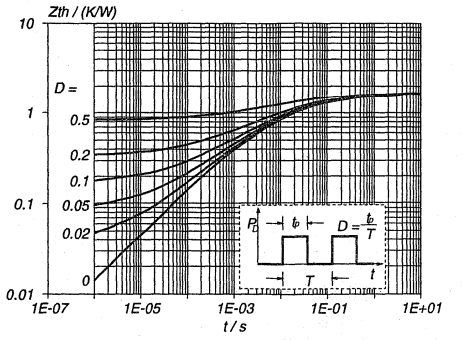


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

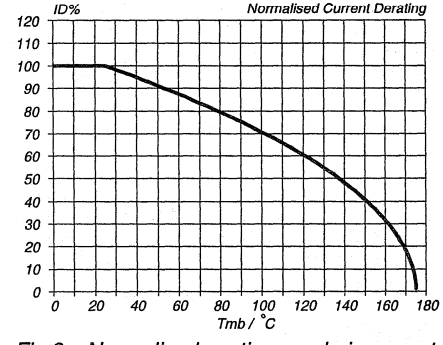


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

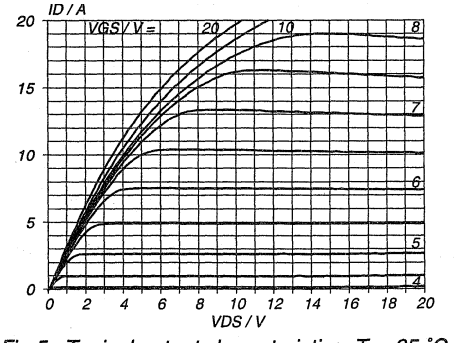


Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

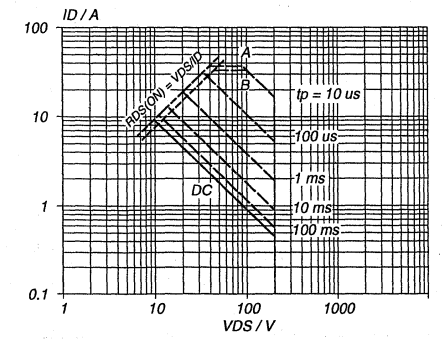


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

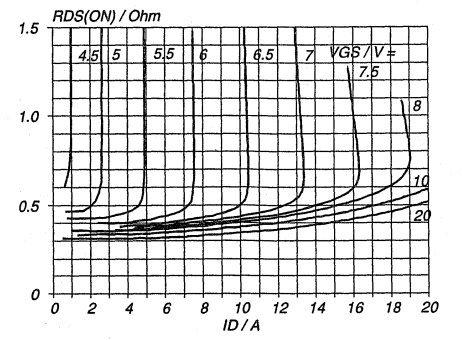


Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

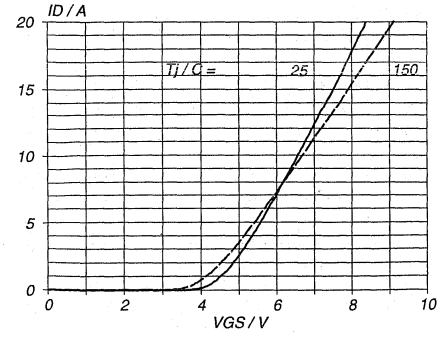


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

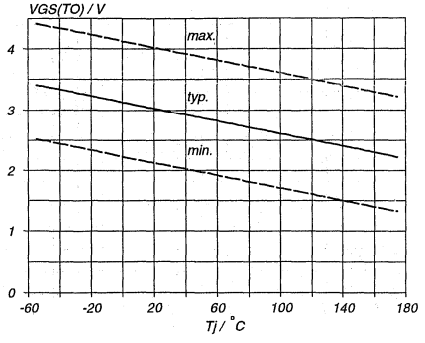


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

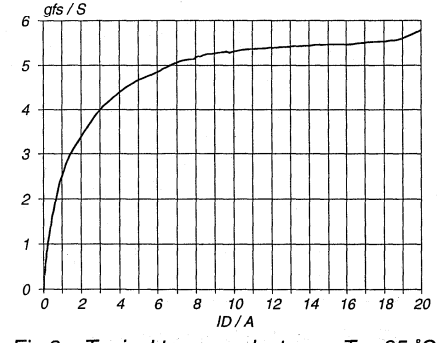


Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

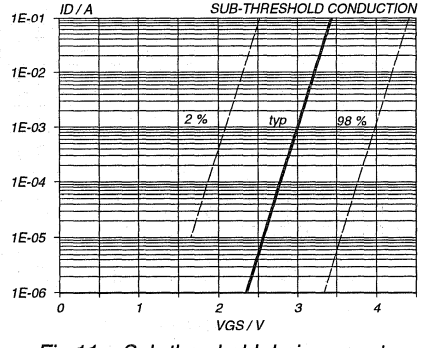


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

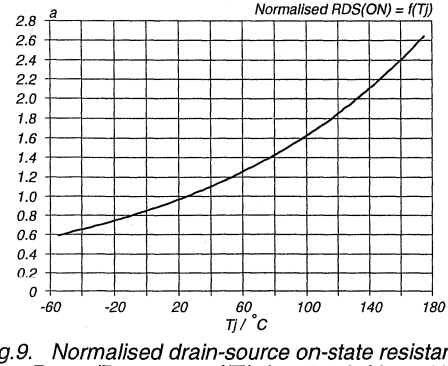


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 3.5 A; V_{GS} = 10 V

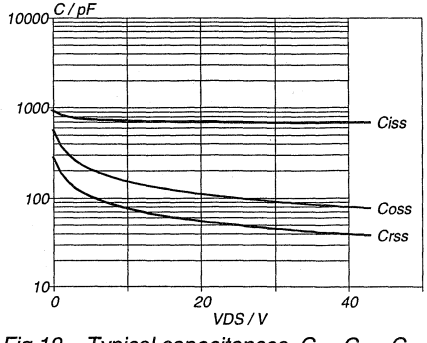


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

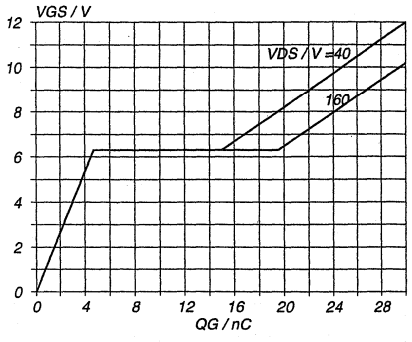


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 9$ A; parameter V_{DS}

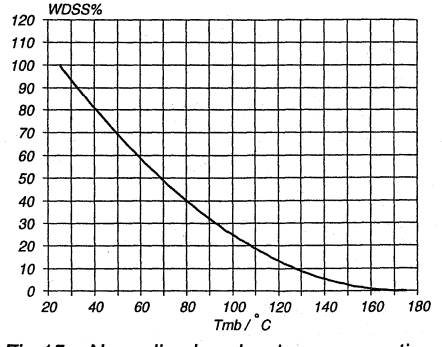


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 9$ A

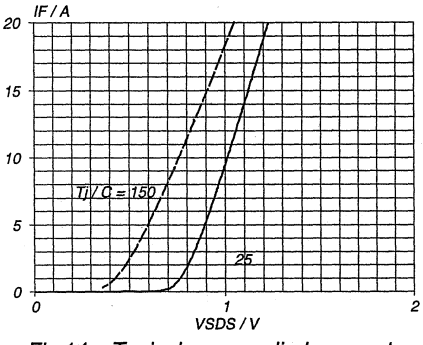


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

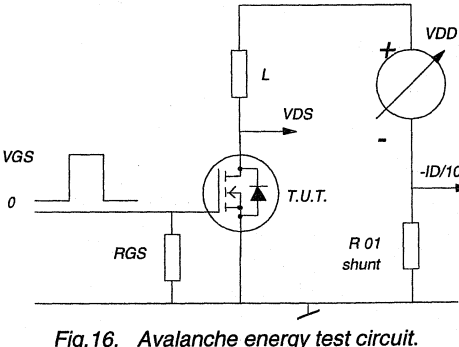


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor | PHP8N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

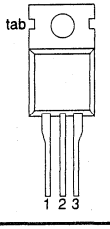
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	8	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.8	Ω

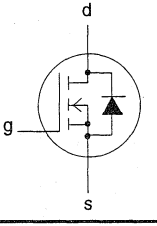
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	8	A
		T_{mb} = 100 °C	-	5.1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	32	A
I_{DR}	Source-drain diode current (DC)	T_{mb} = 25 °C	-	8	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{mb} = 25 °C	-	32	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	125	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 8 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	510	mJ
		T_j = 100°C prior to surge	-	82	mJ
W_{DSR} [1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 8 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	13	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 4 A	-	0.67	0.8	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 8 A ;V_{GS} = 0 V	-	1.4	2.0	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 4 A	4	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	1800	pF
C_{oss}	Output capacitance		-	170	270	pF
C_{rss}	Feedback capacitance		-	70	120	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 8 A; V_{DS} = 400 V	-	65	-	nC
Q_{gs}	Gate to source charge		-	8	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	34	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.8 A;	-	20	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	200	250	ns
t_f	Turn-off fall time		-	75	90	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 8 A; -dI_F/dt = 100 A/µs;	-	500	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6	-	µC
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version of PHP20N06E

PHX15N06E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

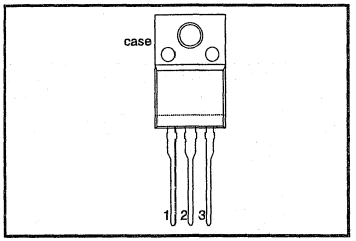
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	13	A
P_{tot}	Total power dissipation	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.08	Ω

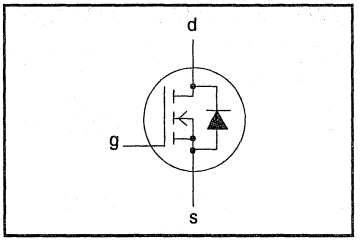
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	13	A
I_D	Drain current (DC)	T_{hs} = 100 °C	-	8.2	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	52	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 9 A	-	0.065	0.08	Ω

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 9 A	4.5	6.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	650	825	pF
C_{oss}	Output capacitance		-	240	350	pF
C_{rss}	Feedback capacitance		-	120	160	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	10	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	35	55	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	60	90	ns
t_f	Turn-off fall time		-	55	80	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	13	A
I_{DRM}	Pulsed reverse drain current	-	-	-	52	A
V_{SD}	Diode forward voltage	I_F = 13 A ; V_{GS} = 0 V	-	1.1	1.3	V
t_{rr}	Reverse recovery time	I_F = 13 A; -dI_F/dt = 100 A/µs;	-	60	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.20	-	µC

AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 22 A ; $V_{DD} \leq$ 25 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω	-	-	50	mJ

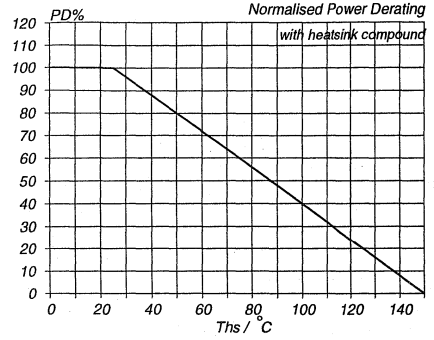


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{hs})

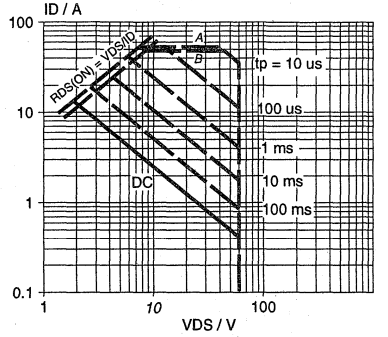


Fig.3. Safe operating area. T_{hs} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

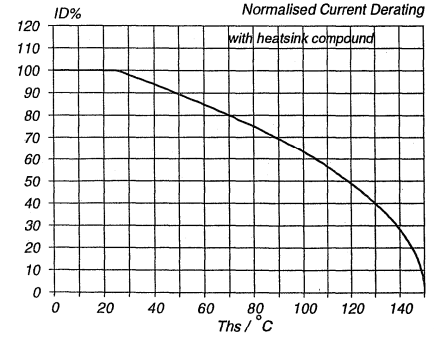


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{hs}); conditions: $V_{GS} \geq$ 10 V

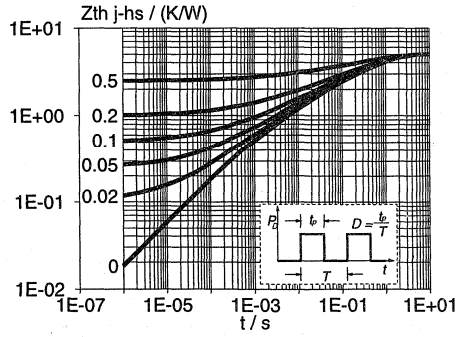


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs}$ = f(t); parameter D = t_p/T

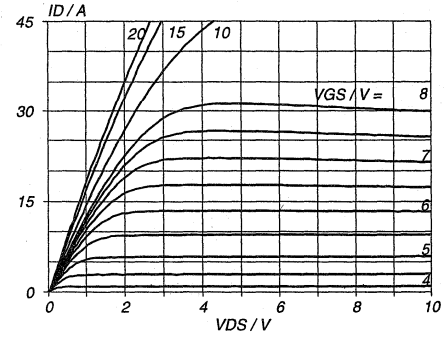


Fig.5. Typical output characteristics, T_j = 25 °C. $I_D = f(V_{DS})$; parameter V_{GS}

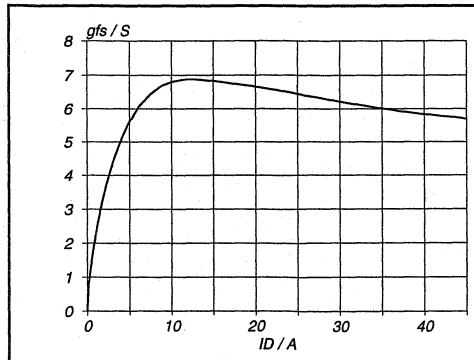


Fig.8. Typical transconductance, T_j = 25 °C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

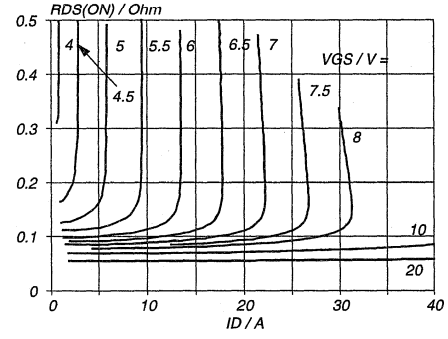


Fig.6. Typical on-state resistance, T_j = 25 °C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

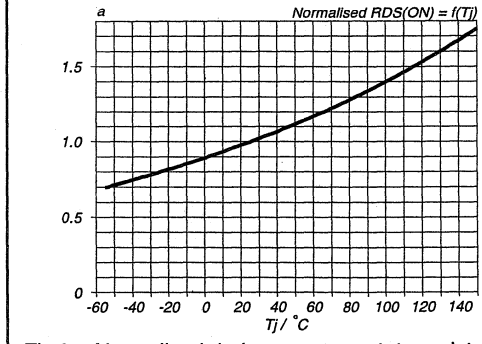


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 9 A; V_{GS} = 10 V

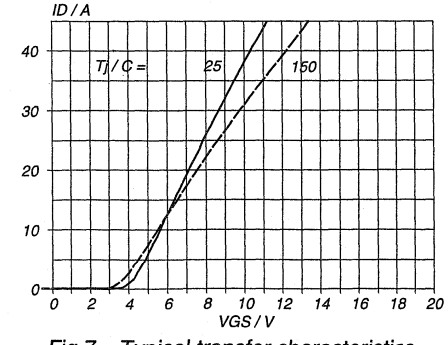


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

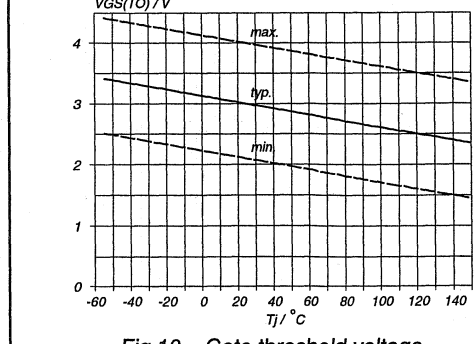


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

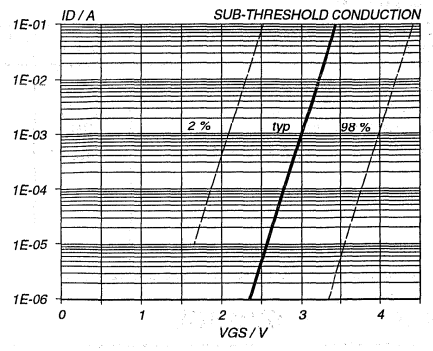


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; *conditions:* $T_j = 25$ °C; $V_{DS} = V_{GS}$

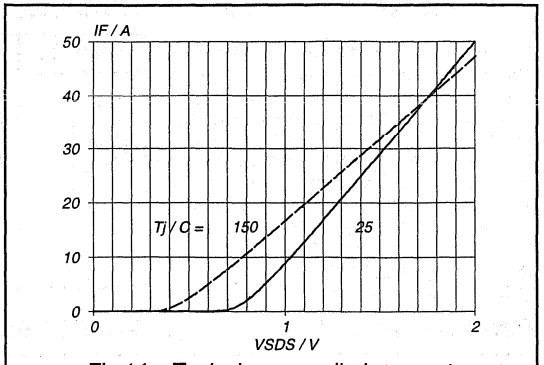


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; *conditions:* $V_{GS} = 0$ V; *parameter* T_j

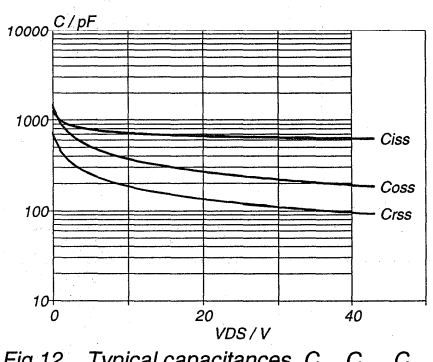


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; *conditions:* $V_{GS} = 0$ V; $f = 1$ MHz

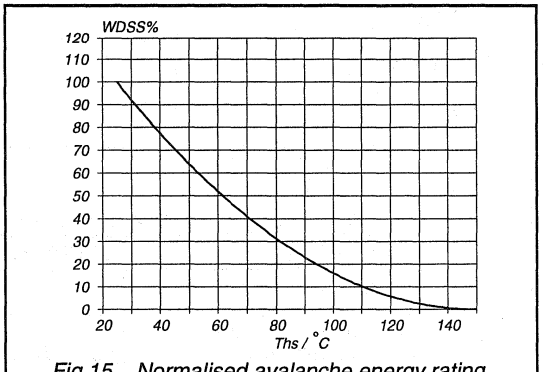


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{hs})$; *conditions:* $I_D = 22$ A

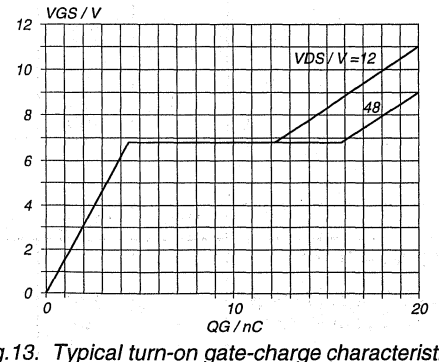


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; *conditions:* $I_D = 22$ A; *parameter* V_{DS}

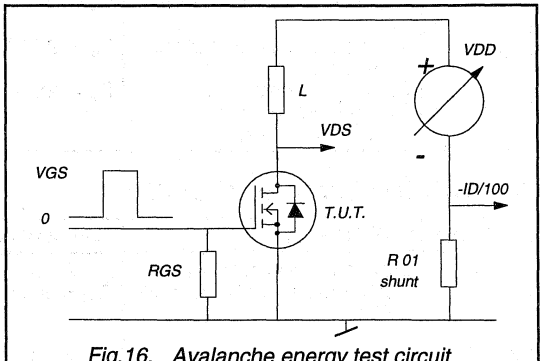


Fig.16. Avalanche energy test circuit.
$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$

PowerMOS transistor
Isolated version of PHP2N40E

PHX1N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

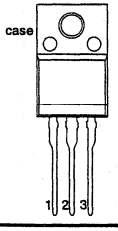
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	1.75	A
P_{tot}	Total power dissipation	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	3.5	Ω

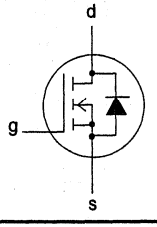
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.75	A
		T_{hs} = 100 °C	-	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	7.0	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	1.75	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	7.0	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2.5 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	120	mJ
		T_j = 100°C prior to surge	-	20	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 2.5 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \leq$ 150 °C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.25 A	-	3.1	3.5	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2.5 A ;V_{GS} = 0 V	-	1.4	2.0	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1.25 A	0.5	0.9	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Feedback capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	- - -	225 30 6.0	315 42 12	pF pF pF
$Q_{g(tot)}$ Q_{gs} Q_{gd}	Total gate charge Gate to source charge Gate to drain (Miller) charge	V_{GS} = 10 V; I_D = 2.5 A; V_{DS} = 320 V	- - -	12 2 6	- - -	nC nC nC
$t_{d\,on}$ t_r $t_{d\,off}$ t_f	Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time	V_{DD} = 30 V; I_D = 2.2 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{GEN} = 50 Ω	- - - -	10 30 30 20	15 45 40 30	ns ns ns ns
t_{rr} Q_{rr}	Source-drain diode reverse recovery time Source-drain diode reverse recovery charge	I_F = 2.5 A; -dI_F/dt = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	- -	350 2.5	- -	ns µC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version fo PHP1N50E

PHX1N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

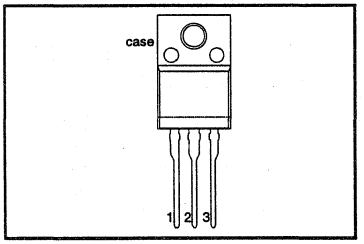
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	1.4	A
P_{tot}	Total power dissipation	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	5	Ω

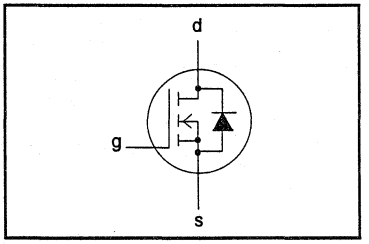
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.4	A
		T_{hs} = 100 °C	-	0.9	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	5.6	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	1.4	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	5.6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	120	mJ
		T_j = 100°C prior to surge	-	20	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \leq$ 150 °C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1 A	-	4.5	5.0	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2 A ;V_{GS} = 0 V	-	0.8	1.2	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1 A	0.5	0.9	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	230	300	pF
C_{oss}	Output capacitance		-	35	50	pF
C_{rss}	Feedback capacitance		-	14	30	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 2 A; V_{DS} = 400 V	-	10	-	nC
Q_{gs}	Gate to source charge		-	1	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	5	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	45	ns
$t_{d\,off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	40	ns
t_f	Turn-off fall time		-	20	30	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	2.5	-	µC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version of PHP1N60E

PHX1N60E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

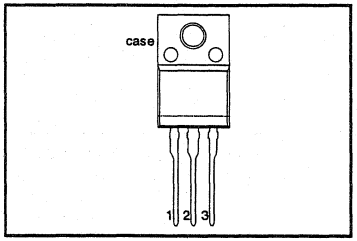
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	1.3	A
P_{tot}	Total power dissipation	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	6	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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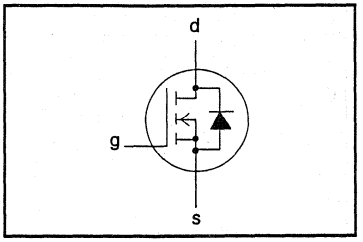


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.3	A
		T_{hs} = 100 °C	-	0.83	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	5.2	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	1.3	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	5.2	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.9 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	120	mJ
		T_j = 100°C prior to surge	-	20	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 1.9 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.9 A	-	5.3	6	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 1.9 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 0.9 A	0.5	0.8	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	224	310	pF
C_{oss}	Output capacitance		-	27	40	pF
C_{rss}	Feedback capacitance		-	6	10	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 1.9 A; V_{DS} = 480 V	-	10	-	nC
Q_{gs}	Gate to source charge		-	1	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	5	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1.9 A;	-	10	15	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	30	45	ns
$t_{d\,off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	30	40	ns
t_f	Turn-off fall time		-	20	30	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 1.9 A; -dI_F/dt = 100 A/µs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	3.5	-	µC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version of PHP4N40E

PHX2N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

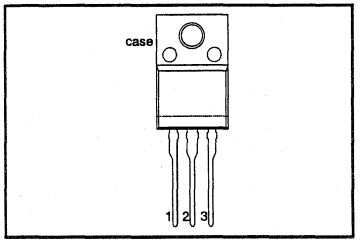
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	2.4	A
P_{tot}	Total power dissipation	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.8	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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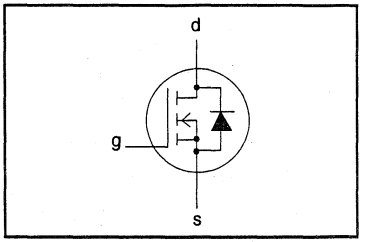


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	2.4	A
		T_{hs} = 100 °C	-	1.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	9.6	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	2.4	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	9.6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 4.2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	190	mJ
		T_j = 100°C prior to surge	-	35	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 4.2 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \leq$ 150 °C	-	5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.1 A	-	1.5	1.8	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 4.2 A ;V_{GS} = 0 V	-	1.2	1.6	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 2.1 A	1.7	2.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	360	500	pF
C_{oss}	Output capacitance		-	60	80	pF
C_{rss}	Feedback capacitance		-	25	60	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 4.2 A; V_{DS} = 320 V	-	19	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	10	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.5 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 4.2 A; -dI_F/dt = 100 A/µs;	-	300	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	2.5	-	µC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version of PHP3N50E

PHX2N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

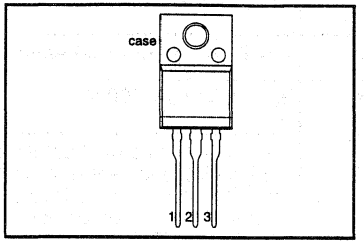
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	1.9	A
P_{tot}	Total power dissipation	25	W
$R_{DS(ON)}$	Drain-source on-state resistance	3	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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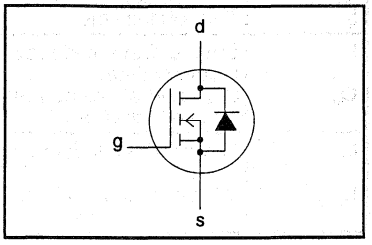


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	1.9	A
		T_{hs} = 100 °C	-	1.2	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	7.6	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	1.9	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	7.6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	25	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 3.2 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	210	mJ
		T_j = 100°C prior to surge	-	33	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 3.2 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.6 A	-	2.4	3.0	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 3.2 A ;V_{GS} = 0 V	-	1.1	1.5	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1.6 A	1.0	2.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	400	500	pF
C_{oss}	Output capacitance		-	55	80	pF
C_{rss}	Feedback capacitance		-	20	55	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 3.2 A; V_{DS} = 400 V	-	20	-	nC
Q_{gs}	Gate to source charge		-	2	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	10	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.3 A;	-	15	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	40	60	ns
$t_{d\,off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	50	65	ns
t_f	Turn-off fall time		-	30	40	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 3.2 A; -dI_F/dt = 100 A/μs;	-	350	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	3.5	-	μC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version of PHP3N50E

PHX2N60E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

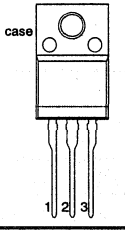
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	2.4	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	2.2	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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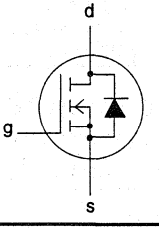


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	2.4	A
		T_{hs} = 100 °C	-	1.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	9.6	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	2.4	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	9.6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 4.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	290	mJ
		T_j = 100°C prior to surge	-	46	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 4.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	7.5	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.15 A	-	2.1	2.2	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 4.3 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 2.15 A	1.5	2.5	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Feedback capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	- - -	750 90 40	1000 140 70	pF pF pF
$Q_{g(tot)}$ Q_{gs} Q_{gd}	Total gate charge Gate to source charge Gate to drain (Miller) charge	V_{GS} = 10 V; I_D = 4.3 A; V_{DS} = 480 V	- - -	35 8 14	- - -	nC nC nC
$t_{d\,on}$ t_r $t_{d\,off}$ t_f	Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time	V_{DD} = 30 V; I_D = 2.5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{GEN} = 50 Ω	- - - -	10 45 100 40	45 60 140 65	ns ns ns ns
t_{rr} Q_{rr}	Source-drain diode reverse recovery time Source-drain diode reverse recovery charge	I_F = 4.3 A; -dI_F/dt = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	- -	1200 6.0	- -	ns µC
L_d L_s	Internal drain inductance Internal source inductance	Measured from drain lead 6 mm from package to centre of die Measured from source lead 6 mm from package to source bond pad	- -	4.5 7.5	- -	nH nH

PowerMOS transistor
Isolated version of PHP5N40E

PHX4N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

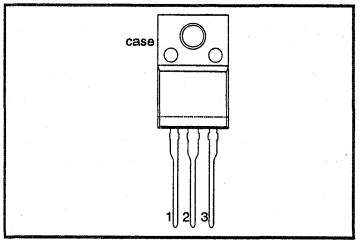
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	3.6	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.0	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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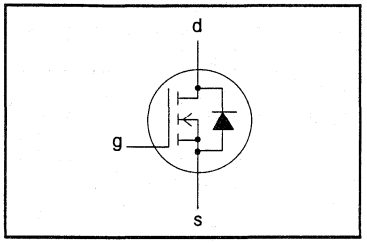


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	3.6	A
		T_{hs} = 100 °C	-	2.3	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	14.4	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	3.6	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	14.4	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	290	mJ
		T_j = 100°C prior to surge	-	46	mJ
W_{DSR} [1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	7.4	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.25 A	-	0.8	1.0	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 6.5 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 3.25 A	2.0	3.5	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Feedback capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	- - -	750 120 50	1000 180 70	pF pF pF
$Q_{g(tot)}$ Q_{gs} Q_{gd}	Total gate charge Gate to source charge Gate to drain (Miller) charge	V_{GS} = 10 V; I_D = 6.5 A; V_{DS} = 320 V	- - -	35 4 18	- - -	nC nC nC
$t_{d\,on}$ t_r $t_{d\,off}$ t_f	Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time	V_{DD} = 30 V; I_D = 2.7 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{GEN} = 50 Ω	- - - -	10 25 120 40	25 40 140 65	ns ns ns ns
t_{rr} Q_{rr}	Source-drain diode reverse recovery time Source-drain diode reverse recovery charge	I_F = 6.5 A; -dI_F/dt = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	- -	1200 6.0	- -	ns μC
L_d L_s	Internal drain inductance Internal source inductance	Measured from drain lead 6 mm from package to centre of die Measured from source lead 6 mm from package to source bond pad	- -	4.5 7.5	- -	nH nH

PowerMOS transistor
Isolated version of PHP4N50E

PHX4N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

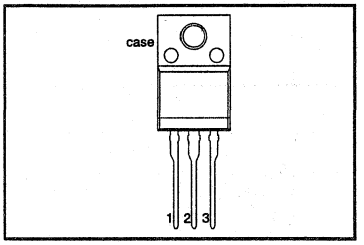
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	2.9	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.5	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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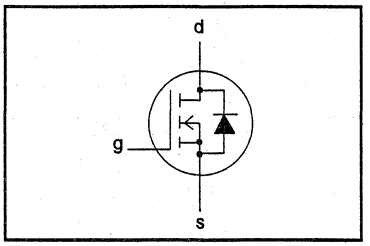


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	2.9	A
		T_{hs} = 100 °C	-	1.8	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	11.6	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	2.9	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	11.6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 5.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	280	mJ
		T_j = 100°C prior to surge	-	44	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 5.3 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	7.4	mJ

Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.65 A	-	1.3	1.5	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 5.3 A ;V_{GS} = 0 V	-	1.1	1.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 2.65 A	1.5	2.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	750	1000	pF
C_{oss}	Output capacitance		-	90	140	pF
C_{rss}	Feedback capacitance		-	40	70	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 5.3 A; V_{DS} = 400 V	-	35	-	nC
Q_{gs}	Gate to source charge		-	4	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	16	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.6 A;	-	10	45	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	45	60	ns
$t_{d\,off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	100	140	ns
t_f	Turn-off fall time		-	40	65	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 5.3 A; -dI_F/dt = 100 A/µs;	-	1200	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6	-	µC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version of PHP6N60E

PHX4N60E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

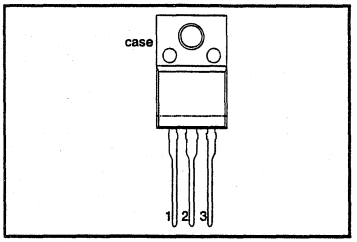
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	3.2	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.2	Ω

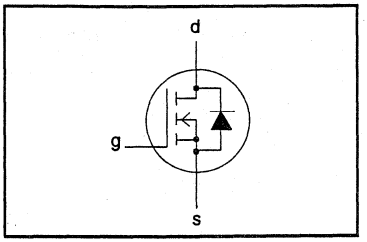
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	3.2	A
		T_{hs} = 100 °C	-	2.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	13	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	3.2	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	13	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	570	mJ
		T_j = 100°C prior to surge	-	91	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 6.5 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	13	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 480 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3.25 A	-	0.87	1.2	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 6.5 A ;V_{GS} = 0 V	-	1.1	1.5	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 3.25 A	2.5	5	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Feedback capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	- - -	1500 170 70	1800 270 120	pF pF pF
$Q_{g(tot)}$ Q_{gs} Q_{gd}	Total gate charge Gate to source charge Gate to drain (Miller) charge	V_{GS} = 10 V; I_d = 6.5 A; V_{DS} = 480 V	- - -	67 7 33	- - -	nC nC nC
$t_{d\,on}$ t_r $t_{d\,off}$ t_f	Turn-on delay time Turn-on rise time Turn-off delay time Turn-off fall time	V_{DD} = 30 V; I_D = 2.8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{GEN} = 50 Ω	- - - -	20 60 200 75	40 90 250 90	ns ns ns ns
t_{rr} Q_{rr}	Source-drain diode reverse recovery time Source-drain diode reverse recovery charge	I_F = 6.5 A; -dI_F/dt = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	- -	500 6	- -	ns µC
L_d L_s	Internal drain inductance Internal source inductance	Measured from drain lead 6 mm from package to centre of die Measured from source lead 6 mm from package to source bond pad	- -	4.5 7.5	- -	nH nH

PowerMOS transistor
Isolated version of PHP10N40E

PHX5N40E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

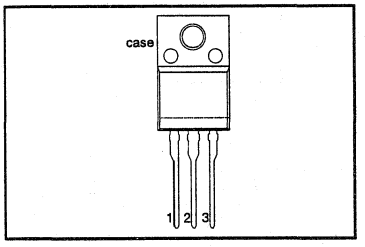
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (DC)	4.9	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.55	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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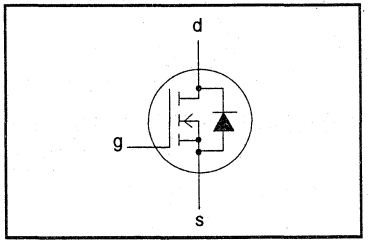


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	400	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	4.9	A
		T_{hs} = 100 °C	-	3.0	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	19.6	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	4.9	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	19.6	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	520	mJ
		T_j = 100°C prior to surge	-	83	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 10 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	13	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	400	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	-	0.4	0.55	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 10 A ;V_{GS} = 0 V	-	1.4	2.0	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 5 A	4	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	1800	pF
C_{oss}	Output capacitance		-	170	270	pF
C_{rss}	Feedback capacitance		-	70	120	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 10 A; V_{DS} = 320 V	-	65	-	nC
Q_{gs}	Gate to source charge		-	8	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	37	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.8 A;	-	20	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	200	250	ns
t_f	Turn-off fall time		-	75	90	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 10 A; $-dI_F/dt$ = 100 A/µs;	-	500	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6.0	-	µC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PowerMOS transistor
Isolated version of PHP8N50E

PHX5N50E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a full pack, plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

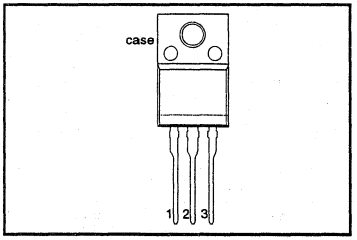
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	4	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.8	Ω

PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



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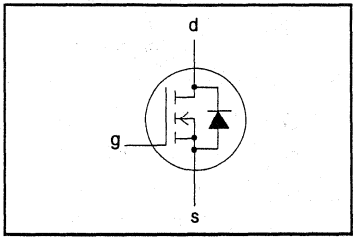


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{hs} = 25 °C	-	4	A
		T_{hs} = 100 °C	-	2.5	A
I_{DM}	Drain current (pulse peak value)	T_{hs} = 25 °C	-	16	A
I_{DR}	Source-drain diode current (DC)	T_{hs} = 25 °C	-	4	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{hs} = 25 °C	-	16	A
P_{tot}	Total power dissipation	T_{hs} = 25 °C	-	30	W
T_{stg}	Storage temperature		-55	150	°C
T_j	Junction temperature		-	150	°C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 8 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω			
		T_j = 25°C prior to surge	-	510	mJ
		T_j = 100°C prior to surge	-	82	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 8 A; $V_{DD} \leq$ 50 V; V_{GS} = 10 V; R_{GS} = 50 Ω; $T_j \leq$ 150 °C	-	13	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	10	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 4 A	-	0.67	0.8	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 8 A ;V_{GS} = 0 V	-	1.4	2.0	V

DYNAMIC CHARACTERISTICS

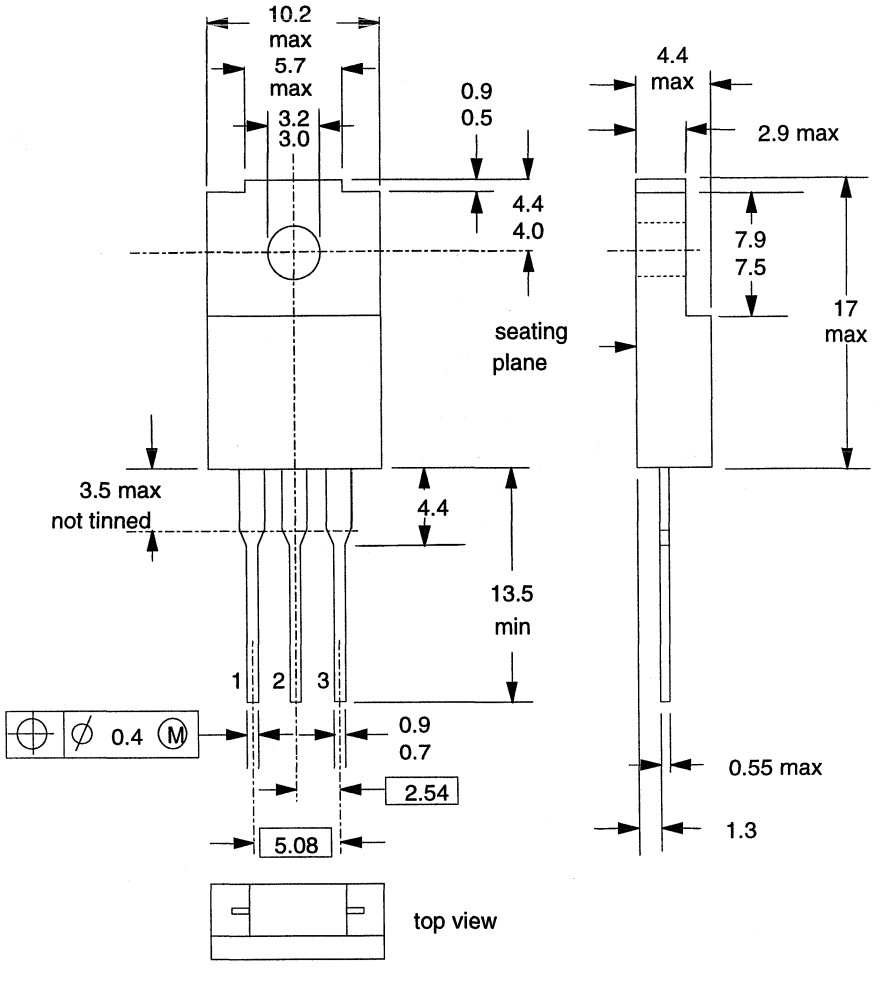
T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 4 A	4	6	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1500	1800	pF
C_{oss}	Output capacitance		-	170	270	pF
C_{rss}	Feedback capacitance		-	70	120	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 8 A; V_{DS} = 400 V	-	65	-	nC
Q_{gs}	Gate to source charge		-	8	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	34	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.8 A;	-	20	40	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	60	90	ns
$t_{d\,off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	200	250	ns
t_f	Turn-off fall time		-	75	90	ns
t_{rr}	Source-drain diode reverse recovery time	I_F = 8 A; -dI_F/dt = 100 A/µs;	-	500	-	ns
Q_{rr}	Source-drain diode reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	6	-	µC
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

PACKAGE OUTLINES

Dimensions in mm

Net Mass: 2 g



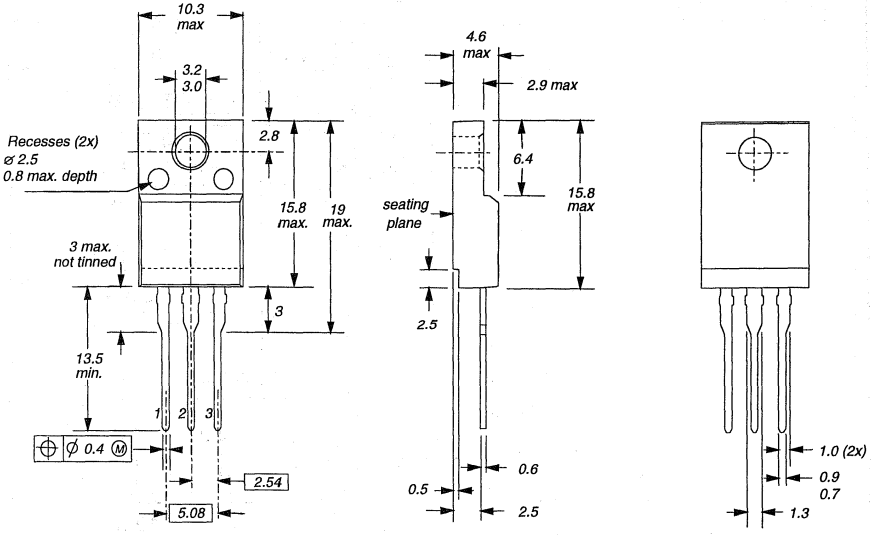
SOT186; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 2 g



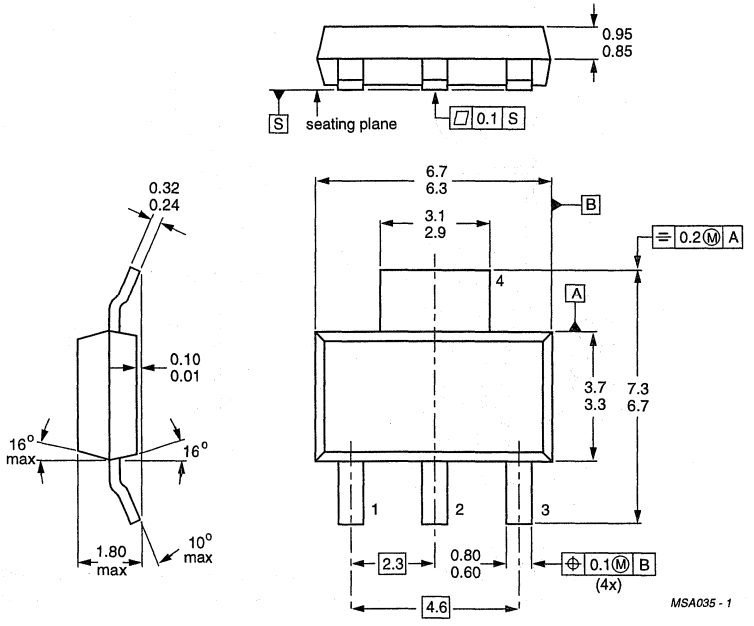
SOT186A; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 0.11 g

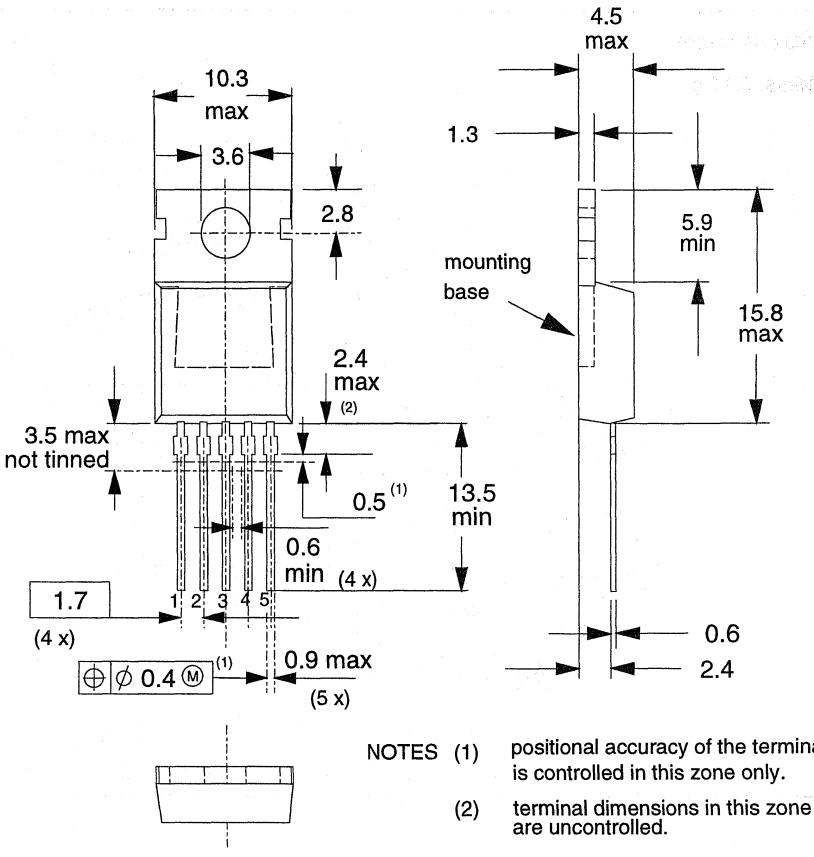


SOT223 surface mounting package[1].

1 For further information, refer to surface mounting instructions for SOT223 envelope. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 2 g



NOTES (1) positional accuracy of the terminals is controlled in this zone only.

(2) terminal dimensions in this zone are uncontrolled.

SOT263 (5-pin TO220);

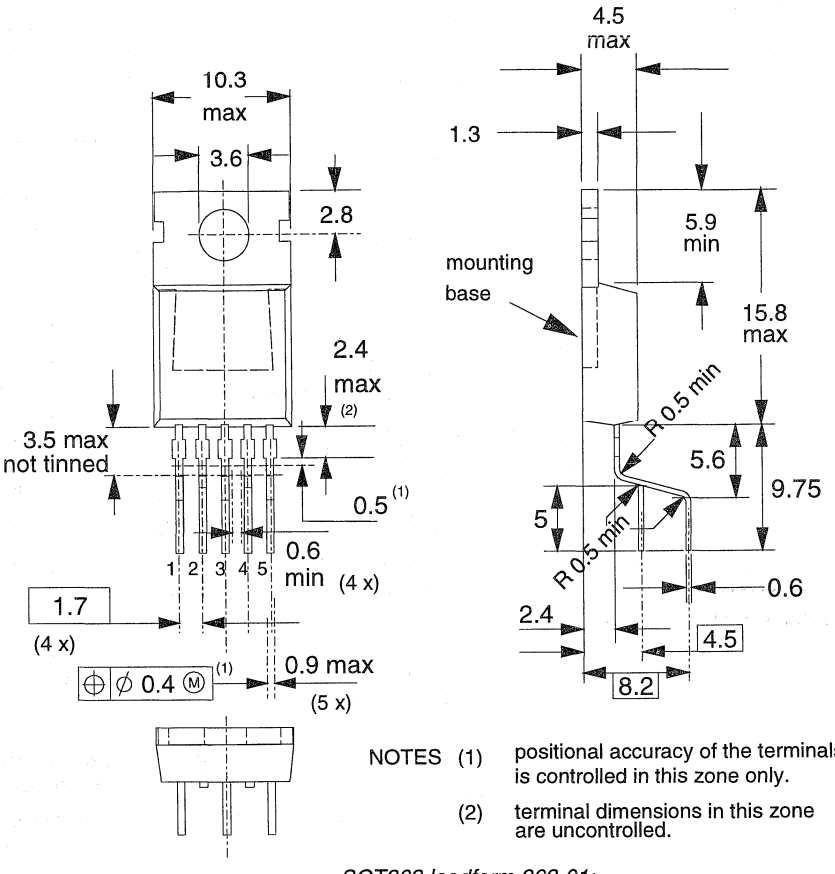
pin 3 connected to mounting base.

Note

1. Refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 2 g



NOTES (1) positional accuracy of the terminals is controlled in this zone only.

(2) terminal dimensions in this zone are uncontrolled.

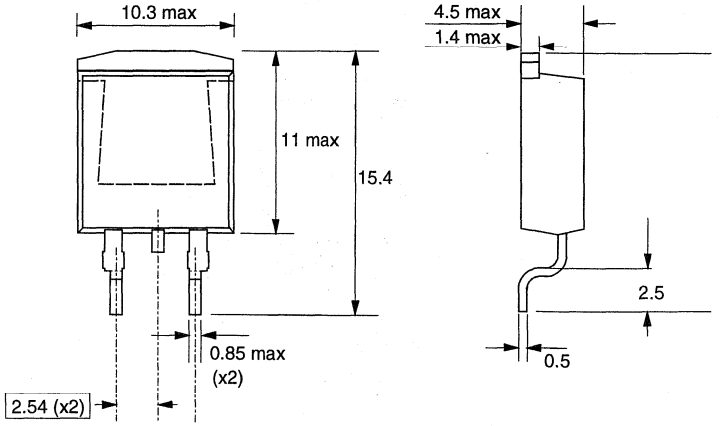
SOT263 leadform 263-01;

pin 3 connected to mounting base.

Note
1. Refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 1.4 g



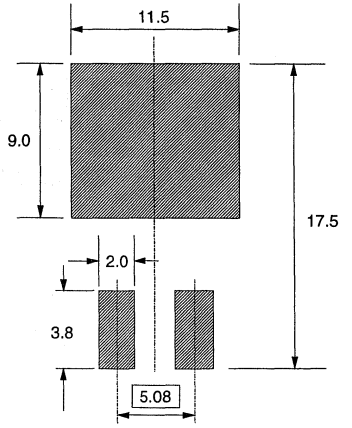
SOT404 : centre pin connected to mounting base.

Notes

1. Epoxy meets UL94 V0 at 1/8".

MOUNTING INSTRUCTIONS

Dimensions in mm



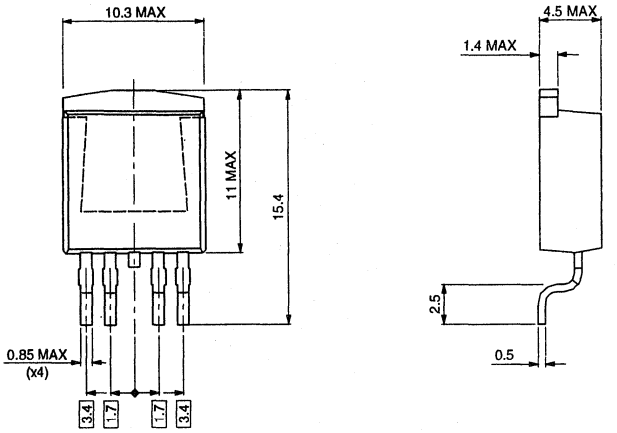
SOT404 : minimum pad sizes for surface mounting.

Notes

1. Plastic meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 1.5 g

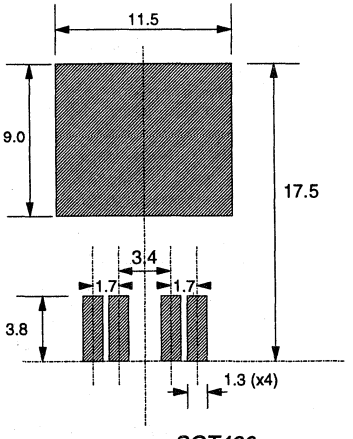


SOT426

mounting base connected to centre pin (cropped short)

MOUNTING INSTRUCTIONS

Dimensions in mm



SOT426

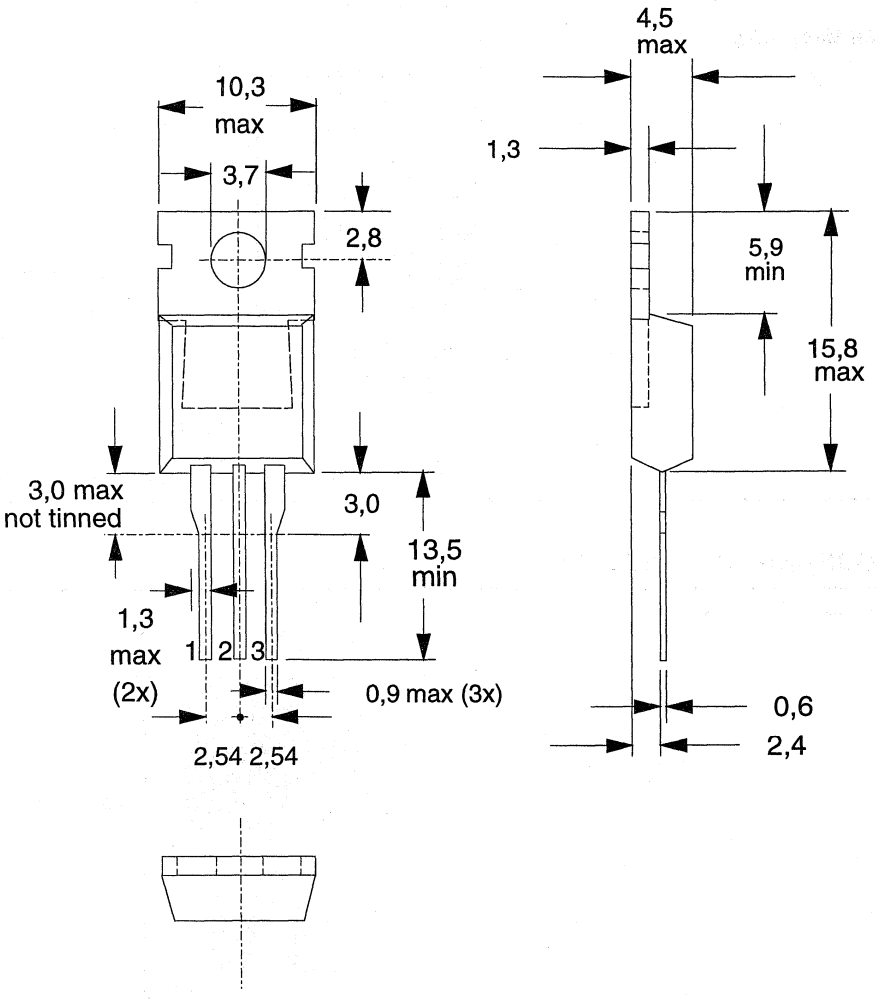
soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

Dimensions in mm

Net Mass: 2 g



TO220AB; pin 2 connected to mounting base.

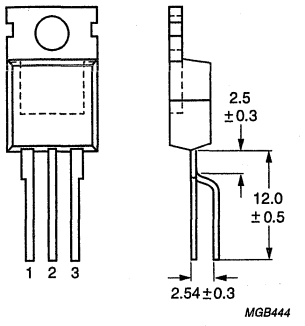
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for TO220 envelopes.
3. Epoxy meets UL94 V0 at 1/8".

LEADFORM OPTIONS

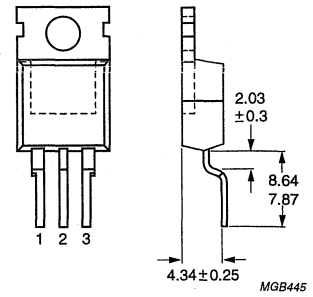
LEADFORM OPTIONS

- These options require a special part number before ordering.
- Contact your local Philips Semiconductors representative for pricing, minimum order quantities and part number.



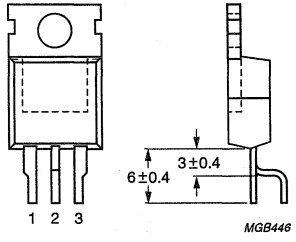
SOT78 (TO-220)

Fig.1 Leadform 78-02.



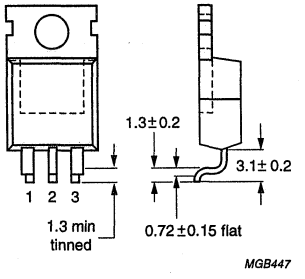
SOT78 (TO-220)

Fig.2 Leadform 78-05W.



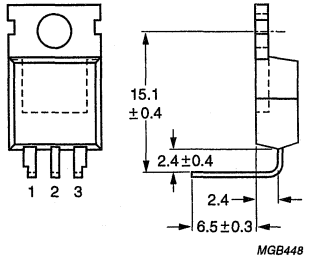
SOT78 (TO-220)

Fig.3 Leadform 78-13.



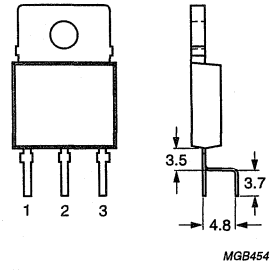
SOT78 (TO-220)

Fig.4 Leadform 78-14.



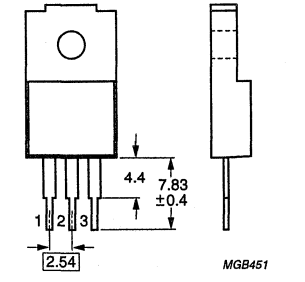
SOT78 (TO-220)

Fig.5 Leadform 78-15.



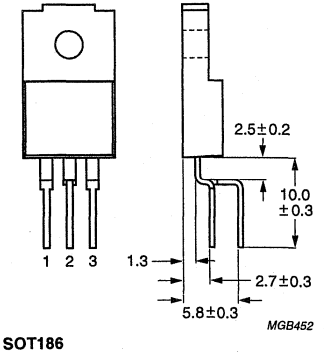
SOT93

Fig.6 Leadform 93-01.



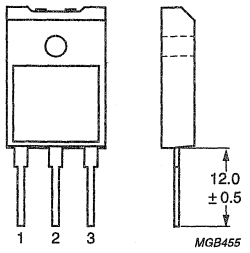
SOT186

Fig.7 Leadform 186-02.



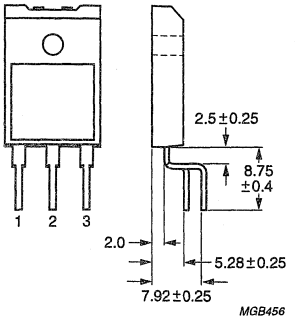
SOT186

Fig.8 Leadform 186A-02.



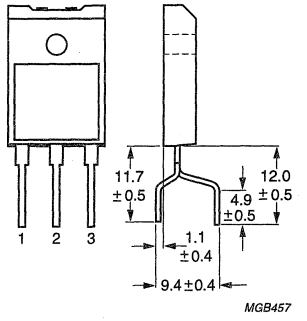
SOT199

Fig.9 Leadform 199-01.



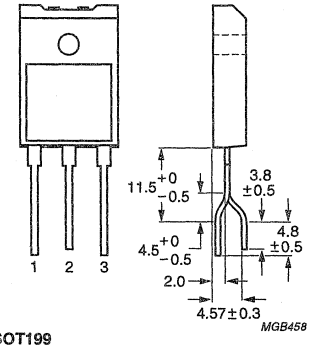
SOT199

Fig.10 Leadform 199-02.



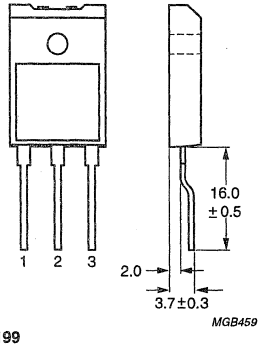
SOT199

Fig.11 Leadform 199-04.



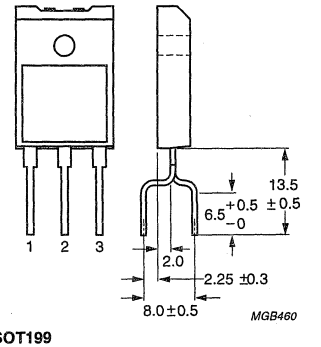
SOT199

Fig.12 Leadform 199-05.



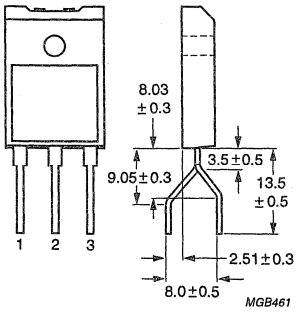
SOT199

Fig.13 Leadform 199-06.



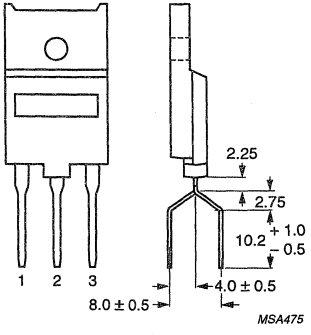
SOT199

Fig.14 Leadform 199-08.



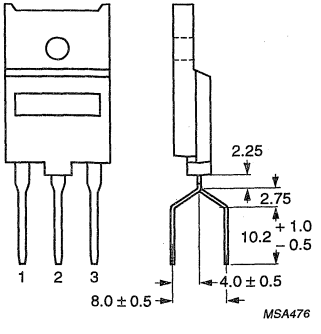
SOT199

Fig.15 Leadform 199-09.



SOT399

Fig.16 Leadform 399-01



SOT399

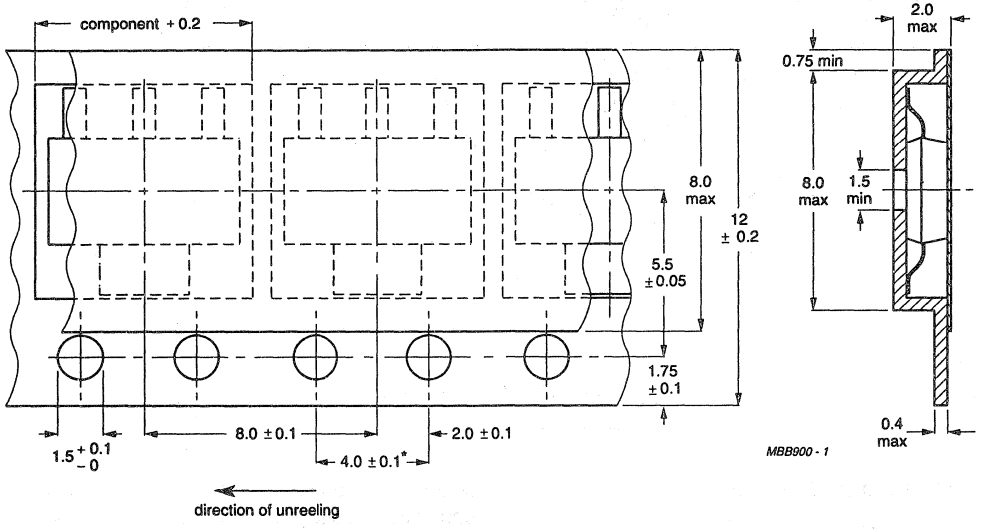
Fig.17 Leadform 399-02.

MOUNTING INSTRUCTIONS

TAPE and REEL PACKING (SOT223)

Tape and reel packing meets the feed requirements of automatic pick and place equipment (packing conforms to IEC publication 286). The tape is an ideal shipping container, making handling easy and providing secure blister cavities in which the transistors are sealed with peel-off cover tape.

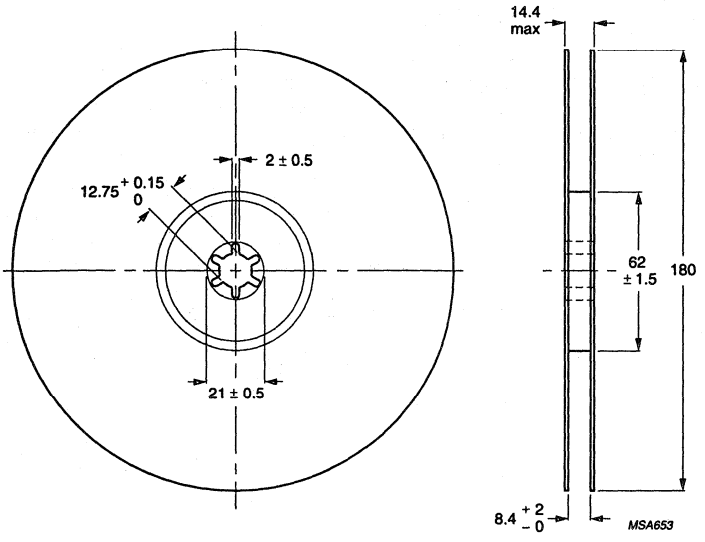
Packing quantities for SOT223 are 1000 pieces per 7-inch (180 mm) reel.



Dimensions in mm.

Tolerance over any 10 pitches: ±0.2 mm.

Fig.1 Specification for 12 mm tape, 7-inch reel (SOT223).



Dimensions in mm.

Fig.2 Reel for blister tape.

MOUNTING AND SOLDERING (SOT223)

Mounting methods

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting (SMD). Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly. Surface mounting techniques are complex and this chapter gives only a simplified overview of the subject.

Not all electronic components are available as surface mounting types and this often leads to the mixing of through-hole with surface mounting components on one substrate (a mixed print). The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double-sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

Reflow soldering

This is the preferred soldering technique for SOT223 components.

SOLDER PASTE

Most reflow soldering techniques utilize a paste that is a mixture of flux and solder. The solder paste is applied to the substrate before the components are placed. It is of sufficient viscosity to hold the components in place and, therefore, an application of adhesive is not required. Drying of the solder paste by preheating increases the viscosity and prevents any tendency for the components to become displaced during the soldering process. Preheating also minimizes thermal shock and drives off flux solvents.

Screen printing

This is the best high-volume production method of solder paste application. An emulsion-coated, fine mesh screen with apertures etched in the emulsion to coincide with the surfaces to be soldered is placed over the substrate. A squeegee is passed across the screen to force solder paste through the apertures and on to the substrate. The layer thickness of screened solder paste is usually between 150 and 200 µm.

Stencilling

In this method a stencil with etched holes to pass the paste is used. The thickness of the stencil determines the amount of amount of solder paste that is deposited on the substrate. This method is also suited to high-volume work.

Dispensing

A computer-controlled pressure syringe dispenses small doses of paste to where it is required. This method is mainly suitable for small production runs and laboratory use.

Pin transfer

A pin picks up a droplet of solder paste from a reservoir and transfers it to the surface of the substrate or component. A multi-pin arrangement with pins positioned to match the substrate is possible and this speeds up the process time.

REFLOW TECHNIQUES

Thermal conduction

The prepared substrates are carried on a conveyor belt, first through a preheating stage and then through a soldering stage. Heat is transferred to the substrate by conduction through the belt. Figure 3 shows a theoretical time/temperature relationship for thermal conduction reflow soldering. This method is particularly suited to thick film substrates and is often combined with infrared heating.

Infrared

An infrared oven has several heating elements giving a broad spectrum of infrared radiation, normally above and below a closed loop belt system. There are separate zones for preheating, soldering and cooling. Dwell time in the soldering zone is kept as short as possible to prevent damage to components and substrate. A typical heating profile is shown in Fig.4. This reflow method is often applied in double-sided prints.

Vapour phase

A substrate is immersed in the vapours of a suitable boiling liquid. The vapours transfer latent heat of condensation to the substrate and solder reflow takes place. Temperature is controlled precisely by the boiling point of the liquid at a given pressure. Some systems employ two vapour zones, one above the other. An elevator tray, suspended from a hoist mechanism passes the substrate vertically through the first vapour zone into the secondary soldering zone and then hoists it out of the vapour to be cooled. A theoretical time/temperature relationship for this method is shown in Fig.5.

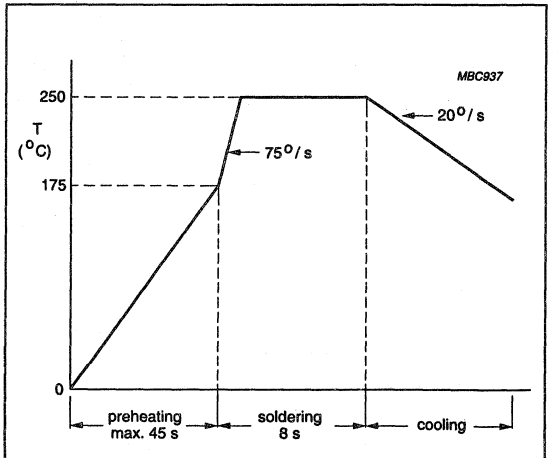


Fig.3 Theoretical time/temperature curve for a typical thermal conduction reflow cycle.

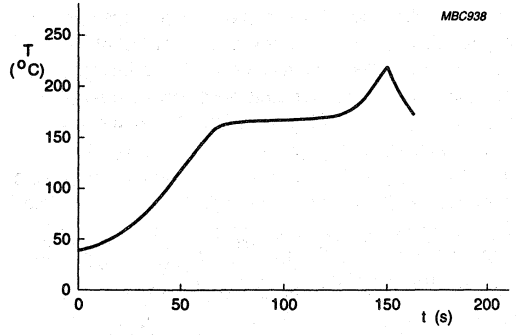


Fig.4 Typical temperature profile of an infrared oven operating at a belt speed of 0.41 m/min.

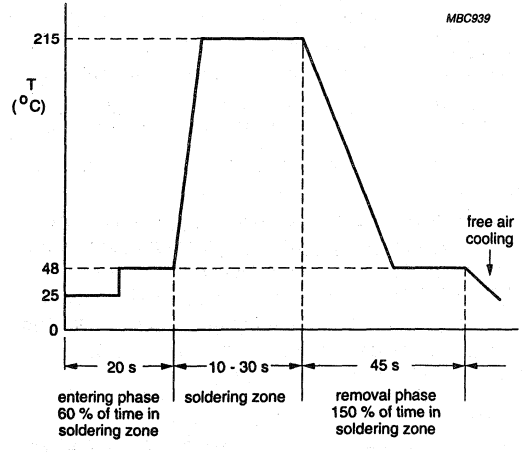


Fig.5 Theoretical time/temperature curve relationship for dual vapour reflow soldering.

Wave soldering

This soldering technique can be applied to SOT223 components.

ADHESIVE APPLICATION

Since there are no connecting wires to retain them, leadless and short-leaded components are held in place with adhesive for wave soldering. A spot of adhesive is carefully placed between each SMD and the substrate. The adhesive is then heat-cured to withstand the forces of the soldering process, during which the components are fully immersed in solder. There are several methods of adhesive application.

Pin transfer method

A pin is used to transfer a droplet of adhesive from a reservoir to a precise position on the surface where it is required. The size of the droplet depends on pin diameter, depth to which the pin is dipped in the reservoir, rheology of the adhesive, and the temperature of adhesive and surrounds. The pin can be part of a pin array (bed of nails) that corresponds exactly with the required adhesive positions on the substrate. With this method, adhesive can be applied to the whole of one side of a substrate in one operation and is therefore suitable for high-volume production and can be used with pre-loaded mixed prints.

Alternatively, pins can be used to transfer adhesive to the components before they are placed on the substrate. This adds flexibility to production runs where variations in layout must be accommodated.

Screen printing method

A fine mesh screen is coated with emulsion except in the positions where the adhesive is required to pass. The screen is placed on the substrate and a squeegee passing across it forces adhesive through the uncoated parts of the screen. The amount of adhesive printed-through depends on the size of the uncoated screen areas, the thickness of the screen coating, the rheology of the adhesive and various machine parameters. With this method, the substrate must be flat and pre-loaded mixed prints cannot be accommodated.

Pressure syringe method

A computer-controlled syringe dispenses adhesive from an enclosed reservoir by means of pulses of compressed air. The adhesive dot size depends on the size of the syringe nozzle, the duration and pressure of the pulsed

air and the viscosity of the adhesive. This method is most suited to low volume production. An advantage is the flexibility provided by computer programmability.

FLUXING

The quality of the soldered connections between components and substrate is critical for circuit performance and reliability. Flux promotes solderability of the connecting surfaces and is chosen for the following attributes:

- Removal of surface oxides
- Prevention of reoxidation
- Transference of heat from source to joint area
- Residue that is non-corrosive or, if residue is corrosive, should be easy to clean away after soldering
- Ability to improve wettability (readiness of a metal surface to form an alloy at its interface with the solder) to ensure strong joints with low electrical resistance
- Suitability for the desired method of flux application.

In wave soldering, liquified flux is usually applied as a foam, a spray or in a wave.

Foam

Flux foam is made by forcing low-pressure, water-free clean air through an aerator immersed in liquid flux. Fine bubbles of flux are directed onto the substrate/component surfaces where they burst and form a thin, even layer. The flux also penetrates any plated-through holes. The flux has to be chosen for its foaming capabilities.

Spray

Several methods of spray fluxing exist, the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate. The amount of flux deposited is controllable by the speed of the substrate passing through the spray, the speed of rotation of the drum and the density of the flux.

Wave

A wave fluxer creates a double flowing wave of liquid flux which adheres to the surface as the substrate passes through. Wave height control is essential and a soft wipe-off brush is usually incorporated to remove excess flux from the substrate.

PRE-HEATING

Pre-heating of the substrate and components is performed immediately before soldering. This reduces thermal shock as the substrate enters the soldering process, causes the flux to become more viscous and accelerates the chemical action of the flux and so speeds up the soldering action.

SOLDERING

Wave soldering is usually the best method to use when high throughput rates are required. The single-wave soldering principle (Fig.6) is the most straight forward method and can be used on simple substrates with two-terminal SMD components. More complex substrates with increased circuit density and closer spacing of conductors can pose the problems of nonwetting (dry joints) and solder bridging. Bridging can occur across the closely spaced leads of multi-leaded devices as well as across adjacent leads on neighbouring components. Nonwetting is usually caused by components with plastic bodies. The plastic is not wetted by solder and creates a depression in the solder wave, which is augmented by surface tension. This can cause a shadow behind the component and prevent solder from reaching the joint surfaces. A smooth laminar solder wave is required to avoid bridging and a high pressure wave is needed to completely cover the areas that are difficult to wet. These conflicting demands are difficult to attain in a single wave but dual wave techniques go a long way in overcoming the problem.

In a dual wave machine (Fig.7), the substrate first comes into contact with a turbulent wave which has a high vertical velocity. This ensures good solder contact with both edges of the components and prevents joints from being missed. The second smooth laminar wave completes the formation of the solder fillet, removes excess solder and prevents bridging. Figure 8 indicates the time/temperature relationship measured at the soldering site in dual wave soldering.

New methods of wave soldering are developing continually. For example, the Omega System is a single wave agitated by pulses, which combines the functions of smoothness and turbulence. In another, a lambda wave injects air bubbles in the final part of the wave. A further innovation is the hollow jet wave in which the solder wave flows in the opposite direction to the substrate.

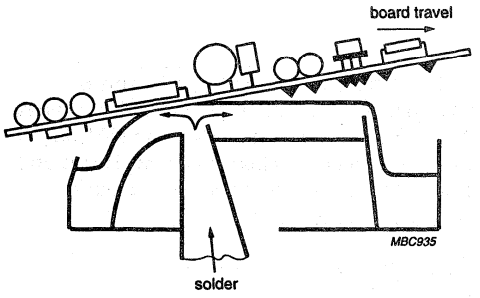


Fig.6 Single wave soldering principle.

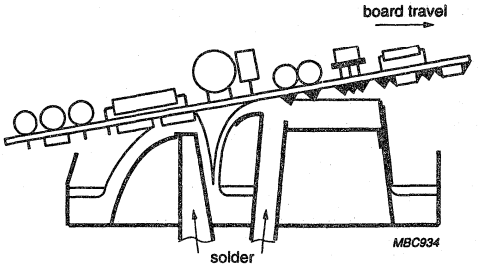


Fig.7 Dual wave soldering principle.

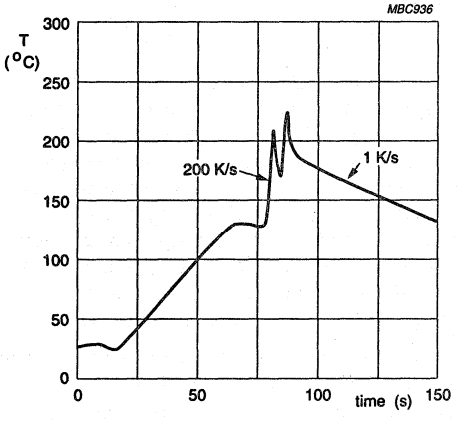


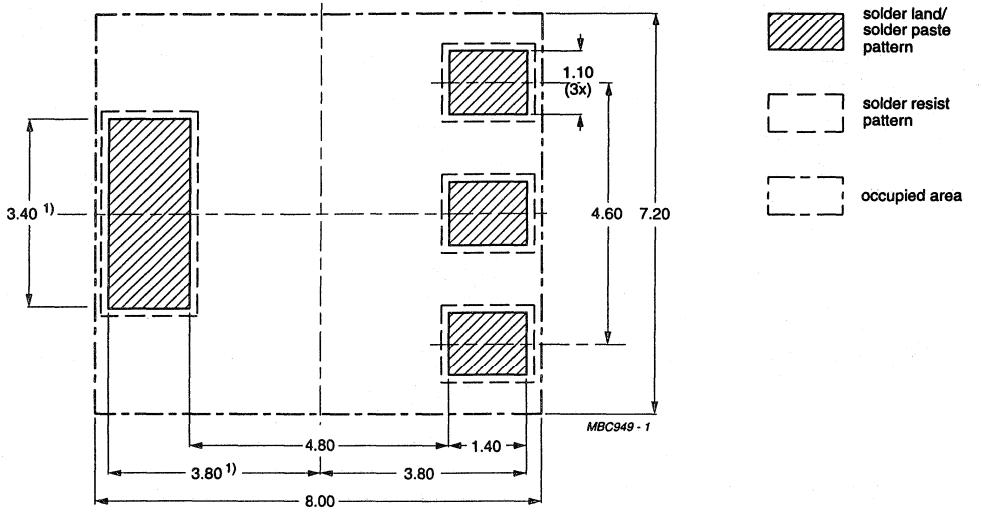
Fig.8 Typical time-temperature curve measured at the soldering site.

Footprint design

The footprint design of a component for surface mounting is influenced by many factors:

- Features of the component, its dimensions and tolerances
- Circuit board manufacturing processes
- Desired component density
- Minimum spacing between components
- Circuit tracks under the component
- Component orientation (if wave soldering)
- Positional accuracy of solder resist to solder lands
- Positional accuracy of solder paste to solder lands (if reflow soldering)
- Component placement accuracy
- Soldering process parameters
- Solder joint reliability parameters.

SOT223 FOOTPRINTS

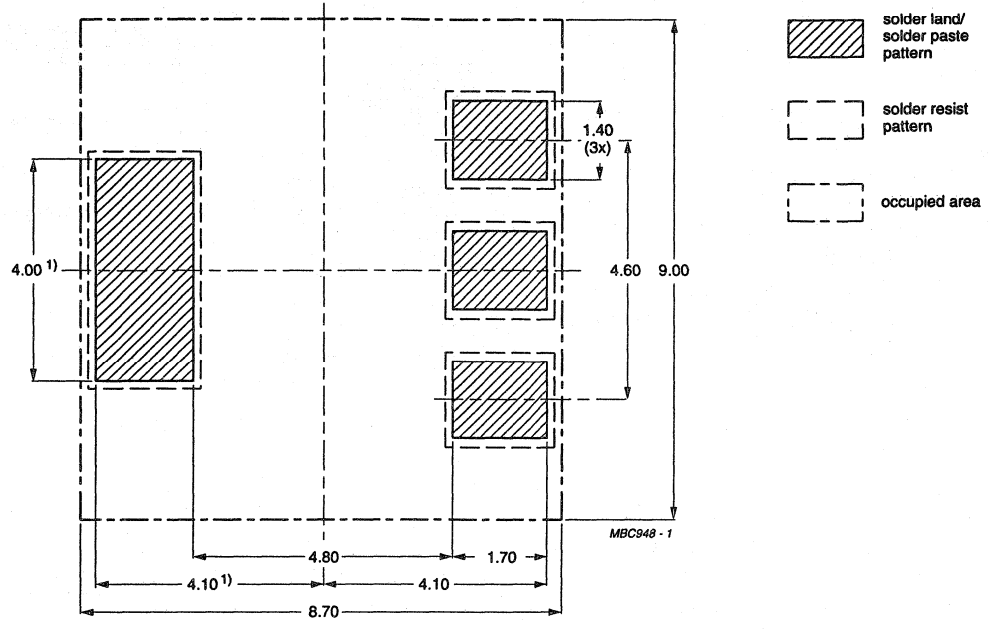


Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve the power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.9 Reflow soldering footprint for SOT223; typical dimensions.



Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.10 Wave soldering footprint for SOT223; typical dimensions.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- Hand-soldering is time-consuming and therefore expensive
- The component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- There is a risk of breaking the substrate and internal connections in the component could be damaged
- The component envelope could be damaged by the soldering iron.

THERMAL CONSIDERATIONS

Thermal resistance

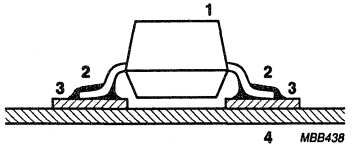
Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a substrate. Referring to Fig.11, heat conducts from its source (the junction) via the envelope leads and soldered connections to the substrate. Some heat radiates from the envelope into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The elements of thermal resistance shown in Fig.12 are defined as follows:

$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base
$R_{th\ j\text{-}c}$	thermal resistance from junction to case
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point
$R_{th\ s\text{-}a}$	thermal resistance from soldering point to ambient
$R_{th\ c\text{-}a}$	thermal resistance from case to ambient ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$ are the same for most envelopes)
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient.



Heat radiates from the envelope (1) to ambient.

Heat conducts via leads (2), solder joints (3) to the substrate (4).

Fig.11 Heat losses.

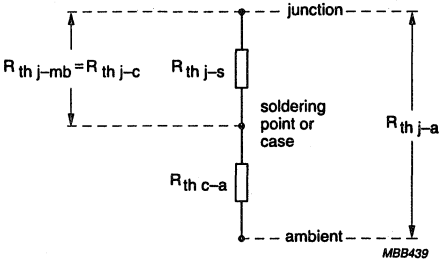


Fig.12 Representation of thermal resistance paths of a device mounted on a substrate or printed board.

The temperature at the junction depends on the ability of the envelope and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$T_{j\ max} = T_{amb} + P_{tot\ max}\ (R_{th\ j\text{-}s} + R_{th\ s\text{-}a})$

$= T_{amb} + P_{tot\ max}\ (R_{th\ j\text{-}a})$

where

$T_{j\ max}$ is the maximum junction temperature

T_{amb} is the ambient temperature

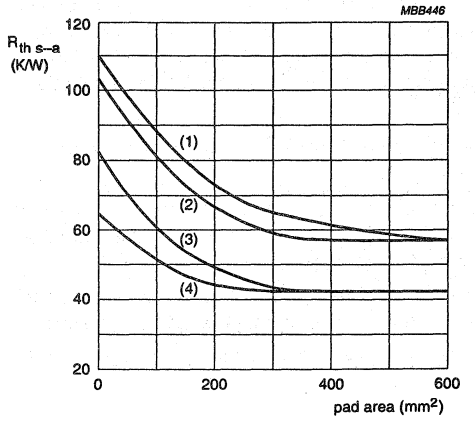
$P_{tot\ max}$ is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\ max}$, only T_{amb} and $R_{th\ s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\ s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\ j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the envelope construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\ max}$ and $R_{th\ j\text{-}s}$ or $R_{th\ j\text{-}c}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from $T_j = T_{case} + P_{tot} \times R_{th\ j\text{-}c}$ or, using the soldering point definition, from $T_j = T_{solder} + P_{tot} \times R_{th\ j\text{-}s}$.

Thermal resistance ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$)

The thermal resistance from soldering point to ambient and that from case to ambient depends on the shape and material of the tracks and substrate as illustrated in Figs 13 and 14. Standard mounting conditions to set the maximum power ratings of the SOT223 envelope are shown in Fig.15. This shows single-sided 35 µm copper-clad epoxy fibre-glass print, 1.5 mm thick. the tracks are fully solder-tinned and the shaded areas shown are copper.



(1) single-sided, unplated

(2) single-sided, plated

(3) double-sided, unplated

(4) double-sided, plated.

Fig.13 Thermal resistance ($R_{th\ s\text{-}a}$) as a function of pad area on different configurations of FR4 epoxy fibre-glass circuit board.

GENERAL DATA AND INSTRUCTIONS

General rules

1. Fasten the device to the heatsink before soldering the leads.
2. Avoid stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.
4. The rectangular washer may only touch the plastic part of the body; it should not exert any force on that part (screw mounting).

Mounting methods

CLIP MOUNTING

Mounting with a spring clip gives:

a) A good thermal contact under the crystal area, and slightly lower thermal resistance than screw mounting.

b) Safe insulation for mains operation.

Minimum force for good heat transfer is 10 N.

Maximum force to avoid damaging the device is 80 N.

M3 SCREW MOUNTING

It is recommended that the rectangular spacing washer is inserted between screw head and mounting tab.

Do not use self-tapping screws.

Mounting torque for screw mounting:

For thread-forming screws these are final values.

Minimum torque for good heat transfer is 0.55 Nm.

Maximum torque to avoid damaging the device is 0.80 Nm.

When a nut or screw is driven directly against the tab, the torques are as follows:

Minimum torque for good heat transfer is 0.40 Nm.

Maximum torque to avoid damaging the device is 0.60 Nm.

RIVET MOUNTING NON-INSULATED.

The device should not be pop-rivetted to the heatsink. It is permissible to press-rivet the metal tab providing that eyelet rivets of soft material are used, and the press forces are slowly and carefully controlled.

This method is not permitted for full-pack envelopes because it will damage the plastic encapsulation.

Heatsink requirements

Flatness in the mounting area: 0.02 mm maximum per 10 mm.
Mounting holes must be deburred, for further information see clip and screw mounting instructions.

Heatsink compound

The thermal resistance from mounting base to heatsink ($R_{th\ mb\text{-}h}$) can be reduced by applying a metallic oxide compound between the contact surfaces. Values given are of thermal resistance using this type of compound. Dow Corning 340 Heat sink compound is recommended. For insulated mounting, the compound should be applied to the bottom of both device and insulator.

Mounting instructions

SOT223

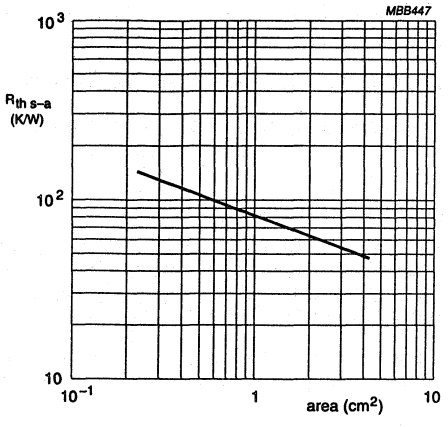


Fig.14 Thermal resistance ($R_{th\ s-a}$) as a function of area of ceramic substrate.

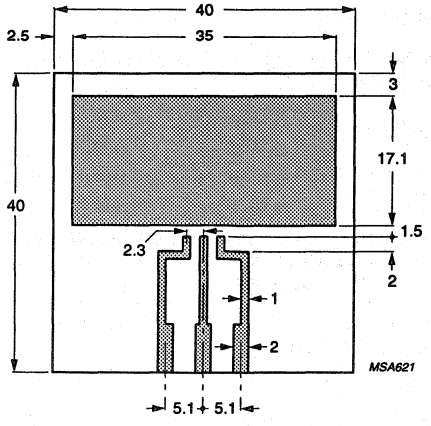


Fig.15 Test circuit for SOT223.

Thermal data for heatsink mounting methods (TO220 only)

Typical figures, for exact figures see data for each device type.

$R_{th\ mb\text{-}h}$	Thermal resistance from mounting base to heatsink	K/W	
Mounting method		**clip**	**screw**
direct with heatsink compound		0.3	0.5
direct without heatsink compound		1.4	1.4
with heatsink compound and 0.1 mm maximum mica insulator		2.2	-
with heatsink compound and 0.25 mm maximum alumina insulator		0.8	-
with heatsink compound and 0.05 mm mica insulator			
	insulated up to 500 V	-	1.4
	insulated up to 800 V / 1000 V	-	1.6
without heatsink compound and 0.05 mm mica insulator			
	insulated up to 500 V	-	3.0
	insulated up to 800 V / 1000 V	-	4.5

Additional insulators are generally not required when mounting the full-pack outlines.

Soldering

Recommendations for devices with a maximum junction temperature rating < 175 °C:

DIP OR WAVE SOLDERING.

Maximum permissible solder temperature is 260 °C at a distance from the body of > 5 mm and for a total contact time with soldering bath or waves of < 7 s.

HAND SOLDERING.

Maximum permissible temperature is 275 °C at a distance from the body of > 3 mm and for a total contact time with the soldering iron of < 5 s.

The body of the device must not touch anything with a temperature > 200 °C.

It is not permitted to solder the metal tab of the device to a heatsink, otherwise the junction temperature rating will be exceeded.

Avoid any force on body and leads during or after soldering; do not correct the position of the device or of its leads after soldering.

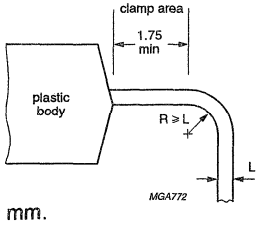
Lead bending

Maximum permissible tensile force on the body for 5 seconds is 20 N.

The leads can be bent, twisted or straightened. To keep forces within the above mentioned limits the leads should always be clamped rigidly near the body during bending. This is also to prevent damage to the seal of the leads within the plastic body.

Leads can be bent as near to the body as required, but adequate length should always be allowed for clamping. This is a minimum of 1.75 mm from the body to the start of a bend radius.

The internal radius of bend should never be less than the thickness of the lead. A minimum radius of at least 1.5 x lead thickness is preferred. See figure 1. Surface cracks in the dip tin coating on the lead are common when a radius less than 1.5 x lead thickness is used. Although exposing the copper material, these cracks do not affect the mechanical strength of the lead. Lead forming by Philips is available as an option on all products supplied in these outlines.



Dimensions in mm.

Fig 1. Minimum lead bend radius.

Additional guide-lines

It is recommended that where a device is rigidly secured to a heatsink which is in turn rigidly secured to a PCB, that a bend is put in the leads to act as an expansion loop. This will prevent differential expansion of the mounting parts transferring stress to the soldering joint, as shown in figure 2 below. This is only necessary where the device is mounted so rigidly that expansion forces are transmitted through the assembly.

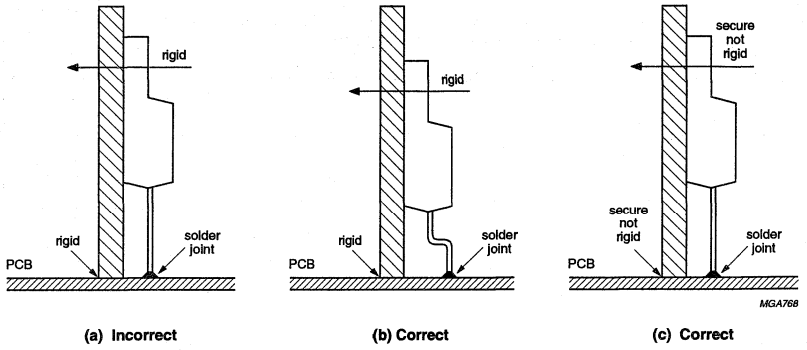
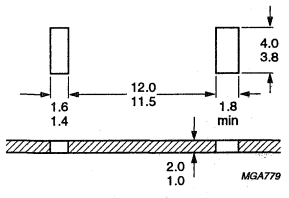


Fig 2. Printed circuit board and heatsink mounting.

INSTRUCTIONS FOR CLIP MOUNTING

Direct mounting with clip 56363

1. Apply heatsink compound to the mounting base, then place the device on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See figures 3 and 4.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. See figure 5.



Dimensions in mm.

Fig 3. Heatsink requirements.

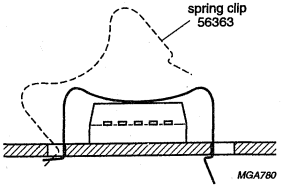


Fig 4. Mounting.

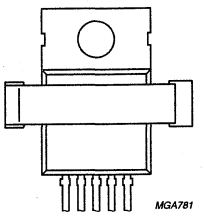
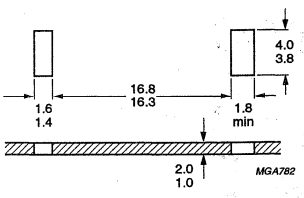


Fig 5. Position of device (top view).

Insulated mounting with clip 56364

With the insulators 56367 or 56369 insulation up to 2 kV is obtained.

1. Apply heatsink compound to the bottom of both device and insulator, then place the device with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of 10° to 30° to the vertical. See figures 6, 7 and 8.
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. Ensure that the device is centred on the mica insulator to prevent unwanted movement.



Dimensions in mm.

Fig 6. Heatsink requirements.

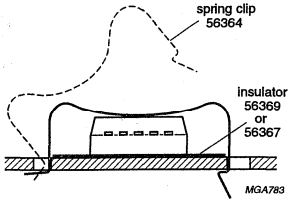


Fig 7. Mounting.

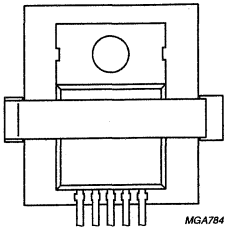


Fig 8. Position of device (top view).

INSTRUCTIONS FOR SCREW MOUNTING

Direct mounting with screw and spacing washer

THROUGH HEATSINK WITH NUT

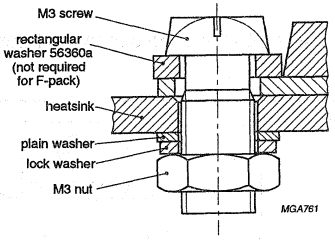
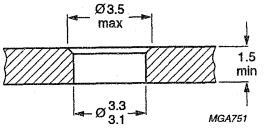


Fig 9. Assembly



Dimensions in mm.

Fig 10. Heatsink requirements.

INTO TAPPED HEATSINK

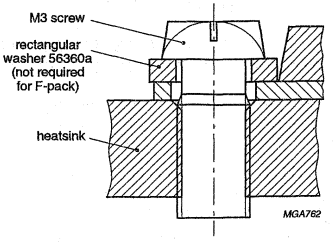
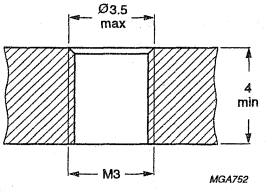


Fig 11. Assembly.



Dimensions in mm.

Fig 12. Heatsink requirements.

Insulated mounting with screw and spacing washer

Not recommended where mounting tab is on mains voltage. Not applicable for F-pack.

THROUGH HEATSINK WITH NUT

Known as a "bottom mounting".

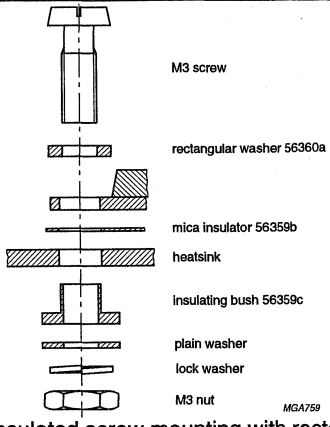


Fig 13. Insulated screw mounting with rectangular washer.

Dimensions in mm.

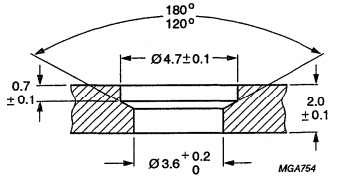


Fig 14. Heatsink requirements for 500 V insulation.

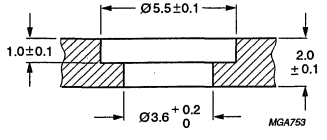


Fig 15. Heatsink requirements for 800 V insulation.

INTO TAPPED HEATSINK

Known as a "top mounting".

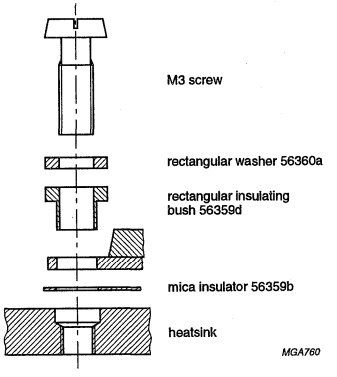


Fig 16. Insulated screw mounting with rectangular washer into tapped heatsink.

Dimensions in mm.

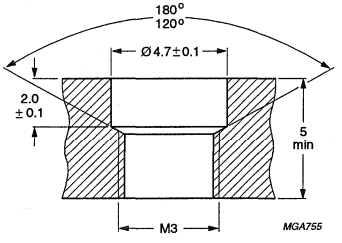


Fig 17. Heatsink requirements for 500 V insulation.

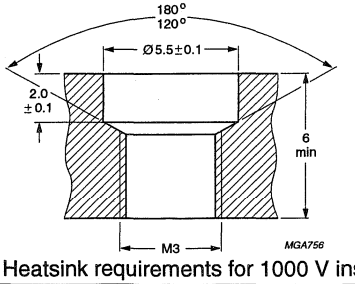


Fig 18. Heatsink requirements for 1000 V insulation.

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DATA HANDBOOK SYSTEM

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SC07	Small-signal Field-effect Transistors
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SC08b	RF Power Transistors for UHF
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